AN785

Simplify A/D Converter Interface with Software

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INTRODUCTION

Integrating analog-to-digital converters (ADCs) featuring binary-coded decimal (BCD) outputs for display interface offer a number of excellent features, as well as high resolution, at a very low cost. These advantages include auto-zeroing, sign-magnitude coding, noise averaging, and high impedance inputs and are also attractive for microprocessor-based systems. Unfortunately, many display-oriented ADCs are difficult to interface due to the multiplexed BCD format of the outputs. An exception is the 4-1/2 digit TC7135 ADC, which provides a "strobe" output.

This output allows the number of I/O port pins required to interface a 4-1/2 digit ADC chip to a microprocessor (µP) to be reduced from 15 lines (see reference) to only 10 lines by counting the digit strobes in a software register. In addition to freeing I/O pins for other applications, this method also results in slightly faster interrupt response because the µP does not have to loop while identifying each digit. Although the hardware and software shown are designed for the 8080, 8085 or Z-80, the same method can be applied to 6502 or 6800 I/O devices.

INTERFACE HARDWARE

The complete TC7135-to-18255A hardware interface is shown in Figure 1. The only digit strobe used is DS5 (MSD), and the BUSY output is ignored. To understand why the other digit strobes are not required, refer to the TC7135 output timing diagram, Figure 2. The STROBE output goes low five times per conversion cycle. The first STROBE pulse occurs in the middle of DS5 when BCD data for the most significant digit (MSD) is available on outputs B1–B8. STROBE also pulses LOW during the following DS4 through DS1 signals, after which STROBE remains high until the next conversion cycle. Therefore, only one STROBE pulse occurs for each digit select, and each STROBE corresponds to a BCD digit in MSD-to-LSD order. The read the ADC's data, the µP simply reads BCD data during each STROBE pulse and stores that data in memory locations corresponding to the number of STROBE pulses received.

Reference: Smith, M. F., "Interface program links A/D chip with microprocessor," Electronics, Nov. 3, 1982, pp. 124, 125.

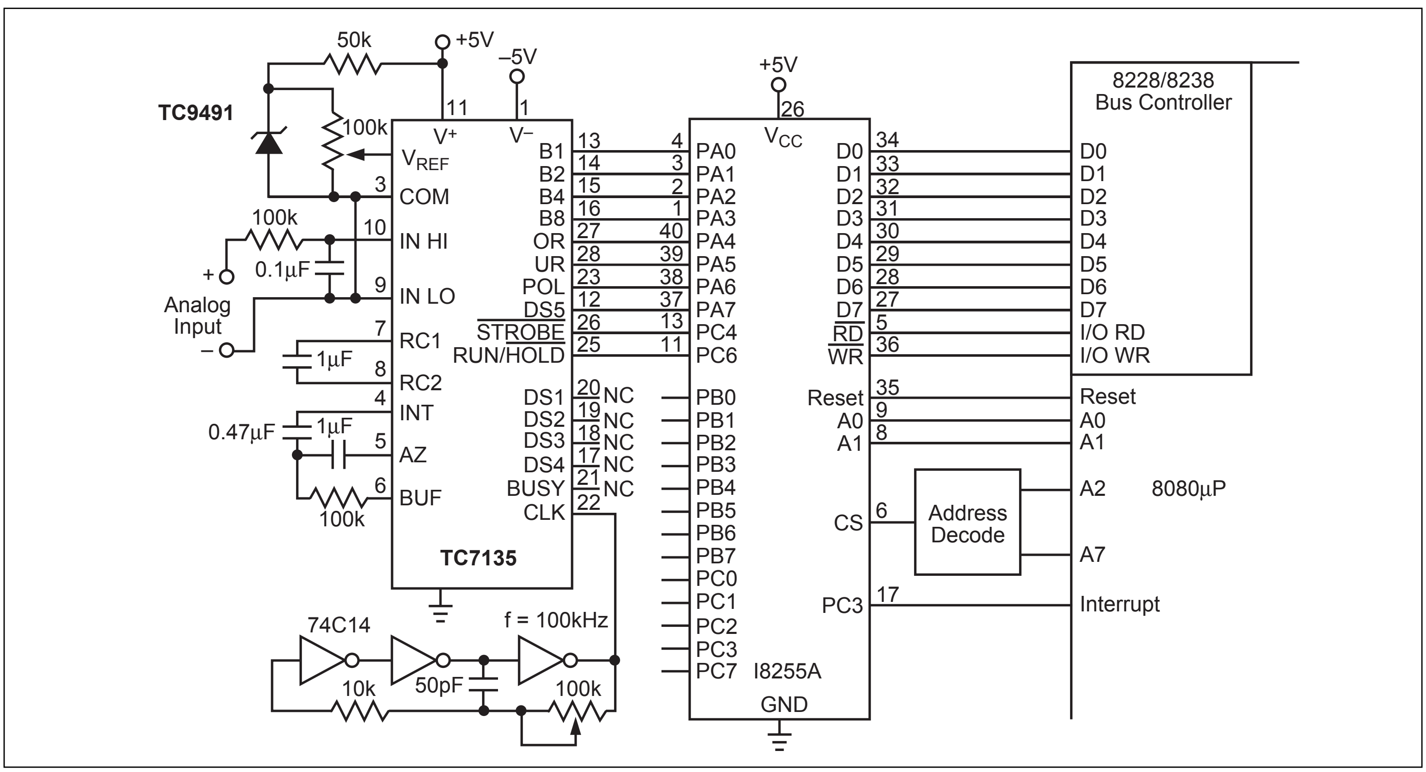


FIGURE 1: TC7135 to I/O port interface.

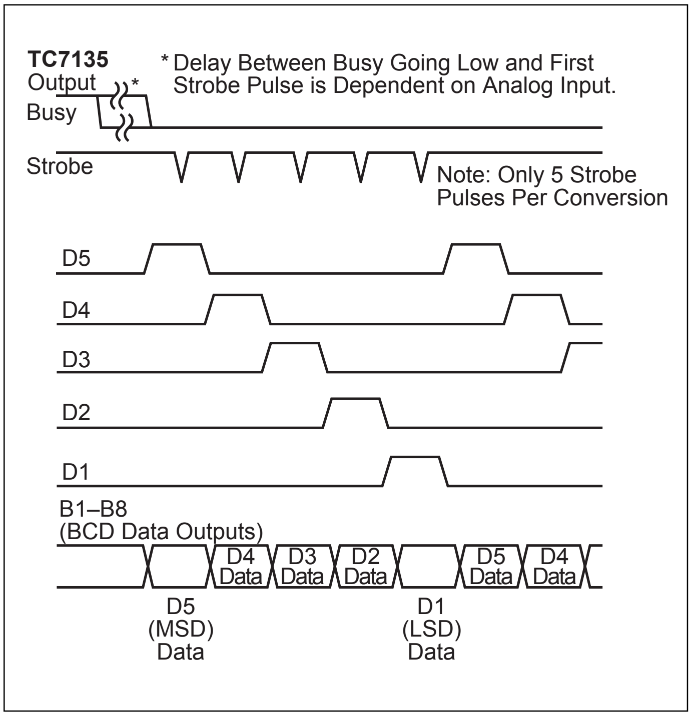


FIGURE 2: TC7135 output timing relationships.

Synchronizing Data Transfer

The microprocessor must be able to identify an end-of-conversion so that each digit will be stored in its proper location. Since the TC7135 has a BUSY output, the processor could simply monitor this output for end-of-conversion status. However, this method requires an extra input bit, as well as processor time, to test for BUSY status. By using software to identify the end-of-conversion, both software and hardware can be simplified.

In order to synchronize data transfer between the µP and ADC, the µP tests the most significant bit of I/O Port A for the presence of DS5. If DS5 is true, an end-of-conversion has occurred. The data pointer is then initialized and assembly of 5 BCD digits begins. The next four STROBE pulses will find DS5 false, so the BCD digits are simply stored in successive memory locations. The fifth STROBE pulse signals an end-of-data transfer so the user can display or manipulate the data as desired.

Initializing the I8255A I/O Port

At power-up, or after a µP reset, the I8255A is initialized for unlatched (Mode 0) input operation. In order to interface to the TC7135, the I8255A must be programmed to latch data, and generate an interrupt, from Port A (Mode 1 operation). In addition, one bit of Port C can be utilized for controlling the TC7135's RUN/HOLD input, if conversions on command are required.

Programming the I8255A is accomplished by writing data to the control register. Figure 3 outlines the function of each control bit. Writing "0B2H" to the control register, for example, configures Port A as a latched input, Port B as a nonlatched input, and remaining Port C bits as outputs.

In Port A strobed input mode, bit PC3 becomes the interrupt output. In a large system with many interrupting devices, this output would typically go to a priority interrupt controller, such as the I8259A. Smaller systems simply use a single interrupt input, with polling in software to identify the source of the interrupt. To determine if the TC7135 has caused the interrupt in a polled system, Port A Input Buffer Full (IBFA) is tested for a HIGH state. If IBFA is HIGH, data has been latched into Port A by the TC7135. Reading Port A will clear the interrupt and reset IBFA.

Programming Port A for strobed operation defines bit PC3 as an interrupt output, but a separate operation is required to enable the output. Bit PC4 is the interrupt enable bit for Port A. This bit must be set, using the Port C bit set/reset function, before the I8255A will respond to interrupts.

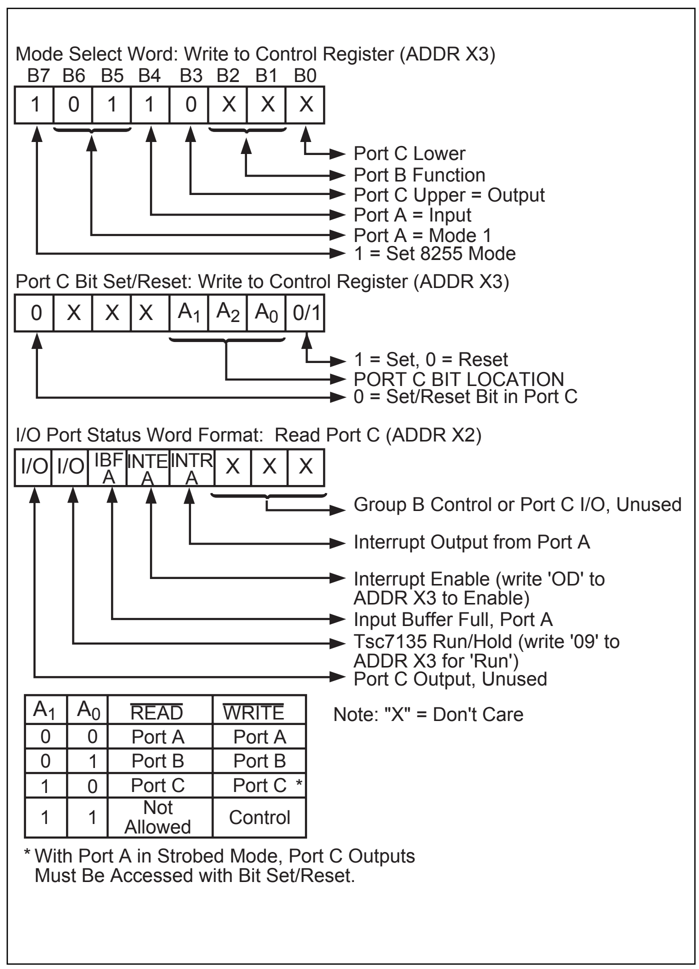


FIGURE 3: I8255A I/O port register functions.

Figure 1 also shows the TC7135's RUN/HOLD input controlled by bit PC6. Setting PC6 high results in continuous conversions. When PC6 is low, the TC7135 remains in auto-zero cycle. If PC6 pulses high, the TC7135 performs a conversion, outputs the new data, and returns to auto-zero.

INTERFACE SOFTWARE

Listing 1 shows software for acquiring data from the ADC. Two separate routines are required to program the I/O port and respond to interrupts. Code at location "SETUP" configures the I8255A for strobed input and enables Port A's interrupt.

The user must provide software for vectoring interrupts from Port A of the I8255A to interrupt service routine (SVC). As mentioned previously, SVC will test for D55 being HIGH (i.e., beginning of a new digit scan). If DS5 is HIGH, data pointer HL is loaded with the digit storage address.

If DS5 is not HIGH, or after HL has been initialized, the BCD digits are stored in memory. If 5 digits have not been received, register HL is incremented to point to the next digit storage location. After five STROBE pulses, locations STOR through STOR+4 will contain 5 BCD digits that represent the latest TC7135 conversion, plus sign, polarity, overrange and underrange flags.

Converting Multiplexed BCD Numbers to 2's Complement Format

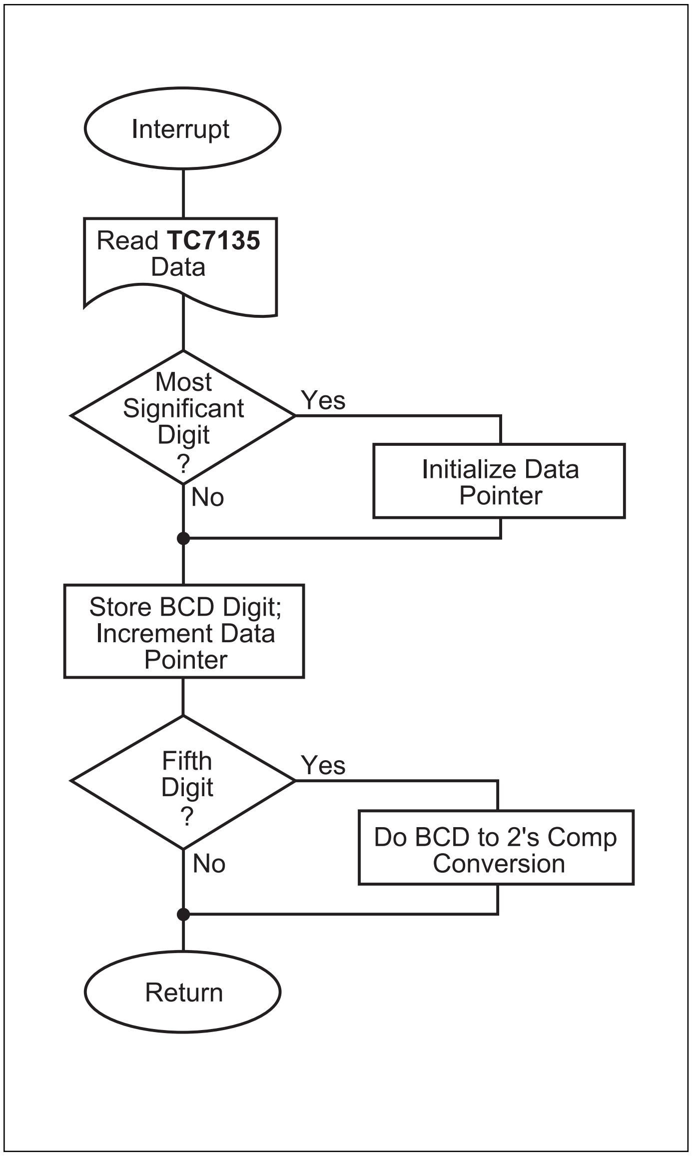
Binary-coded decimal data is convenient for driving LED displays or LCDs, but 2's complement format is usually preferred for computer arithmetic operations. Listing 2 is a program that converts 5 BCD digits to 2's complement. This program multiplies the BSD by 10, adds the next digit, multiplies the sum again, etc., until all 5 digits have been converted. The sign bit is then tested and, if negative, a 2's complement adjustment (complement all data bits and add one) is performed. Finally, the 2's complement data is stored at location AD2SCM.

```
;TC7135 TO 8255 I/O PORT INTERFACE SOFTWARE, WITH
;SIGN-MAGNITUDE TO 2'S COMPLEMENT CONVERSION
;
;
;CONFIGURE PORT A OF 8255 FOR STROBED INPUT AND
;ENABLE INTERRUPT FROM PORT A
;
;
I8255:   EQU   0               ;8255 I/O PORT ADDRESS
         ORG   20000H          ;CAN BE IN ROM OR RAM
SETUP    DI
         LD    A,0B2H          ;SET 8255A FOR LATCHED
         OUT   (I8255+3),A     ;  INPUT ON PORT A
         LD    A,0DH           ;ENABLE INTERRUPT FROM
         OUT   (I8255+3),A     ;  PORT A
         LD    A,09H           ;TURN ON TC7135
         OUT   (I8255+3),A     ;  (RUN/HOLD='RUN')
         LD    HL,STOR         ;LOAD DATA POINTER WITH
         LD    (COUNTR),HL     ;  DATA STORE ADDRESS
         EI
         JP    MAINPR              ;JUMP TO USER PROGRAM OR
;                                     TO OPERATING SYSTEM
;
;
;INTERRUPT SERVICE ROUTINE———USER MUST
;PROVIDE HARDWARE/SOFTWARE TO VECTOR
;INTERRUPTS FROM THE 8255A TO THIS ROUTINE,
;AND PROVIDE FOR SAVING REGISTERS AS REQUIRED
;
;
SVC:     IN    A,(I8255)       ;GET TC7135 DATA
         OR    A               ;SET FLAGS
         JP    P,NXTDG         ;DS5=0;NOT A NEW SCAN, GO ON
         LD    HL,STOR         ;NEW SCAN, SO SET DATA POINTR
         LD    (COUNTR),HL     ;  TO 1ST DIGIT STOR LOCATION
NXTDG:   LD    HL, (COUNTR)    ;LOAD STOR ADDR OF THIS DIGIT
         LD    (HL),A          ;STORE BCD DATA
         LD    A,L             ;GET LO BYTE OF STORE ADDR
         SUB   ENDSTR.MOD.256  ;SUBTRACT ENDING STOR ADDR-1
         JP    P,BCD2BI        ;DONE IF RESULT MINUS
         INC   HL              ;POINT TO NEXT ADDR
         LD    (COUNTR),HL     ;SAVE STORE ADDR
         RET                   ;RETURN TO MAIN PROG
;
;
;
;
```

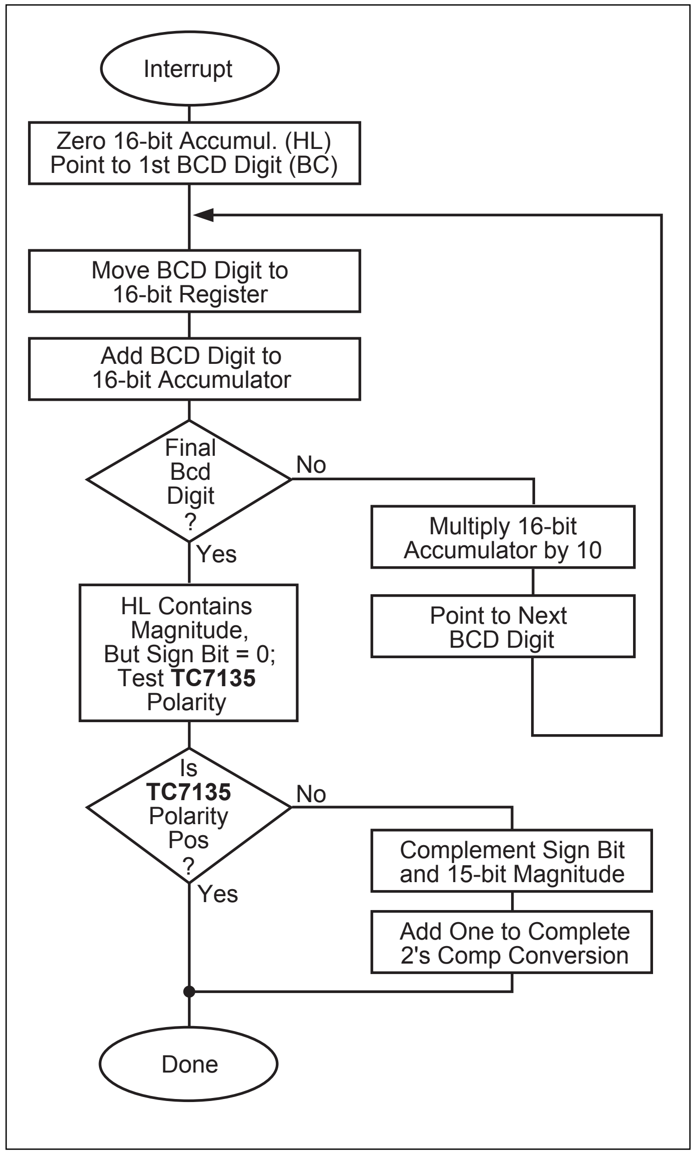
LISTING 1: TC7135-to-TC8250 interface software.

```
;
;BCD TO 2'S COMPLEMENT CONVERSION SOFTWARE
;THIS ROUTINE CONVERTS 5 BCD DIGITS LOCATED AT
;'STOR' TO 2'S COMP AND STORES RESULT AT 'AD2SCM'
;
         ORG   2040H
BCD2BI:  LD    HL,0000         ;ZERO HL REG
         LD    BC,STOR         ;POINT TO 1ST (MSD) BCD DIGIT
DIGIT:   LD    A,(BC)          ;GET DIGIT
         AND   OFH             ;MASK DS5,POL,OR,AND UR FLAGS
         LD    D,0             ;ZERO D
         LD    E,A             ;DIGIT TO E
         ADD   HL,DE           ;16 BIT ADD
         LD    A,C             ;LO BYTE OF DIGIT POINTER
         SUB   ENDSTR.MOD.256  ;COMPARE TO END; IF DONE,
         JP    P,DONE          ;  BC POINTS TO LAST DIGIT
         INC   BC              ;NOT DONE
         ADD   HL,HL           ;MULTIPLY HL BY 10;START
         PUSH  HL              ;  WITH HL#2; SAVE ON STACK
         ADD   HL,HL           ;     (HL#2)#2=HL#4
         ADD   HL,HL           ;     TIMES 2 AGAIN=HL#B
         POP   DE              ;       GET BACK HL#2
         ADD   HL,DE           ;         HL#B+HL#2=HL#10
         JP    DIGIT           ;NEXT BCD DIGIT
DONE:    LD    A,(BC)          ;BC STILL POINTS TO BCD DIGIT
         AND   40H             ;TEST 7135 POL -IF POSITIVE,
         JP    NZ,AD2CPL       ;  NO 2'S COMP CORRECTION REQ
         LD    A,H             ;RESULT NEG, SO DO A 2'S COMP
         CPL                   ;  CORRECTION BY COMPLEMENTING
         LD    H,A             ;     THE 15 BIT RESULT IN HL,
         LD    A,L             ;       AND COMPLEMENTING THE
         CPL                   ;         SIGN BIT
         LD    L,A             ;RESULT NOW IS 1'S COMP IN HL
         INC   HL              ;ADD ONE FOR 2'S COMPLEMENT
AD2CPL:  LD    (AD2SCM),HL     ;STORE RESULT AND DONE
         RET
;
;
;RESERVE STORAGE FOR POINTER AND RESULTS
;
         ORG   OBFFCH          ;MUST BE LOCATED IN RAM
COUNTR:  DEFS  2               ;STORAGE FOR DATA POINTER
STOR:    DEFS  5               ;STORAGE FOR 5 BCD DIGITS
ENDSTR:  EQU   STOR+4
AD2SCM:  DEFS  2               ;2'S COMPLEMENT DATA STOR
;
;
```

LISTING 2: BCD-to-2's complement conversion software.



FLOWCHART 1: "SVC" interruput service subroutine.



FLOWCHART 2: "BCD2B1" 2's complement conversion subroutine.

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