INTRODUCTION

Microchip Technology, Inc.’s family of micropower LDOs utilizes low-voltage CMOS process technology. These LDOs provide similar ripple rejection and dropout characteristics as their bipolar equivalents, but are significantly more efficient. A typical bipolar regulator has base current equal to 1-2% of the output load, whereas Microchip’s LDOs have approximately 60 µA resulting in total operating current orders of magnitude lower than their bipolar counterparts. In addition, Microchip’s LDOs can be placed in a shutdown mode, further enhancing their effectiveness in low-power applications.

This low-power operation makes Microchip’s family of LDOs ideal for upgrading the LP2980 and MIC5205 bipolar LDOs in cellular phones, pagers, PDAs, laptops, hand-held meters, and other portable applications.

Microchip’s micropower LDOs are available with fixed and adjustable outputs, supporting load currents up to 50 mA, 100 mA, 150 mA and 300 mA. SOT-23-5, SOT-23-6, SOT-223, and MSOP-8 packaging require minimal board space. Shutdown capability, thermal protection, and current limiting are standard in every device. Adjustable output, error flag, and noise bypass capability are provided on select devices (see Table 3).

APPLICATIONS

Optimizing Output Voltage Accuracy of TC1070/TC1071 Adjustable LDOs

Microchip’s LDOs are available in both adjustable and fixed output voltage options. The accuracy of the output depends on the initial accuracy, stability, and temperature coefficient of the internal bandgap reference and the feedback resistors.

Rather than specifying \( V_{OUT} \) accuracy on adjustable regulators, the initial accuracy and temperature coefficient of the internal reference is specified. \( V_{OUT} \) accuracy is not specified because it depends on the external feedback resistors. Figure 1 shows a typical adjustable LDO feedback circuit in which resistors \( R_1 \) and \( R_2 \) set the output voltage per the following formula:

\[
EQUATION 1: \quad V_{OUT} = V_{REF}[(R_1/R_2) + 1] \\
V_{REF} = 1.20V
\]

FIGURE 1: Adjustable LDO Feedback Circuit.

The ADJ pin is a high impedance CMOS input. Consequently, resistor values can be between 300 kΩ and 1 MΩ to minimize the current through \( R_1 \) and \( R_2 \).

Inspection of Equation 1 reveals the following:

1. When \( V_{OUT} \) is made equal to \( V_{REF} \) (i.e., \( R_1 \) is zero), the tolerance of \( V_{OUT} \) will be approximately that of \( V_{REF} \).

2. The tolerance of \( V_{OUT} \) is a function of both the tolerance of \( V_{REF} \) and the tolerance of the \( R_1/R_2 \) ratio when \( V_{OUT} \) is greater than \( V_{REF} \) (i.e., when \( R_1/R_2 > 0 \)).

For the purposes of worst case analysis, the tolerances of \( R_1 \) and \( R_2 \) are additive. For example, if \( R_1 \) and \( R_2 \) are both 1% resistors, the maximum tolerance of the \( R_1/R_2 \) ratio is 2%.

Re-examining the effect of tolerances on Equation 1 reveals that the tolerance of \( V_{OUT} \) worsens proportionally as the \( V_{OUT} \) setting departs the value of \( V_{REF} \).

EQUATION 2:

\[
ERROR_{VOUT}a(V_{OUT} - V_{REF})
\]

Table 1 shows that percentage of total output voltage error contributed by the tolerances of \( V_{REF} \) and \( R_1/R_2 \) for various values of \( V_{OUT} \).
The output voltage accuracy of the adjustable regulator improves with tighter tolerance resistors. However, accuracy will be limited to ±2% due to the accuracy of the reference. Table 2 shows output voltage accuracy for the adjustable LDO using 1%, 0.5%, and 0.1% tolerance resistors.

### TABLE 1: OUTPUT ERROR CONTRIBUTORS

<table>
<thead>
<tr>
<th>V&lt;sub&gt;OUT&lt;/sub&gt; (V)</th>
<th>Reference Tolerance (%)</th>
<th>Resistor Tolerance (%)</th>
<th>Resistor Error (%)</th>
<th>Total Output Error (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.23</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>1.23</td>
<td>2</td>
<td>2</td>
<td>0</td>
<td>2</td>
</tr>
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<td>0.77</td>
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<td>1.54</td>
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<td>3.0</td>
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<td>4.0</td>
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<td>4.0</td>
<td>2</td>
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<td>2.76</td>
<td>4.76</td>
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<td>5.0</td>
<td>2</td>
<td>1</td>
<td>1.50</td>
<td>3.5</td>
</tr>
<tr>
<td>5.0</td>
<td>2</td>
<td>2</td>
<td>3.0</td>
<td>5.0</td>
</tr>
</tbody>
</table>

### TABLE 2: RESISTOR TOLERANCE EFFECT ON V<sub>OUT</sub> ERROR

<table>
<thead>
<tr>
<th>V&lt;sub&gt;OUT&lt;/sub&gt;</th>
<th>V&lt;sub&gt;OUT&lt;/sub&gt; Error</th>
<th>1% Resistor Tol.</th>
<th>0.5% Resistor Tol.</th>
<th>0.1% Resistor Tol.</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.0V</td>
<td>3.5%</td>
<td>2.75%</td>
<td>2.15%</td>
<td></td>
</tr>
<tr>
<td>4.0V</td>
<td>3.38%</td>
<td>2.69%</td>
<td>2.14%</td>
<td></td>
</tr>
<tr>
<td>3.0V</td>
<td>3.2%</td>
<td>2.6%</td>
<td>2.12%</td>
<td></td>
</tr>
<tr>
<td>2.46V</td>
<td>3.0%</td>
<td>2.5%</td>
<td>2.10%</td>
<td></td>
</tr>
<tr>
<td>2.0V</td>
<td>2.77%</td>
<td>2.39%</td>
<td>2.08%</td>
<td></td>
</tr>
<tr>
<td>1.23V</td>
<td>2.0%</td>
<td>2.0%</td>
<td>2.0%</td>
<td></td>
</tr>
</tbody>
</table>

**Power-Saving Shutdown Mode**

All of Microchip’s micropower LDOs have a shutdown input that allows the user to digitally disconnect the load from the power source and send the regulator into a low-power “sleep” mode. The supply current is reduced from 50 µA, during normal operation, to 0.05 µA in shutdown.

The SHDN pin input current is guaranteed to be no greater than 1 µA (an order of magnitude lower than bipolar counterparts).

Shutdown mode is activated when SHDN is below 0.2 x V<sub>IN</sub>. In this mode, the pass transistor is turned OFF, disconnecting the load from the power source.

Shutdown mode is disabled, allowing normal device operation, when the input is above 0.4 x V<sub>IN</sub>. This V<sub>IN</sub> is low enough to ensure that a control output from a 3.3V microcontroller, operating from four fully-charged NiCad/ NiMH cells (6V), can enable the LDO. If not used, SHDN should not be left floating, but rather connected to V<sub>IN</sub>.

**Out-of-Regulation (ERROR) Flag**

The TC1070/1/2/3 and TC1054/5 each have Error Flag outputs that are asserted when the LDO falls out of regulation by approximately –5%.

The ERROR pin is an N-channel open-drain output that can sink up to 1 mA. However, larger value pull-up resistors should be selected so that energy loss through ERROR is kept to a minimum. ERROR must be pulled to any supply voltage less than 7V through a pull-up resistor.

ERROR output is valid for input voltages above 1V and undefined for voltages below 1V. As the output is transitioning between 0V and 1.0V during power up/ down, the Error output may float momentarily to 1.0V. If 1.0V is high enough to be interpreted as a logic ‘1’, the two-resistor network shown in Figure 2 may be used. This will ensure that ERROR never will rise above 0.5V during invalid states. Keep in mind the maximum that Error output can be in its high state is V<sub>OUT</sub>/2.

**FIGURE 2:** Ensuring Valid Error Output for Low V<sub>IN</sub> Levels.
By connecting an RC on ERROR output, it can be used as a power on reset. During power up, the Error comparator will go high as soon as the regulator output is within tolerance. ERROR will be delayed by the RC network before releasing the microcontroller from reset.

![FIGURE 3: Out-of-Regulation Error Flag.](image)

ERROR also can be used as a power quality monitor. If a low input voltage or an over-current condition causes the output to fall out of regulation, ERROR will pull low, signifying an unstable power condition. This flags the microcontroller, which now can activate proper shutdown sequencing, ensuring orderly system operation.

The Error comparator has 50 mV of positive hysteresis to provide some VIN noise immunity.

### Input, Output and Bypass Capacitors

It is recommended that input, output, and bypass capacitors be used for optimal device performance. To ensure stability in the LDO’s feedback loop, a capacitor is required from the output to ground (Figures 4 and 5). Capacitors must be chosen that meet the ESR value range and minimum capacitance identified in device data sheets. In general, a 1 µF - 2.2 µF capacitor is recommended to ensure stable operation under maximum load conditions. Larger value capacitors (4.7 µF to 10 µF) will increase transient load response and ripple rejection performance.

Ceramic capacitors offer the lowest ESR followed by, in order of increasing ESR, OS-CON, film, aluminum electrolytic, and tantalum. Film capacitors provide good performance, but usually are not a viable solution due to excessive cost and size. Ceramics combine excellent ESR with relatively small size. However, the ESR of ceramic capacitors sometimes can be too low, requiring a 1Ω series resistor to ensure stability. OS-CON capacitors offer an ESR only slightly higher than ceramics, but consume more volume. The OS-CON capacitors exhibit rock-solid ESR from −55°C to 125°C. Aluminum electrolytics are ideal for low-cost commercial temperature grade applications where board space is not a concern. Like OS-CON capacitors, electrolytics typically are offered in a radial lead package, but are available in surface mount styles. Tantalums offer an ESR similar to aluminum electrolytics. They also provide a reasonable cost, high-volume efficiency solution and are usually the capacitor of choice.

A 1 µF input capacitor should be installed from VCC to GND (Figures 4 and 5) if the IC is powered from a battery or if there is excessive (>1 ft) distance between the regulator and the AC filter capacitor. A larger value capacitor will provide better VCC noise rejection and improved performance when the supply has a high AC impedance. A 470 pF bypass capacitor can be tied to the bypass pin on the TC1014/1015 and TC1072/1073 or the ADJ pin on the TC1070/1071 (see Figure 5) to reduce the VREF noise.

### Thermal Issues

The amount of power that the LDO dissipates is a function of the bias supply current and the pass-through current. The pass-through current is the current that flows from VCC through the pass transistor of the LDO to the load. The following equation is used to calculate power dissipation:

**EQUATION 3:**

$$P_D = (V_{CC} I_S) + [(V_{CC} - V_{OUT}) I_{LOAD}]$$

Maximum values of VCC and ILOAD and minimum values for VOUT should be used when calculating PD to ensure worst-case conditions are met.

The amount of power that the LDO can dissipate depends on the ambient temperature (T_A). A guard-banded maximum die temperature (T_JMAX) of +125°C is used to account for variations in thermal conductivity of PC boards and variations in airflow.

**EQUATION 4:**

$$\theta_JA = \frac{(T_{JMAX} - T_A)}{PD_{MAX}}$$

$$\theta_JA = \theta_J + \theta_CA$$

\(\theta_J\) is the thermal resistance from the die surface to the package body and leads. \(\theta_CA\) is the thermal resistance from the package body and leads to the surrounding air, PC board dielectric, and traces.

The SOT-23-5 and SOT-23-6 packages have a worst-case \(\theta_JA\) of 220°C/W when mounted on a single-layer FR4 dielectric copper-clad PC board. This \(\theta_JA\) can be reduced by using a PC board made with a dielectric that has a better heat transfer coefficient. Additionally, adding a ground plane and large supply traces to the IC will provide better thermal conductivity. The values for \(\theta_J\) are for a system that uses natural convection. A significant reduction in \(\theta_CA\) can be induced with forced airflow.
Excessive power dissipation will result in elevated die temperatures that could activate the device’s thermal shutdown. The LDOs have an integrated thermal protection circuitry that disables the LDO when die temperatures exceed approximately +160°C. Ten degrees Celsius of hysteresis is built into the protection circuitry, such that the LDO is not released from thermal shutdown until the die temperature drops to +150°C. In addition to thermal protection, an internal sense resistor in series with the pass element provides a short-circuit limit.

<table>
<thead>
<tr>
<th>Ambient Temperature</th>
<th>$P_{D\text{MAX}}$</th>
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</thead>
<tbody>
<tr>
<td>+25°C</td>
<td>0.454W</td>
</tr>
<tr>
<td>+50°C</td>
<td>0.341W</td>
</tr>
<tr>
<td>+85°C</td>
<td>0.182W</td>
</tr>
</tbody>
</table>

**FIGURE 4:** Typical Application Circuit (Fixed Output)
FIGURE 5: Typical Application Circuit (Adjustable Output).

TABLE 3: CMOS LDOS SELECTION GUIDE

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Package</th>
<th>Output Voltage †</th>
<th>ADJ</th>
<th>SHDN</th>
<th>Error Flag</th>
<th>Bypass</th>
<th>IIS (Typ. µA)</th>
<th>IOUT (Max. mA)</th>
<th>VDROP (Typ. mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC1014</td>
<td>SOT-23-5</td>
<td>X X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>50</td>
<td>50</td>
<td>85</td>
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<td>SOT-23-5</td>
<td>X X</td>
<td>X</td>
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<td>SOT-23-5</td>
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<td></td>
<td>50</td>
<td>50</td>
<td>85</td>
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<td>X</td>
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<td>X</td>
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<td>100</td>
<td>180</td>
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</tbody>
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* Pin Compatible Replacement for MAX8863/8864.
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