AN723

Operational Amplifier AC Specifications and Applications

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INTRODUCTION

This application note defines the ac specifications of voltage feedback operational amplifiers (Op Amps). Directly following these definitions, related amplifier circuits are given where the ramifications of the particular specifications causes less than optimum circuit performance. This is then followed with appropriate circuit solutions.The companion application note for DC specifications along with various application circuits is titled "Operational Amplifier Topologies and DC Specifications", AN-722 and available on Microchip's web site.

The performance specifications discussed in this application note are separated into the two categories listed below.

Frequency Domain Specifications

- Gain Bandwidth Product (GBWP)
- Open Loop Gain/Phase (A_{OL},PH)
- Load Capacitance (C_L) - Output Impedance (Z_O)
- Full Power Bandwidth (FPBW)

Time Domain Specifications

- Slew Rate (SR)
- Settling Time (t_S)
- Overshoot

Topics such as bode plot generation, bode plot translation, stability analysis and feedback theory are discussed throughout this application note.

Additionally, there are numerous ac performance aspects of an operational amplifier that can be described from the frequency domain perspective or the time domain perspective. For instance, amplifier stability can be described in the frequency domain with the closed loop phase margin and its relationship to the amplifier open loop gain. In the time domain, the phase margin, in degrees, can be directly mapped to the settling time, and overshoot. Where appropriate, discussions in this application note will establish the correlation between these two domains.

The ac op amp open loop model that will be referred throughout this discussion is shown in Figure 1.

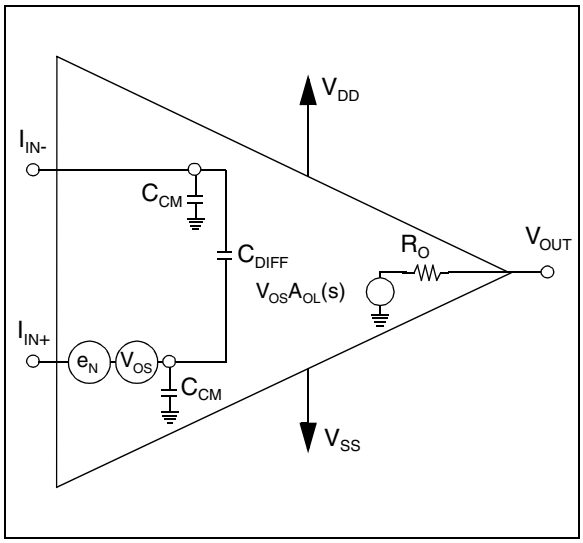

FIGURE 1: *Voltage Feedback Operational Amplifier frequency model.*

In this figure, the amplifier is shown with five terminals. The two input terminals have an offset voltage error (V_{OS}), a noise source (e_N) and differential capacitance (C_{DIFF}). The finite impedance of the output terminal is modeled using R_O. The amplifier's open loop gain over frequency is represented by the term $A_{OL}(j\omega)$. This gain term can be described in simple terms with the 2nd order transfer function:

$$A_{OL}(j\omega) = \frac{A_{OL}(DC)}{(as+1)(bs+1)}$$

Where:

a = the location of the dominant pole and

b = the location of the second pole

FREQUENCY DOMAIN SPECIFICATIONS

Bode Plot Analysis Method

The bode plot is a tool that is used to approximate the magnitude and phase of a transfer function. An example of the op amp gain and phase bode plots are shown in Figure 2.

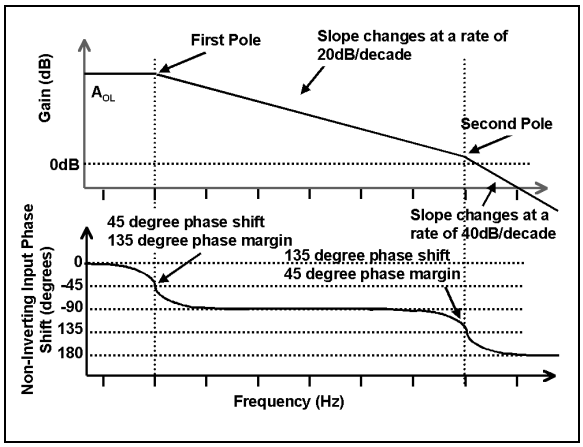

FIGURE 2: *The frequency response of an analog system can be characterized with a bode plot. The bode plot graphically describes gain and phase of the system.*

These two plots illustrate the gain (top) and phase response (bottom) of a typical op amp. The units of the y-axis of the gain curve are decibels (dB). Decibels can be translated to volts with the formula:

$$A_{OL}(j\omega) \text{ in dB} = 20 \log\left(\frac{V_{OUT}(j\omega)}{V_{IN}(j\omega)}\right)$$

The units of the y-axis of the phase plot is in degrees.

Degrees can be converted to radians with the formula:

Phase in radians = (Phase in degrees) / 2π

Phase in degrees can be translated to phase delay or group delay (seconds), with the formula:

Phase delay = (δphase in degrees/ δf)/360

Both plots are aligned on the same frequency scale with their respective x-axis.

Gain Bandwidth Product (GBWP)

Specification Discussion - The Gain Bandwidth Product (GBWP) of an amplifier is the product of the amplifier open loop gain times the frequency at any point in the frequency range where the amplifier response is attenuating at a rate of -20dB per decade of frequency.

By definition, if an amplifier is unity gain stable, it does not oscillate when the non-inverting input is used for the signal input and the inverting input is connected directly to the output. The unity gain bandwidth of the amplifier is equivalent to the amplifier's GBWP. The fact that an amplifier is unity gain stable implies that the phase shift from the non-inverting input to output is between zero and -180 degrees at the zero dB crossing of the open loop gain curve. Some amplifiers are not unity gain stable, in which case, the open loop gain zero crossing frequency is less than the GBWP.

Application Challenge - An amplifier configured as a buffer is shown in Figure 3. In this circuit, the buffer is used to electrically isolate conflicting impedances or to thermally isolate heavy loads. In this application, the amplifier selected must be unity gain stable.

A good stability test for a buffer is to apply a square wave to the input of the amplifier. The overshoot and ringing at the output of the amplifier will directly reflect the phase shift at the frequency where the gain is down 3dB.

For example, the bode plot of an amplifier that is not unity gain stable is shown in Figure 4. When this amplifier is configured as a buffer, the step response will show that the amplifier has a tendency to oscillate (Figure 5). The only remedy to this application problem is to select an amplifier that is unity gain stable. This is shown with the response of a second amplifier whose bode plot response is shown in Figure 6 and step response is shown in Figure 7.

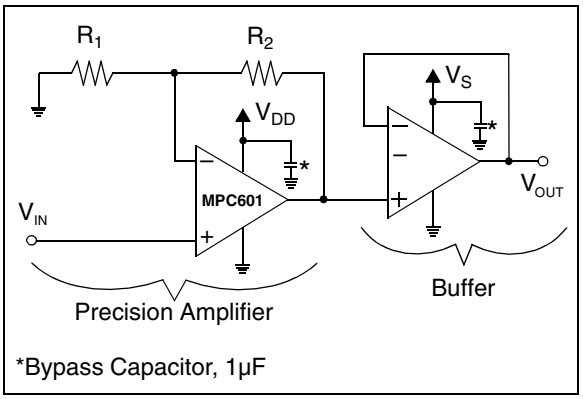

FIGURE 3: *A typical application for an amplifier is the voltage buffer or follower.*

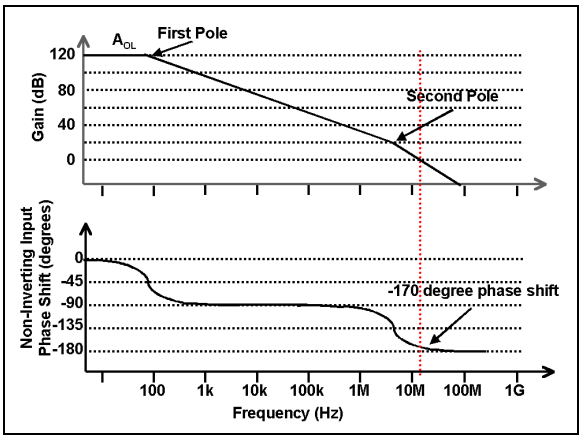

FIGURE 4: *A bode plot of an amplifier that is not unity gain stable. This condition exists because the phase at the zero dB crossing frequency is nearly -180 degrees.*

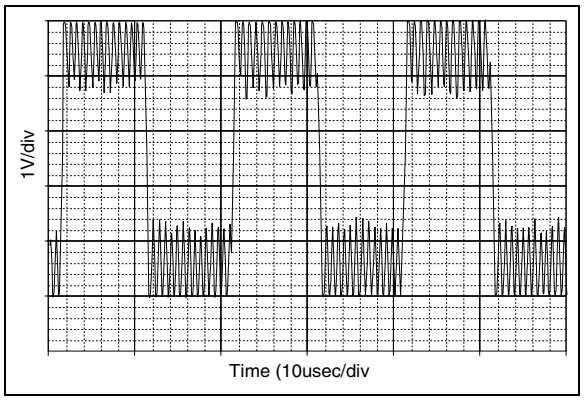

FIGURE 5: *The unity gain step response of the amplifier specified with the bode plot of Figure 4 demonstrates the instability of the amplifier.*

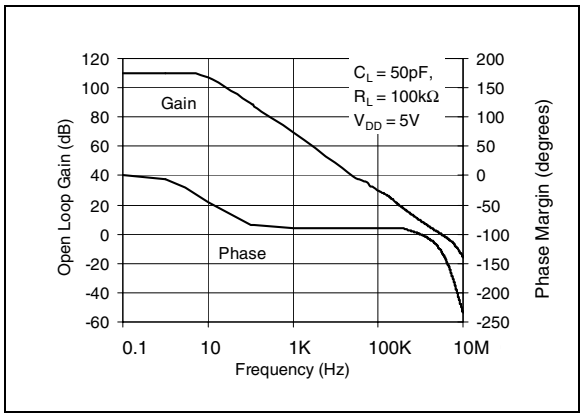

FIGURE 6: *Bode plot of the MCP601 unity gain amplifier.*

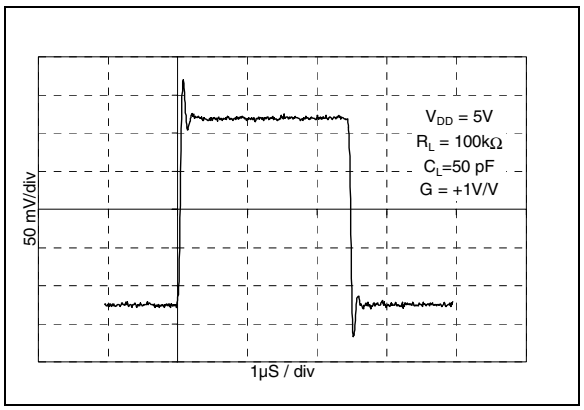

FIGURE 7: *Step response of the unity gain stable MCP601 amplifier.*

Open Loop Gain/Phase (A_{OL}, PH)

Specification Discussion - Ideally, the open loop gain of an amplifier is equal to the absolute value of the ratio of the voltage at the output terminal divided by the difference of the voltages applied between the two input terminals.

$$A_{OL}(dB) = 20\ log\left(\frac{V_{OUT}}{V_{IN+} - V_{IN-}}\right)$$

It would be ideal if the open loop gain ratio were infinite, but in reality, the complete frequency response of the open loop gain, $A_{OL}(j\omega)$, is less than ideal at DC and attenuates at a rate of 20dB/decade beginning at the frequency where the first pole in the transfer function appears. This is illustrated in the bode plot in Figure 2.

Usually, the first pole of the open loop response of an operational amplifier occurs between 1Hz to 10kHz. The second pole occurs at a higher frequency, nearer to the frequency where the open loop gain curve crosses 0dB. The gain response of an amplifier starts to fall off at 40dB/decade at the frequency where the second pole occurs.

The phase response of an amplifier in this open loop configuration is also fairly predictable. The phase shift or change from the non-inverting input to the output of the amplifier is zero degrees at DC. Conversely, the phase from the inverting input terminal to the output is equal to -180 degrees at DC.

At one decade (1/10 f_1) before the first pole, f_1, the phase relationship of non-inverting input to output has already started to fall (~ -5.7 degrees). At the frequency where the first pole appears in the open loop gain curve (f_1), the phase has dropped to -45 degrees. The resultant phase continues to drop for another decade ($10f_1$) where it is 5.7 degrees above its final value of -90 degrees. This phase response discussion can be repeated for the second pole, f_2.

What is important to understand is the ramifications of the changes in this phase relationship of the input to output of the amplifier. One frequency decade past the second pole, the phase shift of the non-inverting input is -180 degrees. At this same frequency, the phase shift of the inverting input to output is zero or -360 degrees. With this type of shift, V_{IN+} is actually inverting the signal to the output. In other words, the role of the two inputs have reversed.

Stability in Closed Loop Amplifier Systems

Typically, op amps are used with a feedback network in order to reduce the variability of the open loop gain response from part to part. A block diagram of this type of network is shown in Figure 8.

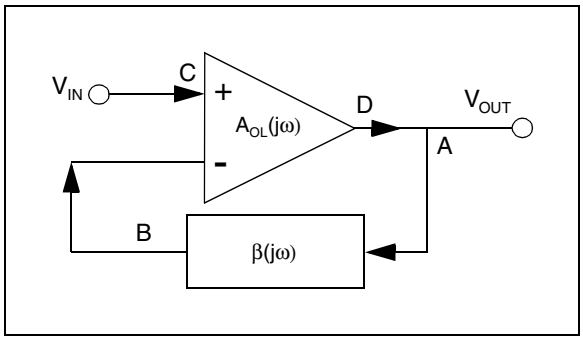

FIGURE 8: *A block diagram of an amplifier circuit which includes the amplifier gain cell, A_{OL}, and the feedback network, β.*

In Figure 8, β represents the feedback factor. Due to the fact that the open loop gain of the amplifier (A_{OL}) is relatively large, a fraction of the output voltage is fed back to the inverted input of the amplifier. If β were fed back to the non-inverting terminal, this small fraction of the output voltage would be added instead of subtracted. This configuration is appropriately called positive feedback and the output would eventually saturate.

The job of the feedback factor in this network is to reduce part-to-part variations in the system. However, if care is not taken, the feedback network can introduce unwanted frequency oscillations. This circumstance exists if the feedback factor is fed into the input of the system as a positive entity.

Closed Loop Transfer Function - The loop in Figure 8 can be analyzed by assuming an output voltage exists making the voltage at "A" equal to $V_{OUT}(j\omega)$. The signal passes through the feedback system, $\beta(j\omega)$, so that the voltage at "B" is equal to $\beta(j\omega)V_{OUT}(j\omega)$. This voltage is then summed to the input voltage which equates the voltage at "C". "C" is equal to $(V_{IN}(j\omega) - \beta(j\omega)V_{OUT}(j\omega))$. With the signal passing through the gain cell, $A_{OL}(j\omega)$, the voltage at point "D" is equal to $A_{OL}(j\omega)(V_{IN}(j\omega) - \beta(j\omega)V_{OUT}(j\omega))$. It should be noted that this voltage is equal to the original node, "A", or V_{OUT}. The formula that describes this complete closed loop system is equal to:

"A" = "D" or

$$V_{OUT}(j\omega) = A_{OL}(j\omega)(V_{IN}(j\omega) - \beta(j\omega)V_{OUT}(j\omega))$$

By collecting the terms, the manipulated transfer function becomes:

$$\frac{V_{OUT}(j\omega)}{V_{IN}(j\omega)} = \frac{A_{OL}(j\omega)}{(1 + A_{OL}(j\omega)\beta(j\omega))}$$

This formula is essentially equal to the closed loop gain of the system, or $A_{CL}(j\omega)$.

This is a very important result. If the open loop gain ($A_{OL}(j\omega)$) of amplifier is allowed to approach infinity, the response of the feedback factor can easily be evaluated as:

$$A_{CL}(j\omega) = \frac{1}{\beta(j\omega)}$$

This formula allows an easy determination of the frequency stability of an amplifier's closed loop system.

Calculation of 1/β - The easiest technique that can be used to calculate 1/β is to place a source directly on the non-inverting input of the amplifier. One could argue that this calculation will not give the appropriate circuit closed loop gain equation for the actual signal and this is true. But this calculation can be used to ascertain the level of circuit stability.

The circuits in Figure 9 are used to show how to calculate 1/β.

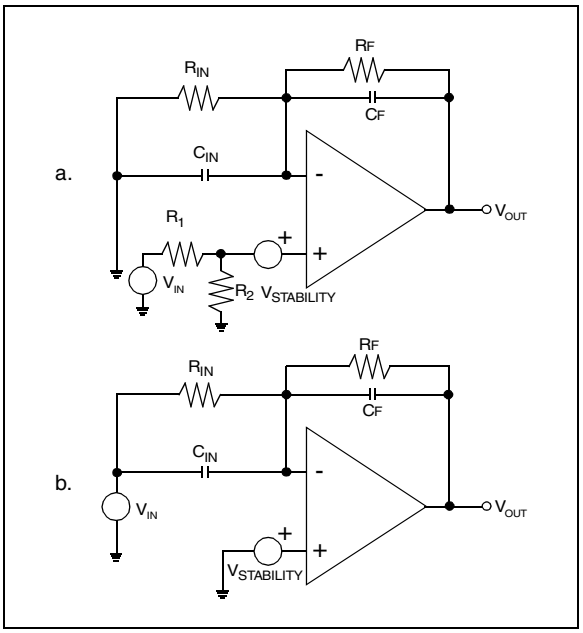

FIGURE 9: *The input signal in circuit 9a. at DC will be gained by $(R_2/(R_1+R_2)(1+R_F/R_{IN})$. The input signal in circuit 9b. has a DC gain of $-R_F/R_{IN}$. Neither of these gain equations match the DC gain of the feedback factor, 1/β*

In Figure 9a., the fictituos voltage source, $V_{STABILITY}$, is used for the 1/β stability analysis calculation. Note that this source is not the actual application input source.

Assuming that the open loop gain of the amplifier is infinite, the transfer function of this circuit is equal to:

$$\frac{V_{OUT}}{V_{STABILITY}} = \frac{1}{\beta}$$

$$\frac{1}{\beta} = 1 + \frac{R_F \| C_F}{R_{IN} \| C_{IN}}$$

$$\frac{1}{\beta(j\omega)} = \frac{(R_{IN}((j\omega)R_FC_F + 1) + R_F((j\omega)R_{IN}C_{IN} + 1))}{R_{IN}((j\omega)R_FC_F + 1)}$$

or

In this equation above, when ω is equal to zero:

$$\frac{1}{\beta(j\omega)} = 1 + \frac{R_F}{R_{IN}}$$

As ω approaches infinity,

$$\frac{1}{\beta(j\omega)} = 1 + \frac{C_{IN}}{C_F}$$

The transfer function has one zero and one pole. The zero is located at:

$$f_z = \frac{1}{(2\pi R_{IN} \parallel R_F(C_{IN} + C_F))}$$

$$f_p = \frac{1}{2\pi R_F C_F}$$

The bode plot for the 1/β(jω) transfer function of the circuit in Figure 9a. is shown in Figure 10.

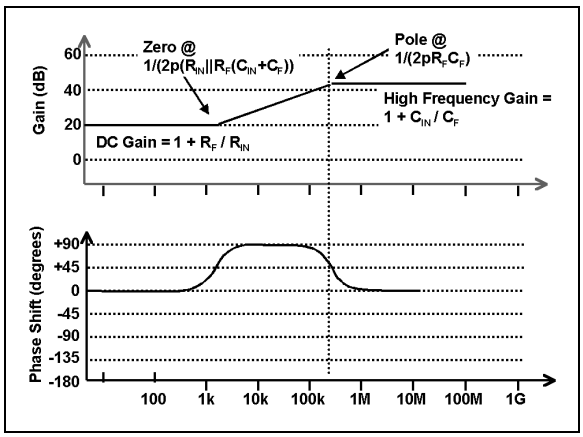

FIGURE 10: *These are the bode plots of the inverse of the feedback factor (1/β) for circuit in Figure 9a. using $V_{STABILITY}$ as the input source.*

Once again, in Figure 9b, the input source that is used for this analysis is not the same as the input source for the actual application circuit. However, the amplifier stability is determined in the same manner. The closed loop transfer function, using $V_{STABILITY}$ is equal to:

$$\frac{V_{OUT}}{V_{STABILITY}} = \frac{1}{\beta}$$

$$\frac{1}{\beta} = 1 + \frac{R_F \parallel C_F}{R_{IN} \parallel C_{IN}}$$

or

$$\frac{1}{\beta(j\omega)} = \frac{(R_{IN}((j\omega)R_FC_F + 1) + R_F((j\omega)R_{IN}C_{IN} + 1))}{R_{IN}((j\omega)R_FC_F + 1)}$$

Note that the transfer functions of 1/β between Figure 9a. and Figure 9b.are identical.

Determining System Stability - In a closed loop amplifier system, stability can be determined if the phase margin of the system is known. In this analysis, the Bode stability analysis technique is commonly used. With this technique, the magnitude (in dB) and phase response of both the open loop response of the amplifier and circuit feedback factor are included in a Bode plot.

The system closed loop gain is equal to the lesser (in magnitude) of the two gains. The phase response of the system is the equal to the open loop gain phase shift minus the inverted feedback factor's phase shift.

The stability of the system is defined at the frequency where the open loop gain of the amplifier intecepts the closed loop gain response. At this point, the theoretical phase shift of the system should be greater than -180 degrees. In practice, the system phase response should be larger than -135 degrees. This technique is illustrated in Figures 11 through 14. The cases presented in Figure 11 and Figure 12 represent stable systems. The cases presented in Figure 13 and 14 represent unstable systems.

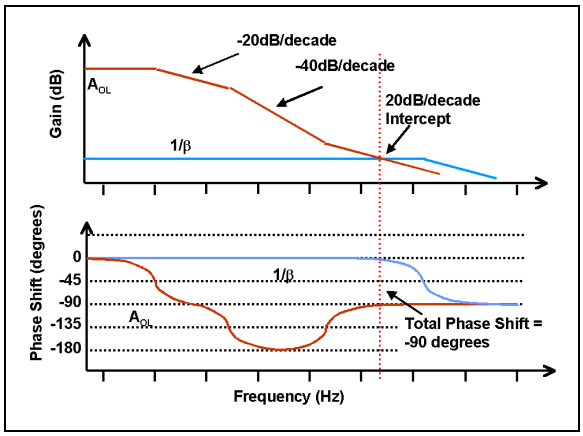

FIGURE 11: *This closed loop system is stable with a phase shift of -90 degrees at the intecept of the A_{OL} and 1/β curves.*

In Figure 11, the open loop gain of the amplifier ($A_{OL}(j\omega)$) starts with a zero dB change in frequency and quickly changes to a –20dB/decade slope. At the frequency where the first pole occurs, the phase shift is –45 degrees. At the frequency one decade above the first pole, the phase shift is approximately –90 degrees. As the gain slope progresses with frequency, a second pole is introduced causing the open loop gain response to change –40dB/decade. Once again, this is accompanied with a phase change. The third incident that occurs in this response is where a zero is introduced and the open loop gain response returns back to a –20dB/decade slope.

The 1/β curve in this same graph starts with a zero dB change with frequency. 1/β remains flat with increased frequency until the very end of the curve where a pole occurs and the curve starts to attenuate –20dB/decade.

The point of interest in this graph is where the $A_{OL}(j\omega)$ curve intersects the 1/β curve. The rate of closure of 20dB/decade between the two curves suggests the phase margin of the system and in turn predicts the stability. In this situation, the amplifier is contributing a -90 degree phase shift and the feedback factor is contributing a zero degree phase shift. The phase shift and consequently the stability of the system is determined at this intersection point. The system phase shift is calculated by subtracting the $1/\beta(j\omega)$ phase shift from the $A_{OL}(j\omega)$ phase shift. In this case, the system phase shift is -90 degrees. Theoretically, a system is stable if the phase shift is between zero and -180 degrees.

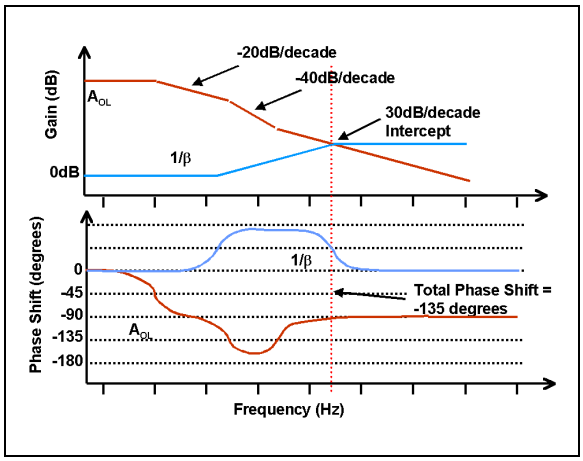

FIGURE 12: *This system is marginally stable with a -135 degree phase shift at the intersection of the two gain curves.*

In the case presented in Figure 12, the point of intersection between the $A_{OL}(j\omega)$ curve and the $1/\beta(j\omega)$ curve suggests a marginally stable system. At that point, the $A_{OL}(j\omega)$ curve is changing –20dB/decade. The $1/\beta(j\omega)$ curve is changing from a +20dB/decade to a 0dB/decade slope. The phase shift of the $A_{OL}(j\omega)$ curve is -90 degrees. The phase shift of the $1/\beta(j\omega)$ curve is +45 degrees. The system phase shift is equal to -135 degrees.

Although this system appears to be stable, i.e. the phase shift is between zero and -180 degrees, circuit implementation will not be as clean as calculations or simulations would imply. Parasitic capacitance and inductance on the board can contribute additional phase errors. Consequently, this system is deemed “marginally stable” with this magnitude of phase shift. This closed loop circuit will be shown to have significant overshoot and ringing in the Time Response discussion.

In Figure 13, the $A_{OL}(j\omega)$ is changing at a rate of –20dB/decade. The $1/\beta(j\omega)$ is changing at a rate of +20dB/decade. The rate of closure of these two curves is 40dB/decade and the system phase shift is -168 degrees. The stability of this system is very questionable.

In Figure 14, $A_{OL}(j\omega)$ is changing at a rate of –40dB/decade. The $1/\beta(j\omega)$ is changing at a rate of 0dB/decade. The rate of closure of these two curves is 40dB/decade indicating a phase shift of -170 degrees. The stability of this system is also questionable.

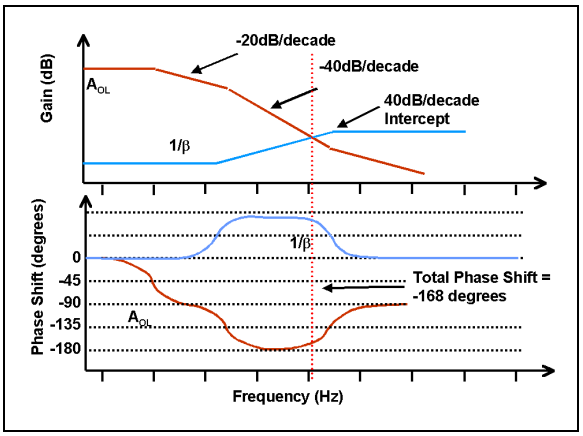

FIGURE 13: *In a practical circuit implementation, given layout parasitics, this system is unstable.*

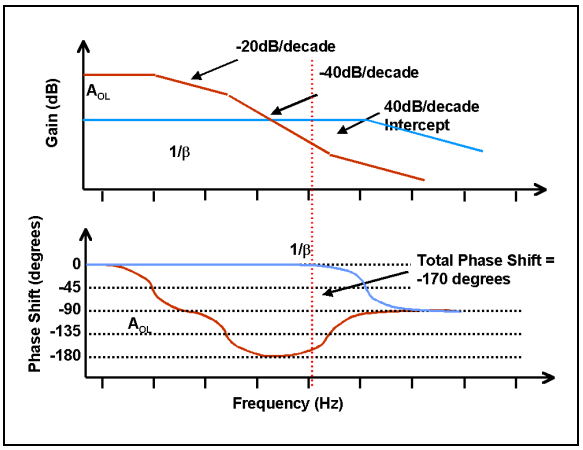

FIGURE 14: *In a practical circuit implementation, given layout parasitics, this system is also unstable.*

Load Capacitance (C_L) - Output Impedance (Z_O)

A primary application for amplifiers is to separate or isolate a signal source from a load. Sometimes the loads that need to be isolated are fundamentally resistive. In other cases, the load is pure capacitive. The third scenario is where the amplifier has an R/C load. An example of an amplifier circuit that has a resistive and capacitive load is shown in Figure 15. The critical

specification that effects the stability of this system is the open loop output impedance of the amplifier, R_O and the open loop phase response.

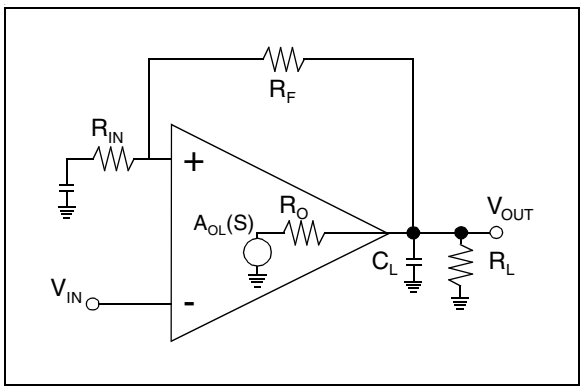

FIGURE 15: *Any load on an amplifier may effect the performance of the closed loop circuit. In the case of capacitive loads, the frequency stability can also be compromised.*

When the output impedance of the amplifier is considered in this closed loop system, the effective open-loop gain of the amplifier is changed to:

$$A_{OL}'(j\omega) = A_{OL}(j\omega)\left(\frac{R_P}{R_P + R_O}\right)\left(\frac{1}{1 + R_X C_L(j\omega)}\right)$$

Where:

$R_P = R_F // R_L$ *and*

$R_X = R_O // R_F // R_L$

Application Challenge - Even though an amplifier is unity gain stable, a capacitive load may make the system unstable.

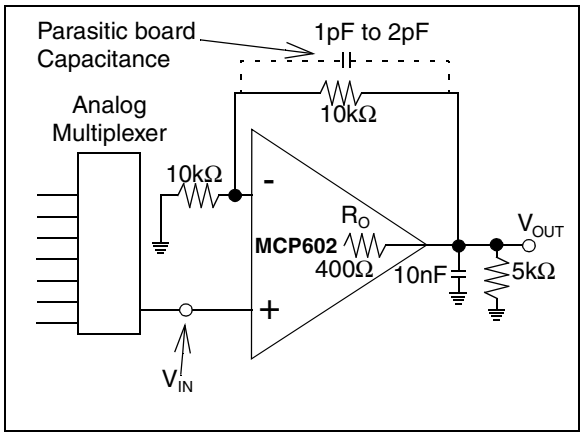

FIGURE 16: *This amplifier configuration is potentially unstable because of the low closed loop gain and high capacitive load.*

An example where a unity gain stable amplifier can be made unstable is shown in Figure 16. The open loop output resistance is 400Ω. Using the formulas of R_P and R_X above:

$R_P = 10k\Omega // 10k\Omega = 2.5k\Omega$

$R_X = 400\Omega // 10k\Omega // 5k\Omega = 357\Omega$

The bode plot for the modified open loop (A_{OL}') gain and phase curves are shown in Figure 17, along with the actual A_{OL} plots of the amplifier.

The feedback transfer function is:

$1/\beta = 1 + 10k\Omega / 10k\Omega$

The bode plot of 1/β is also shown in Figure 17.

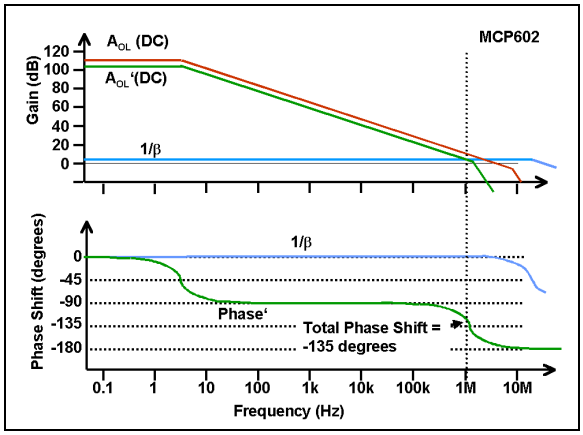

FIGURE 17: *Capacitive loads on amplifiers degrade the system stability. This bode plot demonstrates the effects of the load illustrated in Figure 16.*

From this simple calculation, the circuit is shown to be very marginal in terms of instability. Any parasitic board capacitance will simply aggravate the condition.

Capacitive loading can be corrected by implementing the circuit shown in Figure 18.

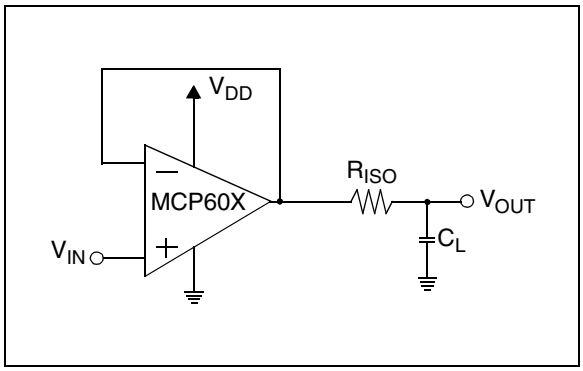

FIGURE 18: *In most cases, the addition of a resistor, R_{ISC}, between the output of the amplifier and the capacitive load will eliminate any unwanted oscillation.*

Full Power Bandwidth

Specification Discussion - The Full Power Bandwidth (FPBW) of an amplifier is the maximum frequency that the output of an amplifier can swing over the full dynamic range without significant distortion. At lower frequencies, the FPBW is limited by the output swing of the amplifier. At higher frequencies, the response is limited by the slew rate of the amplifier. The definition of slew rate is given under the Time Domain specifications later on in this application note. Distortion due to slew limiting of the amplifier starts to occur at the point where the sine wave is at its highest dV/dt or half way between the peak-to-peak values. By equating the maximum slope of a sine wave to the slew rate of the amplifier at higher frequencies, the full power response equals:

$$f_{FP} = \frac{SR}{\pi Vp-p}$$

The FPBW of the MCP601, CMOS amplifier is shown in Figure 20.

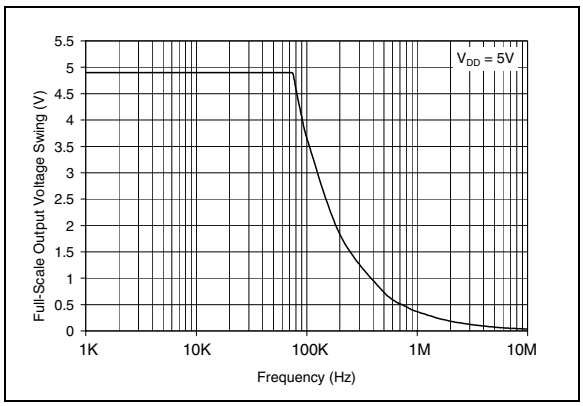

FIGURE 19: *The MCP601 Full Power Bandwidth.*

Application Challenge - In an A/D Converter application, the input to the A/D Converter is typically driven by an amplifier. It may be tempting to select an amplifier based on the unity gain bandwidth, however, if the application demands that the full dynamic range of the A/D converter is used, the bandwidth of the amplifier under these conditions is much less than the unity gain bandwidth. This type of circuit is shown in Figure 20, where the single supply MCP601 op amp is used to drive the 12-bit MCP3201 A/D converter. As shown in Figure 19, the FPBW of the MCP601 is 80kHz. In contrast, the unity gain bandwidth (which is a small signal specification) is typically 2.8MHz.

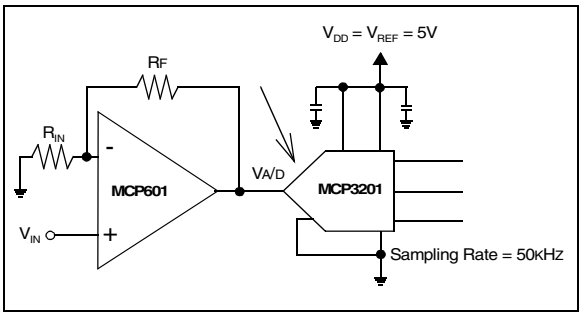

FIGURE 20: *The MCP601 is used to driving the MCP3201, 12-bit A/D converter.*

If the sampling frequency of the MCP3201 is 50kHz, the amplifier in this circuit must be able to drive a full scale signal a 1/2 of nyquist or 25kHz at the $V_{A/D}$ node shown in Figure 21. The MCP601 is fully capable of meeting this performance requirement with a FPBW that exceeds 25kHz by more than three times.

TIME DOMAIN SPECIFICATIONS

The time domain responses of amplifier circuits provide a real world result of the previous frequency discussions. The graphical definition of time domain specifications is shown in Figure 21. The waveform in this figure depicts the response of the output of the amplifier with regards to a step response at the input of the circuit. This figure will be referred to throughout the following discussion.

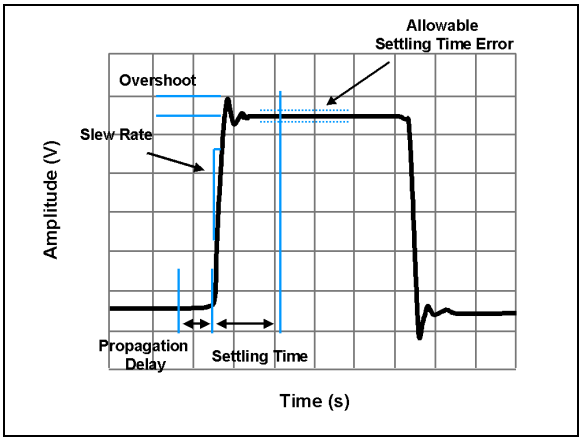

FIGURE 21: *The time domain step response behavior of an amplifier configured in a closed loop system can be described using the definitions diagrammed here.*

Slew Rate (SR)

Specification Discussion - The Slew Rate (SR) specification for an amplifier quantifies the speed at which the output terminal can execute a full scale output voltage swing that is driven at the input of the amplifier. This specification is controlled internally by the amplifier and dependent on the amount of tail current available to charge and discharge internal capacitors. The units of

this specification are in volts per second. Slew rate is measured from 10% to 90% at the output of the amplifier through the full scale voltage swing. The most challenging amplifier circuit for this type of specification is the buffer or follower configuration, as shown in Figure 22. In this configuration, the input terminals are pulled out of their nonlinear region by virtue of the fact that the inverting input terminal is connected directly to the slow moving output terminal.

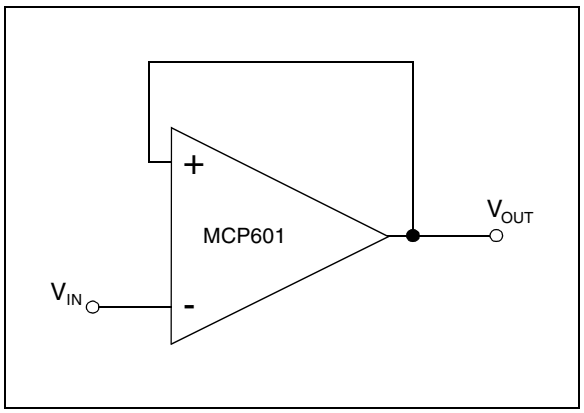

FIGURE 22: *The most challenging test condition for slew rate is the buffer configuration that is shown here.*

Settling Time (t_s) and Overshoot

At the top or bottom of the full-scale slew transition, a degree of ringing occurs. This ringing is directly related to the phase shift of the closed loop system and described in terms of overshoot and the amount of time before the signal to settle within a specified error band. The % overshoot is defined at the highest peak in this portion of the waveform, which occurs at the beginning of the ringing of the system. The magnitude of the system overshoot and the amount of time required for the system to settle is directly related to the frequency domain phase shift of the system.

The Settling Time (t_s) of an amplifier circuit is defined as the amount of time that is required for the output of the amplifier to slew and then settle within a defined error band. This time starts at the point where the output first responds to the input excitation until the last occurrence of the output signal being outside the error band, as illustrated in Figure 21.

Application Challenge - A t_s error is most noticeable in applications where the common mode input of the amplifier has a full scale step response applied. In this situation, the amplifier goes into a full slew rate condition (SR) and then settles to its final value (t_s). For this example, the circuit shown in Figure 16 is integrated into the circuit shown in Figure 23. Even though the system signals are slow moving, the multiplexer in this circuit presents a step response to the amplifier. The step response of this amplifier system is shown in Figure 24.

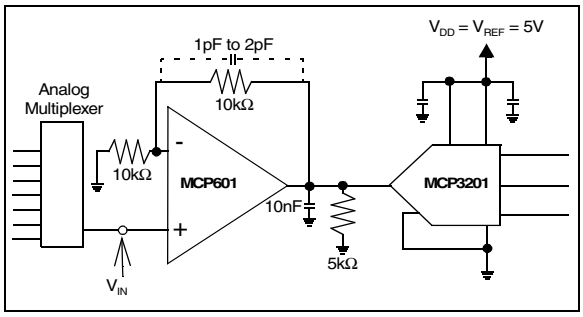

FIGURE 23: *The driver configuration shown in Figure 16 is used in this multiplexing circuit. This driver circuit does not make the system unstable, however, the A/D converter conversion should be delayed while the op amp circuit is settling to final value.*

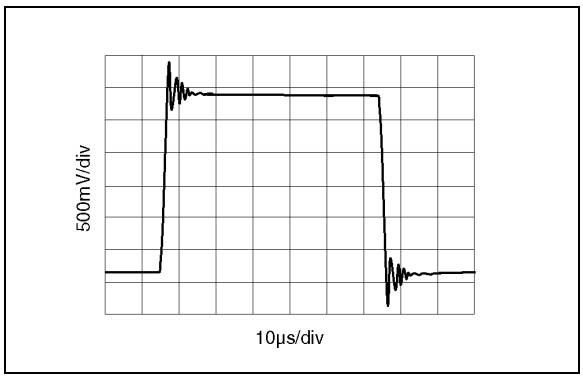

FIGURE 24: *The phase shift of an amplifier in a closed loop system is reflected in the step response in terms of overshoot (15%) and ringing.*

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