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System Level Design Considerations When Using I²C™ Serial EEPROM Devices

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INTRODUCTION

Developing systems that implement the I²C protocol for communicating with serial EEPROM devices requires that a certain key factors be considered during the hardware and software development phase if the system is to achieve maximum compatibility and robustness. This application note discusses these factors, both hardware and software, to help insure that an optimal system design is achieved. This application note is limited to single master systems and therefore does not specifically address the unique requirements of a multi-master system. However, the concepts presented in this application note apply equally as well to those systems.

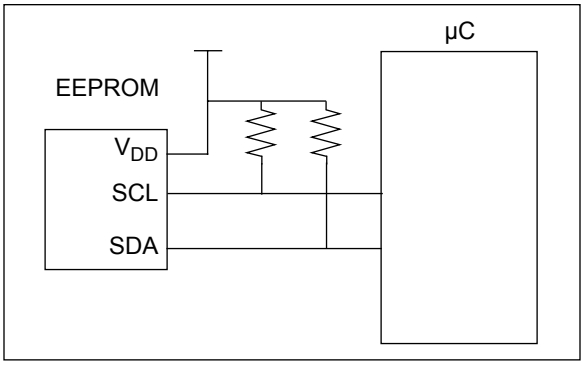
CONDITIONS TO BE CONSIDERED

Due to the bi-directional nature of the data bus devices operate in both transmit and receive modes at various times. In order to make this bi-directional operation possible the protocol must define specific times at which any given device may transmit or receive, as well as define specific points in the protocol where the functions are swapped (i.e. the transmitter becomes the receiver and the receiver becomes the transmitter). There are a number of events which could potentially cause this sender/receiver 'synchronization' to be lost, which can result in situations where:

- Both the master and the slave are in a send mode.
- Both the master and the slave are in a receive mode.
- The 'bit count' is off by one or more bits between the master and the slave.

These events, which include the microcontroller being reset during I²C communication, brown-out conditions, excessive noise on the clock or data lines, and improper bus input levels during power up, can be effectively neutralized through a combination of hardware and software techniques.

FIGURE 1: RECOMMENDED HARDWARE CONFIGURATION



INSURING 'BUS-FREE' DURING POWER-UP

In order to insure that the internal state machine of the serial EEPROM is correctly initialized at power up, it is crucial to guarantee that the device sees a 'bus-free' condition (defined as both SCL and SDA being high) until $V_{DD_{min}}$ has been reached. The ideal way to guarantee this is through the use of pull-up resistors on both the SDA and SCL lines. In addition, these pull-ups should be tied to the same voltage source as the VDD pin of the device. In other words is the device VDD is supplied from the main positive supply rail then the SCL and SDA pull-ups should be connected to that same supply rail (as opposed to being connected to a microcontroller I/O pin, for example). Figure 1 is an example of the recommended hardware configuration. The reasoning behind doing this is the same for both adding the pull-up to the SCL line and for utilizing the same supply for the VDD pin and the pull-ups. As anyone who has had any experience with CMOS logic already knows, it is necessary to ensure that all inputs are tied either high or low, since allowing a CMOS input to float can lead to a number of problems. If the SCL line does not have a pull-up, or if the pull-ups are not tied to the VDD supply rail, then conditions occur, however briefly, where the SCL/SDA inputs are floating with respect to the VDD supply voltage. When possible this condition should be avoided.

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When it is not possible to add a pullup resistor to the SCL line (i.e. the hardware design has already been finalized) then the firmware should be configured to either: 1) drive the SCL line high during power up or, 2) float the SCL input during power up.

Of these two options, the first is the recommended method, despite typical concerns regarding latch-up, because it does not negatively impact the battery life in battery powered applications. Microchip Technology's serial EEPROM devices, like all CMOS devices, are susceptible to latch-up, however latch-up does not occur until currents in excess of 100mA are injected into the pin. Typical microcontrollers are not capable of supply currents of this magnitude, therefore the risk of latch-up is extremely low.

The second option is also acceptable but does lead to a brief increase in the current draw of the device during the time period in which the SCL pin is floating with respect to V_{DD}. This increase can be significant in comparison to the normal standby current of the device and can have a detrimental affect on battery life in power sensitive applications.

In all cases it is important that the SCL and SDA lines not be actively held low while the EEPROM device is powered up. This can have an indeterminable effect on the internal state machine and, in some cases, the state machine may fail to correctly initialize and the EEPROM will power up in an incorrect state.

Another improper practice which should be pointed out is the driving of the SDA line high by the microcontroller pin rather than tri-stating the pin and allowing the requisite pullup resistor to pull the bus up to the high state. While this practice would appear harmless enough, and indeed it is as long as the microcontroller and EEPROM device never get out of sync, there is a potential for a high current situation to occur. In the event that the microcontroller and EEPROM should get out of sync, and the EEPROM is outputting a 'low' (i.e. sending an ACK or driving a data bit of '0') while the microcontroller is driving a high then a low impedance path between V_{DD} and V_{SS} is created and excessive current will flow out of the microcontroller I/O pin and into the EEPROM SDA pin. The amount of current that flows is limited only by the IOL specification of the microcontoller's I/O pin. This high current state can obviously have a very detrimental effect on battery life, as well as potentially present long term reliability problems associated with the excess current flow.

FORCING INTERNAL RESET VIA SOFTWARE

In all designs it is recommended that a software reset sequence be sent to the EEPROM as part of the microcontrollers power up sequence. This sequence guarantees that the EEPROM is in a correct and known state. Assuming that the EEPROM has powered up into an incorrect state (or that a reset occurred at the microcontroller during communication), the following sequence (which is further explained below) should be sent in order to guarantee that the serial EEPROM device is properly reset:

- START Bit
- Clock in nine bits of '1'
- START Bit
- STOP Bit

The first START bit will cause the device to reset from a state in which it is expecting to receive data from the microcontroller. In this mode the device is monitoring the data bus in receive mode and can detect the START bit which forces an internal reset.

The nine bits of '1' are used to force a reset of those devices that could not be reset by the previous START bit. This occurs only if the device is in a mode where it is either driving an acknowledge on the bus (low), or is in an output mode and is driving a data bit of '0' out on the bus. In both of these cases the previous START bit (defined as SDA going low while SCL is high) could not be generated due to the device holding the bus low. By sending nine bits of '1' it is guaranteed that the device will see a NACK (microcontroller does not drive the bus low to acknowledge data sent by EEPROM) which also forces an internal reset.

The second START bit is sent to guard against the rare possibility of an erroneous write that could occur if the microcontroller was reset while sending a write command to the EEPROM, and, the EEPROM was driving an ACK on the bus when the first START bit was sent. In this special case if this second START bit was not sent, and instead the STOP bit was sent, the device could initiate a write cycle. This potential for an erroneous write occurs only in the event of the microcontroller being reset while sending a write command to the EEPROM.

The final STOP bit terminates bus activity and puts the EEPROM in standby mode.

This sequence does not effect any other I^2C devices which may be on the bus as they will simply disregard it as an invalid command.

SUMMARY

This application note has presented ideas that are fundamental in nature, yet not always obvious, to the utilization of I^2C serial EEPROM devices. Ideally the hardware/software engineer(s) takes these ideas into consideration during system development and design accordingly. It is recommended that the software reset sequence detailed in this application note be added to the system initilization code of any system that utilizes an I^2C serial EEPROM device.

REFERENCES

'I^2C-Bus Specification', Philips Semiconductors, January 1992

'The I^2C-Bus and How to Use It', Philips Semiconductors, April 1995

NOTES:

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