

AN695

Interfacing Pressure Sensors to Microchip's Analog Peripherals

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INTRODUCTION

Pressure measurement devices can be classified into two groups: those where pressure is the only source of power and those that require electrical excitation. The mechanical style devices that are only excited by pressure, such as bellows, diaphragms, bourdons, tubes or manometers, are usually suitable for purely mechanical systems. With these devices a change in pressure will initiate a mechanical reaction, such as a change in the position of mechanical arm or the level of liquid in a tube.

Electrically excited pressure sensors are most synergistic with the microcontroller environment. These style of sensors can be piezoresistive, Linear Variable Differential Transformers (LVDT), or capacitive sensors. Most typically, the piezoresistive sensor is used when measuring pressure. This application note will concentrate on the signal conditioning path of the piezoresistive sensing element from sensor to microcontroller. It will show how the electrical output of this sensor can be gained, filtered and digitized in order to ready it for the microcontroller's calibration routines. This theoretical discussion will be followed with a specific pressure sensing design that is specifically designed to measure barometric pressure.

PIEZORESISTIVE PRESSURE SENSORS

The piezoresistive is a solid state, monolithic sensor that is fabricated using silicon processing. Piezo means pressure, resistance means opposition to a DC current flow. Since piezoresistive pressure sensors are fabricated on a wafer, 300 to 500 sensors can be produced per wafer. Since these wafers generate a large number of sensors they are available on the market at a reduced cost as compared to mechanical sensors.



Figure 1: The resistive wheatstone bridge configuration can have one variable element (a.), two elements that vary with excitation (b.) or four elements (c.). The piezoresistive pressure sensing element is usually a four element bridge and is constructed in silicon (d.).

With this sensor, the resistors are arranged in a full wheatstone bridge configuration, which has improved sensitivity as compared to a single element or two element sensors (see Figure 1.d). When a positive differential pressure is applied to the four element bridge, two of the elements respond by compressing and the other two change to a tension state. When a negative differential pressure is applied to the sensor, the diaphragm is strained in the opposite direction and the resistors that were compressed go into a tension state, while the resistors that were in a tension state change into a compression state. Piezoresistive pressure sensors may or may not have an internal pressure reference. If they do, a pressure reference cavity is generally fabricated by sealing two wafers together. The top side of this fabricated sensor is the resistive material and the bottom is the diaphragm.

The high side of the piezoresistive bridges shown in Figure 1 can have a voltage excitation or current excitation applied. Although the magnitude of excitation (whether it is voltage or current) effects the dynamic range of the output of the sensor, the maximum difference between V_{OUT+} and V_{OUT-} generally ranges from 10s of millivolts to several hundred millivolts. The electronics that follow the sensor are used to change the differential output signal to single ended as well as gain and filter it in preparation for digitization.

ELECTRONICS SIGNAL PATH

There are several ways of capturing the small differential output signal of the sensor and transforming it into a usable digital code. One approach that can be taken is shown in the block diagram in Figure 2.a. With this approach, the small differential output of the bridge is gained and converted from differential to single ended with an instrumentation amplifier (IA). The signal may or may not travel through a multiplexer. The signal then passes through a low pass filter. The low pass filter eliminates out-of-band noise and unwanted frequencies in the system before the A/D conversion is performed. This is followed by a stand-alone A/D converter which transforms the analog signal into a usable digital code. The microcontroller takes the converter code, further calibrates and translates if need be for display purposes. In this signal path only one analog filter is required and it is positioned at the output of the multiplexer.

The second signal path shown in Figure 2.b also has an instrumentation amplifier (IA) in the signal path. Following the instrumentation amplifier stage the signal is filtered in the analog domain and then digitized with an on-chip microcontroller's A/D converter. When this type of signal path is used, every signal going into the multiplexer will require its own analog filter. Additionally, the accuracy and speed of the converter in the microcontroller is less than a stand-alone A/D converter. This may or may not be an issue in a particular application.



Figure 2: Three block diagrams for the piezoresistive pressure sensor signal conditioning path are shown in this Figure. The top two block diagrams, a. and b., are discussed in detail in this application note. The bottom block diagram (c.) is discussed in detail in AN717 (Microchip Technology Inc.).

INSTRUMENTATION AMPLIFIER OPTIONS AND DESIGN

With this application, the two low voltage signals from the bridge need to be subtracted in order to produce a single ended output signal. The results of this subtraction also need to be gained so that it matches the input range of the A/D converter. The implementation of the subtraction and gain functions are done so that the sensor signal is not contaminated with additional errors. The instrumentation amplifier circuits shown in Figure 3 and Figure 4 achieve all of these goals. Both of these configurations take two opposing input signals, subtract them and apply gain. The subtraction process inherently rejects common-mode voltages. Combined with these functions the signal is level shifted, making it synergistic with the signal supply environment.

The Two Op Amp Instrumentation Amplifier

A solution to the circuit problem discussed above is shown in Figure 3. The circuit in Figure 3 uses two operational amplifiers and five resistors to solve this gain and subtraction problem.

Dual amplifiers are usually used in this discrete design because of their good matching of bandwidth and over temperature performance. This instrumentation amplifier design uses the high impedance inputs of the operational amplifiers, thereby significantly reducing source impedance mismatch problems at DC. The transfer function of this circuit is equal to:

$$\begin{split} V_{OUT} &= (V_{IN+} - V_{IN-}) \frac{R_4}{R_3} \Big(1 + \frac{1}{2} \Big(\frac{R_2}{R_1} + \frac{R_3}{R_4} \Big) \\ &+ \Big(\frac{R_2 + R_3}{R_6} \Big) \Big) + V_{CM} \Big(\frac{R_4}{R_3} \Big(\frac{R_3}{R_4} - \frac{R_2}{R_1} \Big) \Big) + V_{REF} \end{split}$$

It should be noted from this transfer function that the input signals are gained along with the common-mode voltage of the two signals. The common-mode voltage can be rejected when $R_1 = R_4$ and $R_2 = R_3$. Given this change the transfer function becomes:

$$V_{OUT} = (V_{IN+} - V_{IN-}) \left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G} \right) + V_{REF}$$

The common-mode rejection error that is caused by resistor mismatch is equal to:

$$CMR = 100^{*} \left(\frac{1 + \frac{R_2}{R_1}}{(\% \text{ of mismatch error})} \right)$$



Figure 3: The two op amp instrumentation amplifier takes the difference of two input signals, gains that difference, while rejecting any voltage that is common to both of the input signals.

The ac common mode rejection for this configuration is poor. This is due to the fact that the common mode signal at V_{IN-} is inverted once with A1 and then it travels through A2 causing a second propagation delay. The common mode signal at V_{IN+} only travels through one operational amplifier (A2). Additionally, the two operational amplifiers have different closed loop gains, and consequently different closed loop bandwidths.

In terms of common-mode input range, there are two factors that limit the range of this instrumentation amplifier. The first factor involves the operation of A1 as it responds to the V_{IN-} and V_{IN+} input signals and the voltage reference, V_{REF} . The signal at the non-inverting input to A1 and A2 gained by the output of A1 by:

$$V_{OUT-A1} = V_{IN-} \left(\frac{(R_G R_2 + R_1 R_2 + R_1 R_G)}{(R_1 R_2)} \right)$$
$$-V_{IN+} \left(\frac{R_2}{R_G} \right) - V_{REF} \left(\frac{R_2}{R_1} \right)$$

The second factor that limits the common-mode input range of this circuit comes from the input swing restrictions of the amplifiers themselves.

If this circuit is in a single supply environment, it will typically require a reference that is centered at the common-mode voltage of the input signals. In Figure 4, V_{REF} serves that function. This voltage can be implemented discretely with a precision reference chip as shown in Figure 4.a or with two equal resistors in series between the power supply as shown in Figure 4.b.

Another added benefit to matching $R_2/R_1 = R_3/R_4$ is that the gain of the circuit can be changed with one resistor, R_G .

This instrumentation amplifier circuit has high impedance inputs and programmable gain capability. The features that could be improved in this circuit solution is to have the common-mode rejection independent of gain and better over frequency. These performance characteristics can only be obtained by an instrumentation amplifier configuration that has three operational amplifiers.



Figure 4: The reference voltage for a two op amp instrumentation amplifier in a single supply environment can be implemented with a stand-alone voltage reference (a) or a resistor divider across a voltage reference or the supply voltage (b).

The Three Op Amp Instrumentation Amplifier

An example of a more versatile instrumentation amplifier configuration is shown in Figure 5.

With this circuit configuration, two of the three amplifiers (A1 and A2) gain the two input signals. The third amplifier, A3, is used to subtract the two gained input signals, thereby providing a single ended output. The transfer function of this circuit is equal to:

$$V_{OUT} = V_{IN+} \left(1 + \frac{2R_{F2}}{R_G} \right) R_4 \left(\frac{R_1 + R_2}{(R_3 + R_4)R_1} \right) - V_{IN-} \left(1 + \frac{2R_{F1}}{R_G} \right) \left(\frac{R_2}{R_1} \right) + V_{REF} R_3 \left(\frac{R_1 + R_2}{(R_3 + R_4)R_1} \right)$$

If $R_{F2} = R_{F1}$, $R_1 = R_3$, and $R_2 = R_4$, this formula can be simplified to equal:

$$V_{OUT} = (V_{IN+} - V_{IN-}) \left(1 + \frac{2R_F}{R_G} \right) + V_{REF}$$

Quad amplifiers are typically used in the three op-amp instrumentation amplifier discrete designs because of the matching qualities of amplifiers with the same silicon. In contrast to the two op-amp instrumentation amplifier, the input signal paths (at V_{IN+} and V_{IN-}) are completely balanced. This is achieved by sending V_{IN+} and V_{IN-} signals through the same number of amplifiers to the output and using a common gain resistor, R_G.

Since this input stage is balanced, common mode currents will not flow through R_G . The common-mode rejection of this circuit is primarily dependent on the resistor matching around A3. When $R_1 = R_2 = R_3 = R_4$, common mode signals will be gained by a factor of one regardless of gain of the front end of the circuit. Consequently, large common mode signals can be handled at

all gains as long as the signals stay within A1 and A2 input and output head room limitations. If the common mode errors of the input amplifiers track they will be cancelled by the output stage.

If the assumption that R_1/R_2 equals R_3/R_4 is not correct, there could be a noticeable common mode voltage error. The calculated common-mode rejection (CMR) error that is attributed to resistor mismatches in this circuit is equal to:

$$CMR = 100^{*} \left(\frac{1 + \frac{R_2}{R_1}}{(\% \text{ of mismatch error})} \right)$$

for $R_4 = R_0$ and $R_0 = R_4$

An example of the impact of this error is demonstrated with a 12-bit, 5V system, where the gain of the circuit is 100V/V, the common-mode voltage ranges 0 to 5V and the matching error can be as large as $\pm 1\%$. Using the formula above, the contributed error of this type of common-mode excursion is equal to 1mV. This voltage is slightly less than 1LSB.

In a single supply environment, the voltage reference should be equal to the center of the input signals. This voltage is represented in the circuit in Figure 5 as V_{REF} . The purpose and effects of this reference voltage is to simply shift the output signal into the linear region of the amplifier.



Figure 5: This is a three op amp implementation of an instrumentation amplifier.



Figure 6: The reference voltage in Figure 5 can be implemented by using a precision reference circuit (a.) or a resistive voltage divider circuit (b.).

The V_{REF} circuit function can be implemented with a precision voltage reference or with the resistive network shown in Figure 6.

ANALOG FILTERING

A big topic for debate in digital design circles is whether or not an analog filter is needed and more importantly, can a digital filter replace the analog filter.

A common assumption with designers that are trying to tackle analog challenges of this type is that they claim that they are only measuring DC so they don't have to worry about filtering. Unfortunately, the noise generators in the electronics and the environment do not have the "intelligence" to accommodate the designer's desires. Consequently, if a filter is not included, the circuit will be surprisingly noisier than anticipated.

Once it is accepted that a filter is required, the next debate that ensues is whether the filtering strategy should be analog, digital or both.

A common assumption that is made by programmers is that they can eliminate all ills with digital filtering. To some extent this is true, however, it is at a high price of time and memory and truthfully, it may not be possible to succeed.

Analog filtering removes a considerable amount of headaches for the programmer from the start. Analog filters have their place in circuit designs as do digital filters. For instance, analog filters will eliminate aliasing errors that will occur through the A/D conversion process if they are allowed to go through. Once these errors are allowed in the conversion it is impossible to discriminate good signal from aliased signal in the digital domain. The analog filter also removes large signal noise that is generated by spikes or spurs in the signal. These signals are usually unintentional, but almost always destructive if not controlled. On the down side, analog filters can add to the noise floor particularly if a noisy amplifier is used with a large gain.

Where analog filters earn their worth by rejecting noise in the out of band region, digital filters can be utilized to reduce the in-band noise floor. This is implemented with oversampling algorithms. These types of filters are much easier to change on the fly because it is a matter of programming instead of a matter of changing resistors and capacitors as it is with analog filters. With all of these benefits there is a price to pay in terms of response time. Digital filters must collect a certain amount of conversion data before calculations can be performed. The digital filter algorithms tend to slow down the response time as well as delay the output. If real time responses are not critical, the digital filter disadvantages are not detrimental to the operation of circuit.



Figure 7: By using FilterLabTM software, this 2nd order low pass filter that has a non-inverting gain in the pass band can be configured as a Butterworth, Bessel, or Chebyshev filter.

As discussed previously, the hardware implementation of a low pass filter at its most fundamental level requires a capacitor and resistor for each pole. Active filters, which have one amplifier for every two poles, have the added benefit of preventing conflicting impedances and degrading the signal path.

The 2nd order lower pass filter shown in Figure 7 is one of a class of circuits that were described in 1995 by R.P Sallen and E.L. Key. With this filter the DC gain is positive. In a single supply environment this eases the implementation considerably, because a mid-supply reference is not required. This circuit not only filters high frequencies, but it can be used to gain the incoming signal. Close inspection of this filter shows that the circuit can be configured in a gain of +1V/V by shorting R_4 and opening R_3 . In this configuration it is likely that the input of the amplifier will be exercised across a full rail-to-rail input range.

The second order Multiple Feedback circuit implementation of a low pass filter uses an amplifier, three resistors and two capacitors, as is shown in Figure 8. The DC gain of this filter is negative and easily adjusted with the ratio of R_3 and R_1 . When used in a single supply environment, this circuit usually needs a voltage reference on the non-inverting input of the amplifier.

This is the filter circuit that will be used in a barometric pressure application. An adjustable voltage reference will be Included in this filter design.



Figure 8: By using FilterLabTM software, this 2nd order low pass filter that has an inverting gain in the pass band can be configured as a Butterworth, Bessel, or Chebyshev filter.

BAROMETRIC PRESSURE SENSING

The considerations for the design of a barometric sensing system encompasses altitude and resolution. The expected altitude that our sensor will be placed in is approximately from sea level to 20,000 ft. The nominal pressure at sea level is 14.7 psi and the nominal pressure at 20,000 ft. is 6.75 psi. The difference in pressure between these two altitudes is 7.95 psi. With this range, the appropriate pressure sensor should be an absolute version that is referenced to an on-chip vacuum and have a range up to 15psi. Since the change in pressure for major weather changes is approximately 0.18 psi, a resolution of 0.015 psi is over ten times more accurate than the measured value. The circuit that will be used for this design discussion is shown in Figure 9.

The critical pressure sensor specifications for this application include the operating pressure range, sensitivity, room temperature ($25^{\circ}C$) span and offset errors as well as over temperature (see Table 1). Although, the range of this sensor extends from 0 psi to 15 psi, this application will not be using that lower range. The minimum differential output voltage from the sensor will be 40.5mV (6.75psi or 20,000 ft.) and the maximum sensor voltage will be 88.2mV (14.7psi or sea level). The voltage at the output of the sensor is gained before it is digitized using an instrumentation amplifier.

Parameter (w/ 5V excitation)	Specification
Operating Pressure Range	0 to 15 psi
Sensitivity	6.0mV/psi (typ)
Full-Scale Span	90mV (typ)
Zero Pressure Offset	$\pm300\mu V$
Temperature Effect on Span (0 to 70°C)	± 0.5% FSO
Temperature Effect on Offset (0 to 70°C)	$\pm 500 \mu V$

Table 1: The specifications of the SCX015 fromSenSym indicates that this is a good pressuresensor that can be used to measure barometricpressure.

The specifications of the SCX015 from SenSym indicates that this is a good pressure sensor that can be used to measure barometric pressure.

Note that temperature issues are beyond the scope of this application note. Detailed information about temperature sensing circuits can be found in Microchip's AN679, AN684, AN685, and AN687.



Figure 9: The voltage at the output of the SCX015 pressure sensor is gained by the instrumentation amplifier (A1 and A2) then filtered, gained and level shifted (A4) with a 2nd order low pass filter (A3) and digitized with a 12-bit A/D converter (A5).

Instrumentation Amplifier Design

This sensor requires voltage excitation. In order to determine the required gain of the circuit in Figure 9 the relationship between the maximum sensor output and allowable instrumentation amplifier output is used in the calculation. As stated previously, the maximum differential output of the sensor is 88.2mV. The allowable output range of the instrumentation amplifier is equal to V_{DD} - 100mV. In a five volt system where V_{DD} = 5V, the amplifier output maximum is equal to 4.9V. The minimum output of the sensor is 40.5mV. Since this is a positive voltage and the instrumentation amplifier is in a single supply environment, this minimum sensor output voltage will not drive the output of the instrumentation amplifier below ground. Consequently, the reference voltage called out in Figure 3 and Figure 4 is made to be equal to ground.

Gain is calculated by dividing the maximum output voltage with the maximum input voltage. Using this calculation, the appropriate gain for our system is 55.6V/V. By using the gain formula in Figure 5:

$$R_{G} = \frac{2R_{1}}{\left(\text{Gain} - 1 - \frac{R_{1}}{R_{2}}\right)}$$

If $R_{1} = 30k\Omega$ and $R_{2} = 10k\Omega$,

$$R_G = \frac{60\,k\Omega}{(55.6-4)}$$

=
$$1.15 k\Omega$$
 (closest 1% value)

With this gain, the maximum output of the IA will be 88.2mV*55.6V/V or 4.9V and the minimum output will be 40.5mV*55.6V/V or 2.3V.

Since the gain of this instrumentation amplifier stage is relatively large, it is desirable to use an amplifier that has a low offset voltage. The MCP607, dual CMOS amplifier has a guaranteed input offset voltage of $250\mu V$ (max). This amplifier's low quiescent current of $25\mu A$ (max) make this device attractive for battery powered applications.

Filter Design

Now that the signal from the pressure sensor has been properly differentiated and gained, noise is removed to making the results from the 12-bit A/D conversion repeatable and reliable. Remember that the output of the instrumentation amplifier circuit does not swing a full 0V to 5V. Consequently, the filter stage will also be used to implement a second gain cell as well as offset adjust.

The stop frequency of this filter is 60Hz. This will removes any mains frequencies that may be aliased back into the signal path during conversion. This being the case, the cut-off frequency is selected to be 10Hz. Any cut-off frequency lower than 10Hz, requires capacitors that are too large, making the board implementation awkward. The total attenuation between 10Hz and 60Hz is approximately -30dB. In other words, a 60Hz signal that is part of the output signal of the instrumentation amplifier is attenuated by 0.031 times. Keeping in mind that the instrumentation amplifier has already rejected a major portion of any 60Hz common-mode signal, this level of attenuation is enough to remove any remaining 60Hz noise that exists in the signal path.

The gain and offset adjust features of this filter are also used in this segment of the application circuit. Given that the output from the instrumentation amplifier is 2.3V to 4.9V, the peak-to-peak voltage of this signal is 2.6V. A gain of 1.8V/V will produce an output swing of approximately 4.7V peak-to-peak. The adjustable offset voltage of this circuit which is gained by 2.8V/V will be configured to insure that the signal will fall at the output of the amplifier between the supplies. This adjustment circuit can also be used to remove system offset errors that originate in the sensor or instrumentation amplifier.

The filter circuit in Figure 9 can be designed with the FilterLabTM software from Microchip Technology. The two capacitors are adjusted using the FilterLab program to be equal to 0.22uF. This adjustment is made in order to keep the capacitor packages small enough so surface mount capacitors can be used.

The offset adjust of the filter circuit is implemented with a $10k\Omega$ digital potentiometer in series with a $68.1k\Omega$ and $35.7k\Omega$ resistors. The range of the offset adjust portion of this circuit at the wiper of the digital potentiometer is from 3.0V to 3.4V. This offset circuitry is gained by the filter/amplifier circuit so that the nominal value of the offset circuitry in combination with the sensor signal is equal to:

V_{OUT-FILTER} = -1.8V/V (Nominal Input Signal) + 2.8V/V (Nominal Reference voltage)

 $V_{OUT-FILTER} = -1.8V/V (3.6V) + 2.8V/V (3.2V)$

 $V_{OUT-FILTER} = 2.48V$

A key amplifier specification for this filtering circuit is input voltage noise. The MCP601, single CMOS amplifier has a typical noise density of 29 nV/ \sqrt{Hz} @ 1kHz.

A/D Converter Design

The final design step for this analog signal path is to insert the analog-to digital converter. The converter quantizes a continuous analog signal into discrete buckets. The appropriate converter can be selected once it is determined how many bits the application requires.

The range of the analog signal has been closely matched to the input range of a zero to 5V in A/D converter.

The barometric pressure range is 14.7 psi to 6.75 psi. The expected increase from good weather to a strong storm system would be approximately 0.18 psi. Given this, the equipment should resolve to at least 0.015psi. This is easily achieved with a 10-bit converter. If resolution to 0.002 is needed a 12-bit a/d converter would be more suitable.

Microchip has a large variety of analog to digital converters that can be used for this application. If the stand-alone solution is appealing, the MPC320X family of 12-bit and the MCP300X 10-bit family of converters are available.

Generally speaking, stand-alone A/D converters have better accuracy than those compared to on-board converters. They also have features such a pseudo differential inputs and faster conversion speeds. The pseudo differential capability of these devices allow for configurations that reject small common mode signals. Additionally, the single channel devices can be used in simultaneous sampling applications, such as motor control. The application circuits using the singe converter also require fewer analog filters because the multiplexer is typically placed before the anti-aliasing filter.

If an on-board a/d converter fits the application better, the PICmicro line has a large array of converters combined with other peripherals on a variety of micros that can be used.

The integrated solution offers a degree of flexibility that the stand-alone solution does not have. This flexibility comes in the form of operational flexibility where the device's voltage reference and sampling speed can be reconfigured on the fly. The I/O configuration is also very flexible allowing for easy implementation of the board layout.

The stand-alone and integrated A/D converters from Microchip are both suitable for the pressure sensor circuit that is shown in Figure 9.

CONCLUSION

The design challenge that has been tackled in this application note is gaining, filtering, and digitizing the small differential signal of a pressure sensor bridge. In order to achieve this goal, we used a two-op amp instrumentation amplifier which gained the differential signal from the pressure sensor and converted it to a signal ended output. After this gain stage, a 2nd order, Butterworth, anti-aliasing filter was used to reduce noise so that the A/D converter could achieve a full 10-bit accuracy.

The suggested A/D converter strategy could be on board or off board and the trade-offs were presented. Digital filtering was not needed in this application.

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