



**MICROCHIP**

# AN676

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## Physical Slot Identification Techniques for the 24LCS61/62

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### INTRODUCTION

With the complexity of systems ever increasing, system designers are faced with new challenges in identifying and assigning system resources on-the-fly. Often a system will have multiple peripheral cards that must be added on demand to fill a processing requirement or configuration. These cards will need to be dynamically identified and added to the system's resource management database.

Various Plug and Play (PnP) solutions have been developed to meet these requirements. A common thread among PnP schemes is to have a lower bandwidth channel, such as the I<sup>2</sup>C bus, allocated as a means of interrogating newly added system cards. Through this data link, the system master can get or assign crucial information and calibration data from a specific card, without impacting the system's higher bandwidth bus.

### SOFTWARE ADDRESSABLE SOLUTIONS

The Microchip Technology Inc. 24LCS61/62 is a 1K/2K bit Serial EEPROM developed for applications that require non-volatile storage of data and to have many devices on the same bus but do not have the spare I/O pins required to address each device individually. These devices contain an 8-bit address register that is set upon power-up and allows the connection of up to 255 devices on the same bus. When the process of assigning ID values to each device is in progress, the device will automatically handle bus arbitration if more than one device is operating on the bus. In addition, an external open drain output pin ( $\overline{EDS}$ ) is available that can be used to enable other circuitry associated with each individual system. See the Microchip 24LCS61/62 (DS21226) data sheet for further information on these devices.

### A PNP SCENARIO APPLICATION

This application will utilize a system made of multiple circuit cards plugged into a backplane. A common high bandwidth bus and an I<sup>2</sup>C™ bus will interconnect the slots of the backplane. The system master must create a table that correlates the card type inserted into each slot. To do this, the system master needs to read the information about each board in the system. This information is stored in the 24LCS61/62 on that board. The system master also needs to determine the physical slot number that the board is plugged into. Listed below are five methods for determining physical slot locations.

# AN676

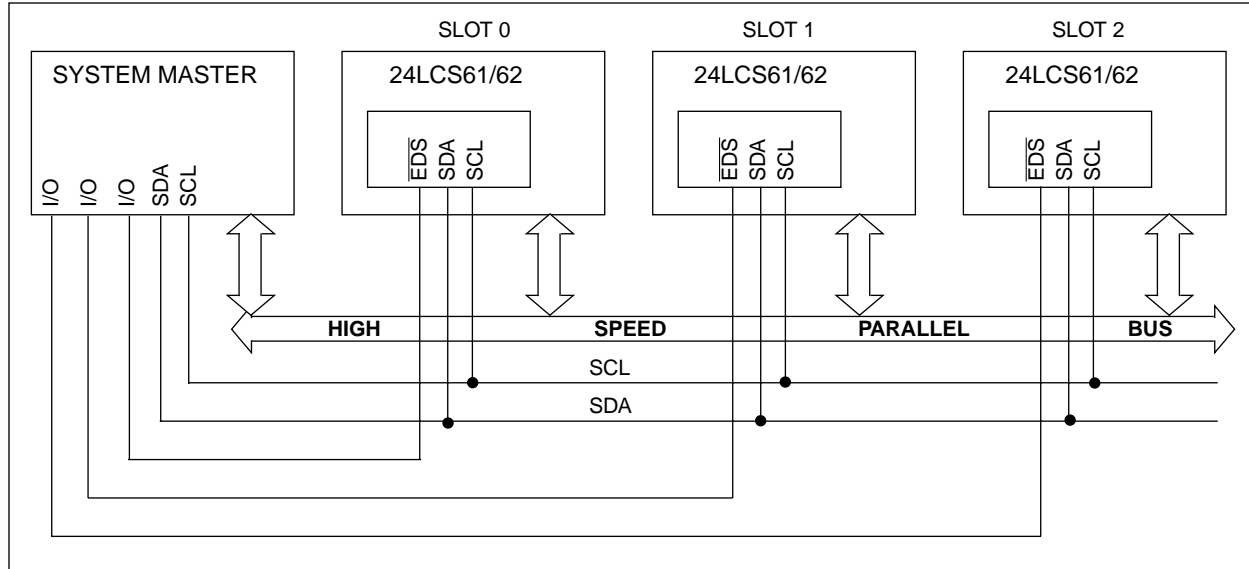
## Method 1: Direct Connection of the $\overline{\text{EDS}}$ Pins to the System Master

The simplest method to determine the physical slot location is to route the  $\overline{\text{EDS}}$  output pin from each card back to the system master. This physical connection, or return line, serves as a fixed slot identifier. Each device on the bus would then be identified by connecting this

line to a unique input pin on the system master. After performing the arbitration process, the system master can toggle the output of the  $\overline{\text{EDS}}$  pin on a particular device, and sense the resulting physical slot location indicated by polling the I/O pins.

This method requires equal number of return lines as there are devices on the bus.

**FIGURE 1: METHOD 1**



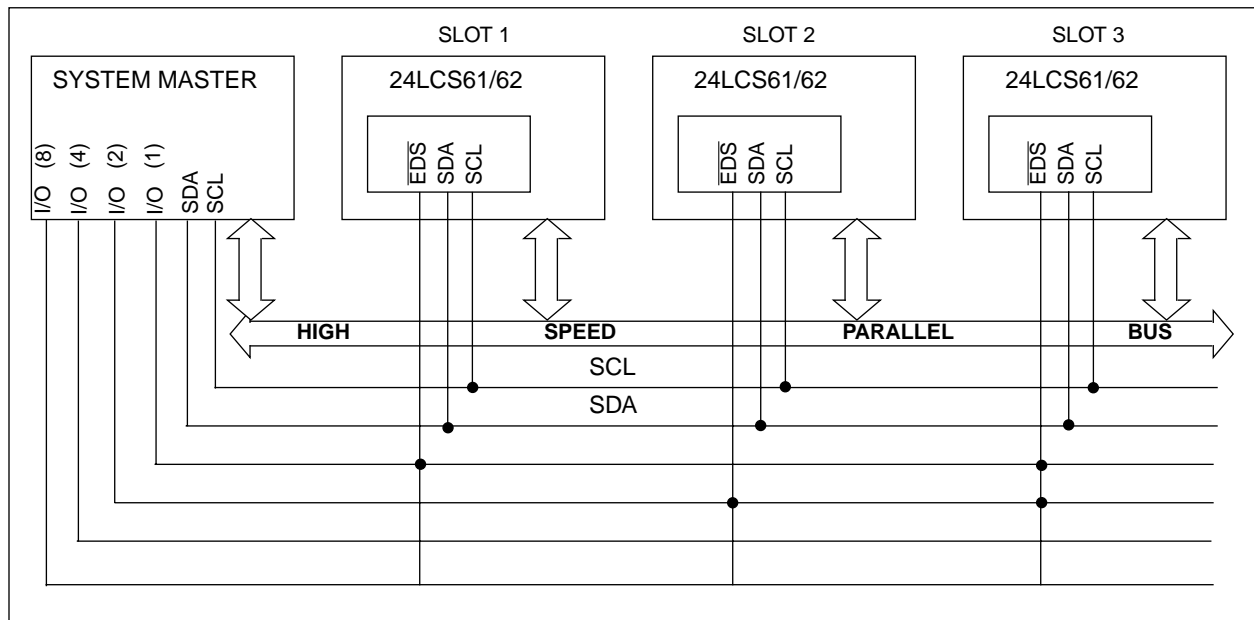
## Method 2: Encoded Return Lines to System Master

Dedicated return lines can be encoded to identify physical slots. The encoding is made by the connections, or lack of connections, between the  $\overline{\text{EDS}}$  pin on a particular device, and the return lines going back to the system master. These connections take place on the main bus backplane. After arbitration, the system master would activate the EDS pin on a single device in sequence, and read the encoded value on the return lines connected to the I/O pins. The physical slot identifier will be returned in binary coded form. In the example shown below, asserting the  $\overline{\text{EDS}}$  pin on the device in slot 1 will yield the binary "0001", indicating to the master that this device is in slot 1. In this method, N return lines can encode a maximum of  $2^N$  devices on the bus.

This method has the advantage that it only consumes one pin on the connector between the board and the backplane. Therefore, the entire bus to identify and interrogate boards in the system will only require three pins (SCL, SDA and  $\overline{\text{EDS}}$ ) on the backplane connector.

For further reliability assurance, the designer can drop the code which has no physical connections to any return lines (i.e., "0000"). This would make every valid slot identifier assert at least one return line. This eliminates the possibility of a faulty device being erroneously assigned the '0' slot identifier. This lowers the total allowable number of slots given N return lines to  $2^N - 1$ .

**FIGURE 2: METHOD 2**



## Method 3: Microcontroller Slot Address Sensing, and Serial Communication

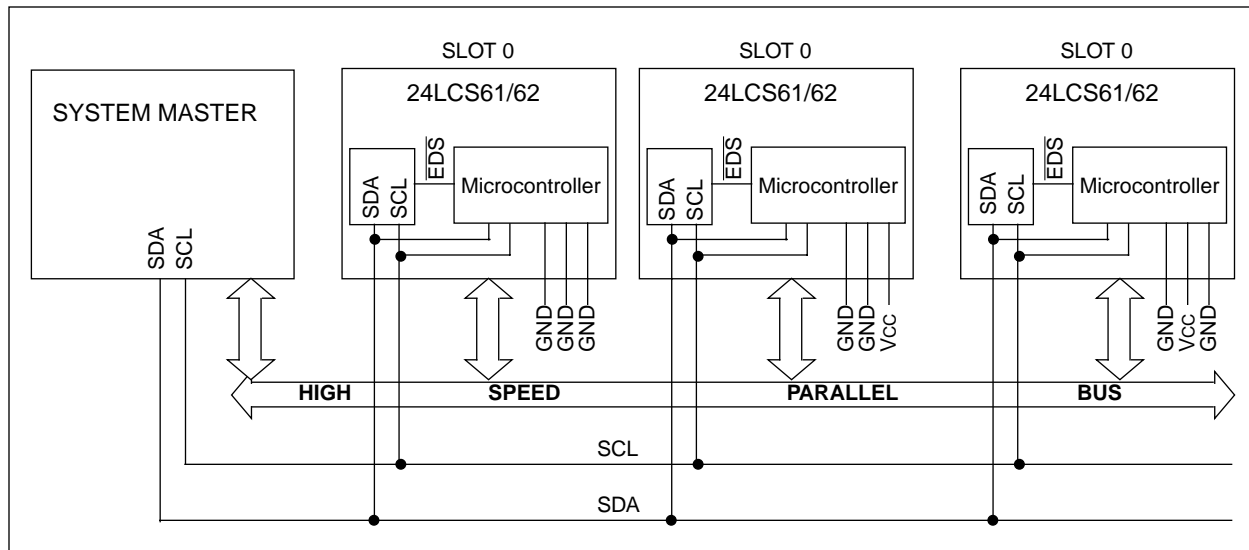
Each card contains a 24LCS61/62 nonvolatile memory device, and a dedicated microcontroller (this example uses the Microchip PIC16C57) for transmitting slot information serially over the I<sup>2</sup>C bus. Both are connected to the backplane's I<sup>2</sup>C bus. The microcontroller on the card uses two dedicated I/O lines for SDA and SCL connections. This provides a feedback path for determining the physical slot in which a card resides. Other dedicated I/O lines by the microcontroller to sense a slot number from the dedicated connector pins. These pins are encoded with the slot identifier on the backplane.

First, the system master processor will initiate the 24LCS61/62 arbitration process until all memory devices are assigned unique ID. Next, the system

master will sequentially address each 24LCS61/62 and assert the EDS pin. The EDS line serves as a select line for that particular microcontroller, and puts that microcontroller into a state where it will respond to commands from the system master. The microcontroller can wake up to a normally formatted I<sup>2</sup>C command and respond with the physical slot identifier. Because the memory devices on the bus wake up to 06XH, and the microcontroller wakes up to 0AXH, there will never be a bus contention issue between them.

The number of I/O lines dedicated to sensing physical slot information will determine the number of devices addressable on the bus. If the microcontroller has eight I/O lines then the full number (255) of 24LCS61/62's can be addressed.

**FIGURE 3: METHOD 3**



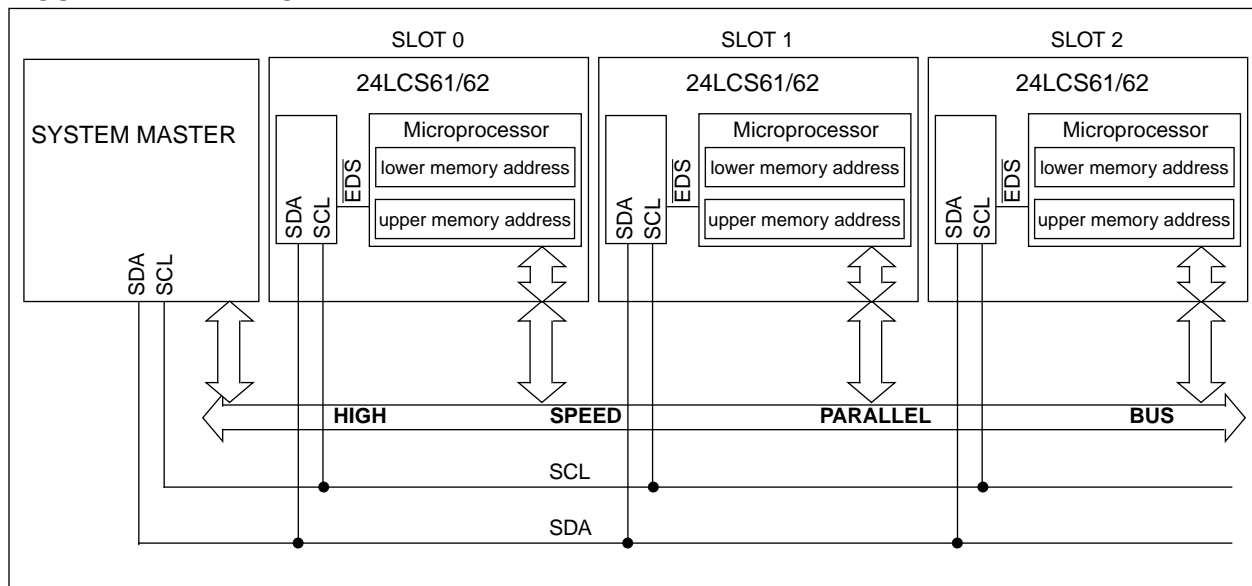
## Method 4: Virtual Memory Addressing on Cards

This method is applicable when all communication between boards is accomplished by transfers between memory spaces on each board. In this scenario, the system master starts by querying the I<sup>2</sup>C bus looking for unassigned 24LCS61/62 devices. This is done by repeatedly sending the assign address command and checking for acknowledging devices. If a device acknowledges, then a software address is assigned to that device after the arbitration cycle has been completed. The system master can then either continue assigning software addresses to any remaining 24LCS61/62 devices on the bus, or it may immediately assign a "virtual memory address" to the board associated with the just assigned 24LCS61/62 device (hereafter referred to as the "slave board"). The first step of assigning the virtual address is to read the configuration data from the 24LCS61/62 device. This tells the system master the amount of virtual memory space to reserve for the slave board. The system master would then issue a command to the 24LCS61/62

device with the OE bit set to '1', which enables the  $\overline{\text{EDS}}$  pin on the 24LCS61/62 device. The  $\overline{\text{EDS}}$  pin is tied to an input on the slave board microcontroller which signals it to enter a "receive virtual address" mode. Once the slave board is ready to receive the virtual address the system master sends the necessary information out over the main system bus to be received by the current slave board. Any necessary communication between the system master and the slave board is completed and the system master then issues a command to the 24LCS61/62 device with the OE bit set to a '0', which signals the slave board microcontroller to terminate the assign virtual memory address mode. This sequence is then repeated until no unassigned 24LCS61/62 devices remain on the I<sup>2</sup>C bus. Once the process is complete the slave board can be addressed by its virtual address.

This method has the advantage of requiring only one I/O pin on the slave board microcontroller, and may be used when it is not necessary to know which physical slot a slave board is in.

**FIGURE 4: METHOD 4**



## Method 5: Microcontroller Slot Address Sensing and Communication over System Bus

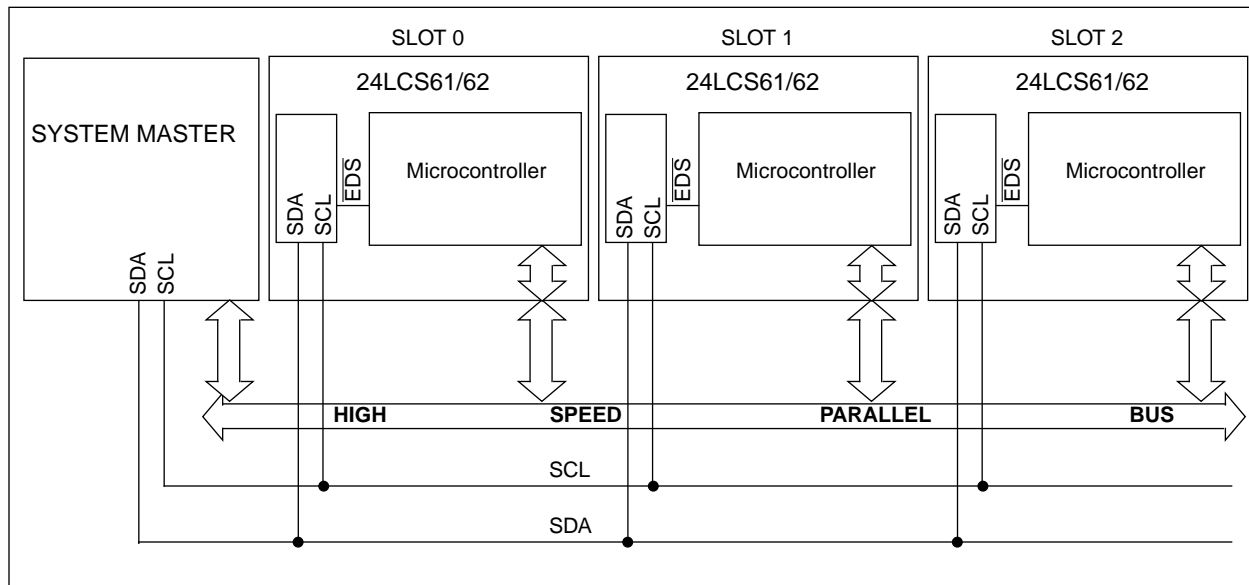
This method may be used if the physical slot must be identified and thus the slot ID number is hard-coded into the slave board connector. In this scenario the  $\overline{EDS}$  pin of the 24LCS61/62 device is used to enable the slave board microcontroller in the same way as in the method above, however, once enabled, the slave board microcontroller reads the hard coded physical slot number and then sends this information to the system master via the system bus. From that point on the slave board can be addressed by using its slot ID number.

This method again requires only a single I/O on the slave board microcontroller, and is effective when the physical location of a given slave board must be known.

## CONCLUSION

The Microchip 24LCS61/62 is a powerful building block in creating a board identification solution for multiboard systems. The methods outlined above are generic in nature, and meant to serve as a starting point for development of individual solutions for physical slot identification.

**FIGURE 5: METHOD 5**



**NOTES:**



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