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Improving the Susceptibility of an Application to ESD-Induced Latch-up

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All semiconductor devices are sensitive to electrostatic discharge (ESD) damage to varying degrees. This is true whether they are soldered to a PC board in an application, or whether they are unattached in the shipping or application assembly process. Good handling techniques such as groundstraps, static free work stations and ionizers can reduce the risk of static build up during assembly. Often more attention is paid to reducing ESD during assembly than is paid to reducing ESD risk during the lifetime of the application.

When a device is installed in an application, it is still susceptible to damage due to ESD. This can take on a different form when the application is powered up and running. If power is supplied to a CMOS device, such as a memory product or a microcontroller when an ESD event occurs, the device can be triggered into a "latch-up" condition. This is a high current mode where internal circuitry can be disturbed into making a short circuit (or a circuit with very low resistance) between power (V_{CC}) and ground (V_{SS}) on a device. This condition is self-sustaining; it does not require subsequent ESD events to continue the latch-up condition.

This short circuit will tend to reduce the voltage level on the application (particularly if the application is battery powered) and will do a great deal of damage to the device which has latched-up. The only way to halt this condition is to remove power from the device.

Microchip uses careful design practices to reduce the susceptibility of all products (microcontrollers or memories) to ESD events. However, the protection level varies for pin-to-pin, reflecting the different functions of each pin. Certain types of pins (notably supply pins) are much more susceptible to latch-up caused by ESD pulses than other pins. This is due to the different design and layout considerations that reduce the effectiveness of ESD protection.

There is a great deal that the system designer can do to improve (by up to an order of magnitude) the level of protection of a device from latch-up inducing ESD events. This tutorial is intended as a guide for helping designers choose protection. This type of protection is application dependent, so consideration should be made of the type of environment that the application, or the device, will be in.

FIGURE 1: CIRCUIT DIAGRAM FOR ESD-INDUCED LATCH-UP

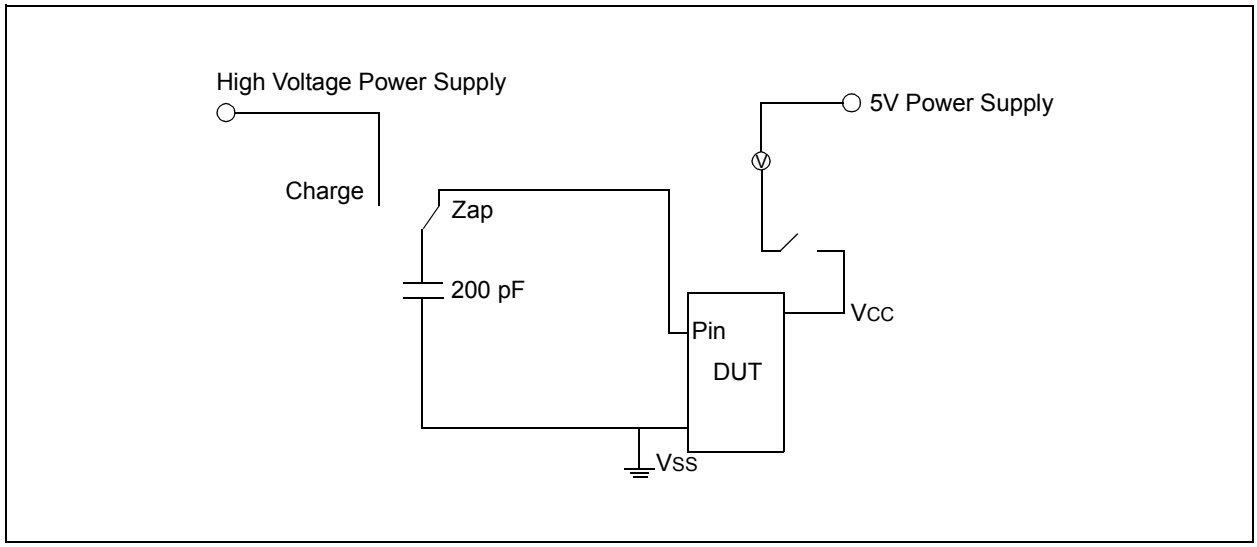
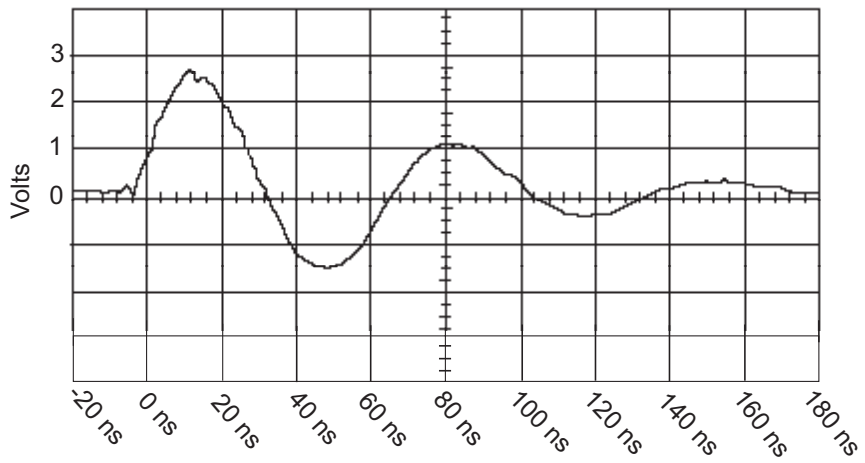


FIGURE 2: WAVEFORM USED TO SIMULATE ESD EVENT



Ch. 1	=	1.000 Volts/div.	Offset	=	0.000 Volts
Time base	=	20.0 ns/div.	Delay	=	-20.000 ns

ELECTROSTATIC DISCHARGE

Electrostatic discharges can come from a variety of sources. The traditional ESD pulse is caused by a body at very high potential coming into contact, or near contact, with a grounded object. This could be a human body, a piece of electrical equipment, or even a piece of furniture.

In a dry environment, where static dissipation is low, a human body can develop tens of thousands of volts of potential. Almost everyone has experienced the shock of walking across a new carpet and touching a door handle. An audible snap can be heard when the potential difference between the person and the door handle is around 5,000V.

Any piece of equipment which has metal components moving against other metal components can develop a charge. An automated device handler will generally have a metal tray where devices move around, with pins in occasional contact with the tray. Static build up can reach hundreds of volts and can damage the devices in the same way as an ungrounded human handler can.

Incorrectly placed ionizers, meant to improve static dissipation, can build large potentials on office or laboratory furniture. Any person touching such a piece of furniture might feel a shock. Any devices being placed on a table with a large potential can suffer damage.

All these situations can be avoided by careful handling procedures. Groundstraps for manual handling of devices is essential, as are grounded tables and work surfaces with anti-static surfaces such as metal or specially designed plastic mats. Equipment can be carefully grounded wherever the potential exists for static build up.

ELECTROSTATIC DISCHARGE IN A POWERED APPLICATION

Once the device has been mounted to a board or installed in an application, most types of ESD events will no longer occur. For example, unless the PC board is out in the open, it is very unlikely to be touched by the user, and so a direct ESD pulse will not be a concern.

However, there are several sources of indirect ESD pulses, or noise pulses which are very similar in nature and magnitude to ESD pulses. ESD pulses can induce currents in nearby wiring. So, for example, if the user creates an ESD event on the casing of an application, the magnetic field of the pulse can induce currents inside the casing, in the wiring of an application. This electromagnetic interference can occasionally be seen in other ways, such as a noisy TV picture when a vacuum cleaner is being used, or a “click” heard on the radio when a light switch is turned on. This type of event is often called Radio Frequency Interference (RFI) or Electromagnetic Interference (EMI).

Often the application itself can induce noise spikes during operation. If one component in that application is a high speed, high current transistor or other type of switch, the sudden change in current can induce a noise spike which could be seen by that component, or other components in the system. This switching noise is endemic in systems with metal wires, and can not be removed completely. Large magnitude pulses of switching noise can induce latch-up on sensitive CMOS devices.

The effects of switching noise or EMI can be catastrophic to an application with sensitive components. Even components which are not particularly sensitive or already have some built-in protection (such as Microchip Technology Inc.'s products) can still be latched-up by noise pulses if they are of a large enough magnitude.

PROTECTING AGAINST ESD PULSES

Basic protection can be provided by a simple decoupling capacitor, placed as close as possible to the power and ground pins of components. Each component should have its own capacitor; simply decoupling the whole application at the supply points will not be sufficient if a component in the application is producing noise.

If the value of the capacitor is chosen to match the device, then non-supply pins can also benefit from a decoupling capacitor between power and ground. A single capacitor can not filter out all the frequencies associated with a noise spike, but it can still offer very effective and low-cost protection.

We used a simple test circuit to accurately model an ESD-induced noise spike. The test circuit is shown in Figure 1. A 200 pF capacitor was charged to various voltages and then switched to discharge directly into the device being tested. The waveform is a high frequency (≈14 MHz) and short period (≈100 ns) decaying oscillation. The resulting waveform, measured through a Tektronix CT-1 current probe with a 10X attenuator, is shown in Figure 2. The testing was conducted at 25°C.

The period of the oscillation is governed by the relationship:

$$\omega = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$$

where L, C and R are the inductance, capacitance and resistance of the oscillating circuit, and w is the frequency of the oscillation. Since R and L are very small, and C is 200 pF, the oscillation period is very fast.

Two devices were tested. A typical serial EEPROM, the 24LC04B, was tested on all function and supply pins. The results, shown in graphical form (Figure 3 through Figure 7) show that, even with a capacitor placed between power (V_{CC}) and ground (V_{SS}) other pins, such as SDA, can have increased protection. From the figures it is clear that the best all-around protection can be obtained from a 10,000 pF capacitor.

Particular applications may be different. For example, the designer may know that there is a better chance for a noise spike on the SDA signal, and so may want to use a 1,000 pF capacitor to improve the protection level of SDA.

A PIC16C54 microcontroller in XT mode was tested on all functional and supply pins. The results are shown in Figure 8 through Figure 17. From these results, it is clear that the particular application environment will be much more important in determining which capacitor value to use. Some pins, such as $\overline{MCLR}$, do not respond at all to a decoupling capacitor. Others, such as the RA ports, respond strongly to a capacitor. Note that for the RA and RB graphs, the pin with the lowest latch-up threshold was used. All other pins are higher.

It is important for the designer to be aware of the potential problems associated with noise in a powered application. A combination of using sound design techniques to reduce causes of noise and an awareness of the protection levels of the components being used can make the problems of ESD manageable.

FIGURE 3: 24LC04B PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON VSS. PROTECTION CAPACITOR BETWEEN VSS AND VCC.

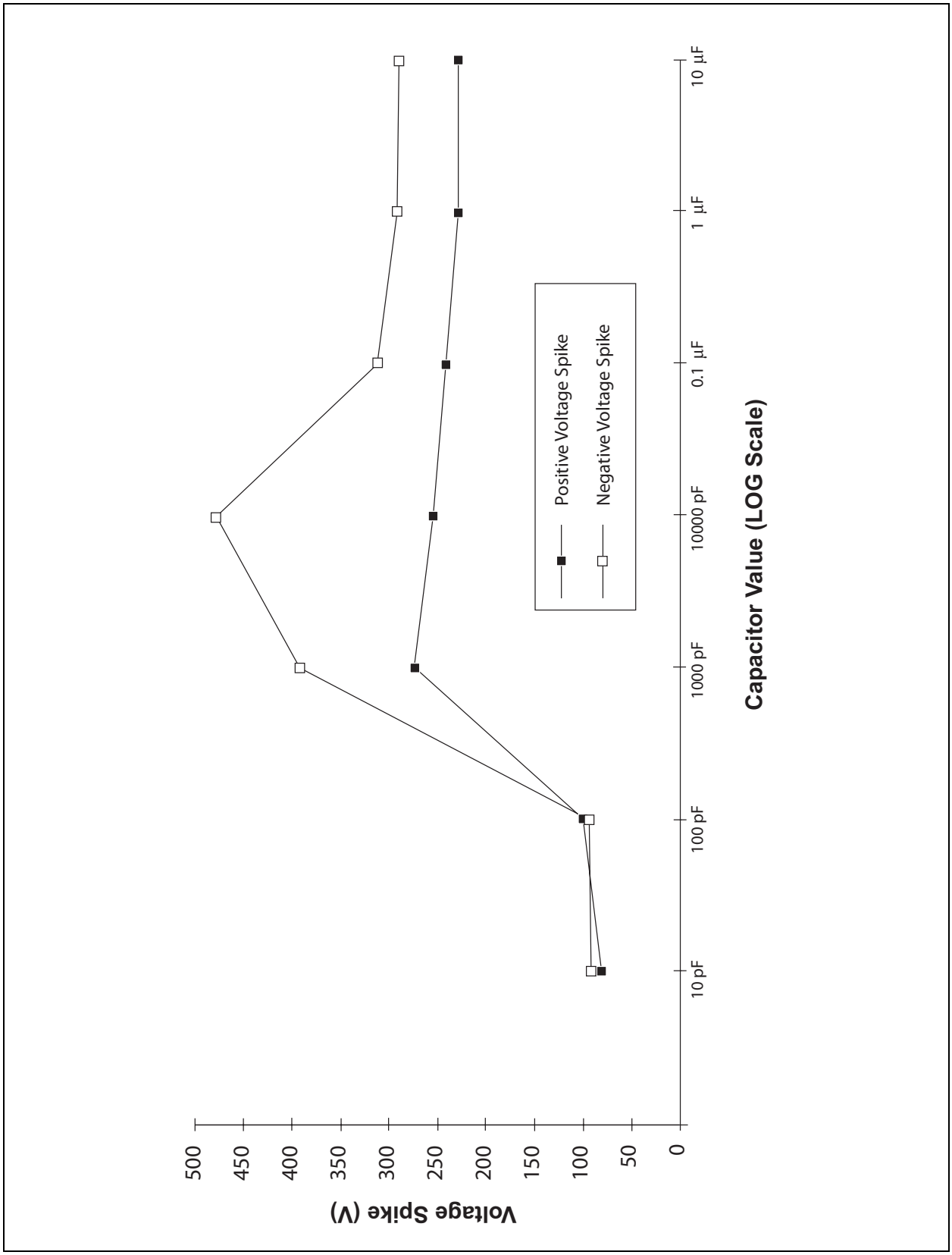


FIGURE 4: 24LC04B PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON SDA. PROTECTION CAPACITOR BETWEEN VSS AND VCC.

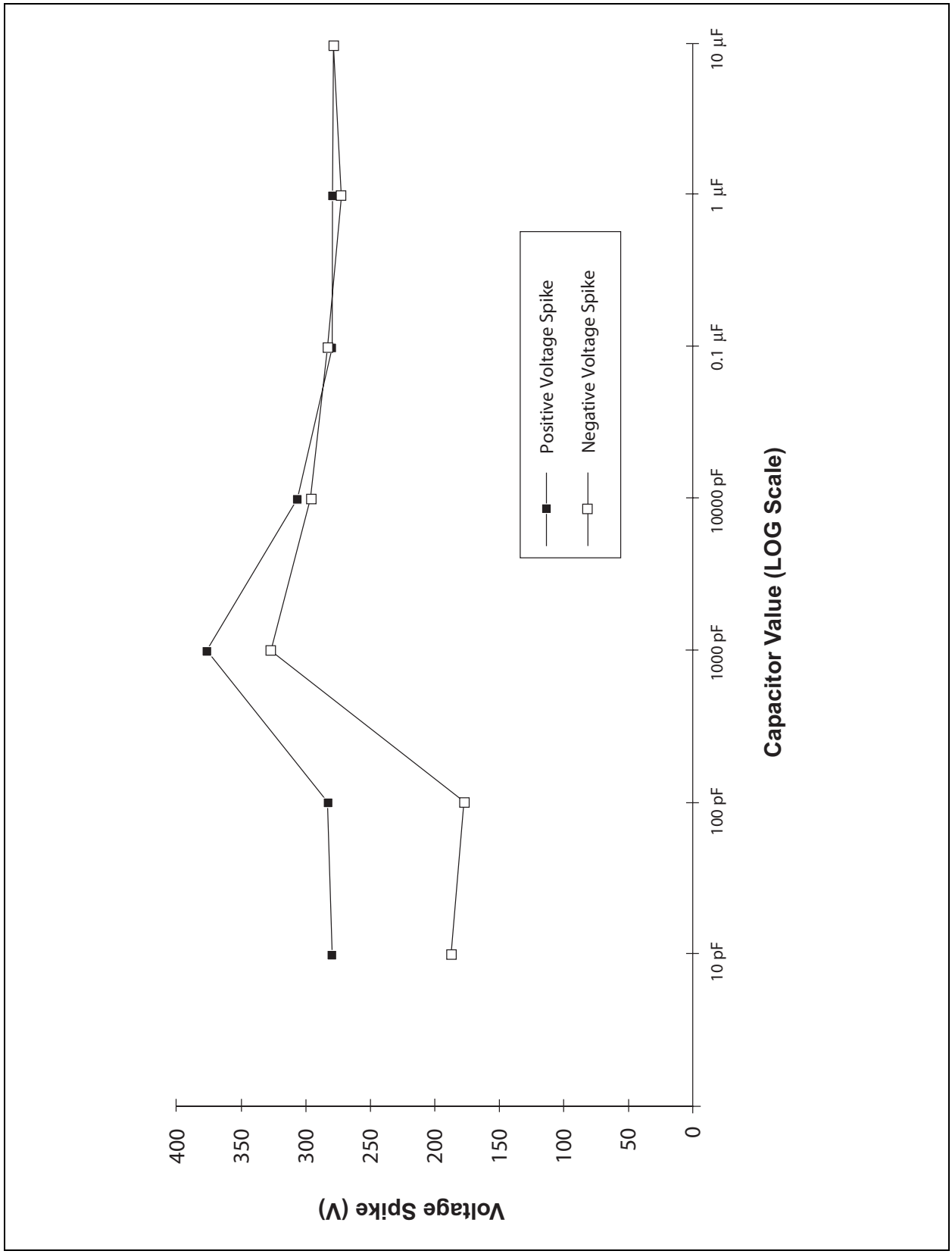


FIGURE 5: 24LC04B PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON SCL. PROTECTION CAPACITOR BETWEEN Vss AND Vcc.

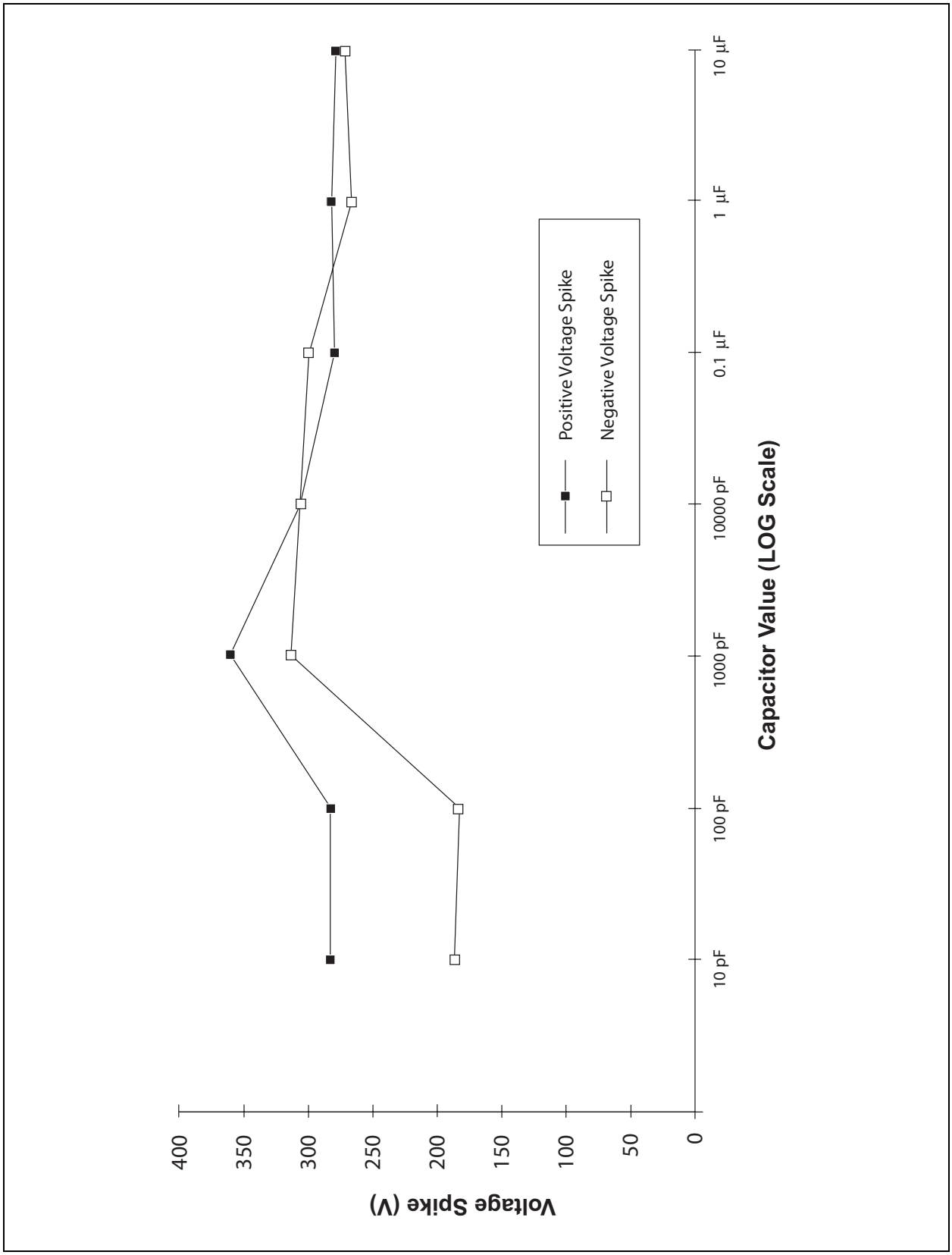


FIGURE 6: 24LC04B PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON WP. PROTECTION CAPACITOR BETWEEN VSS AND VCC.

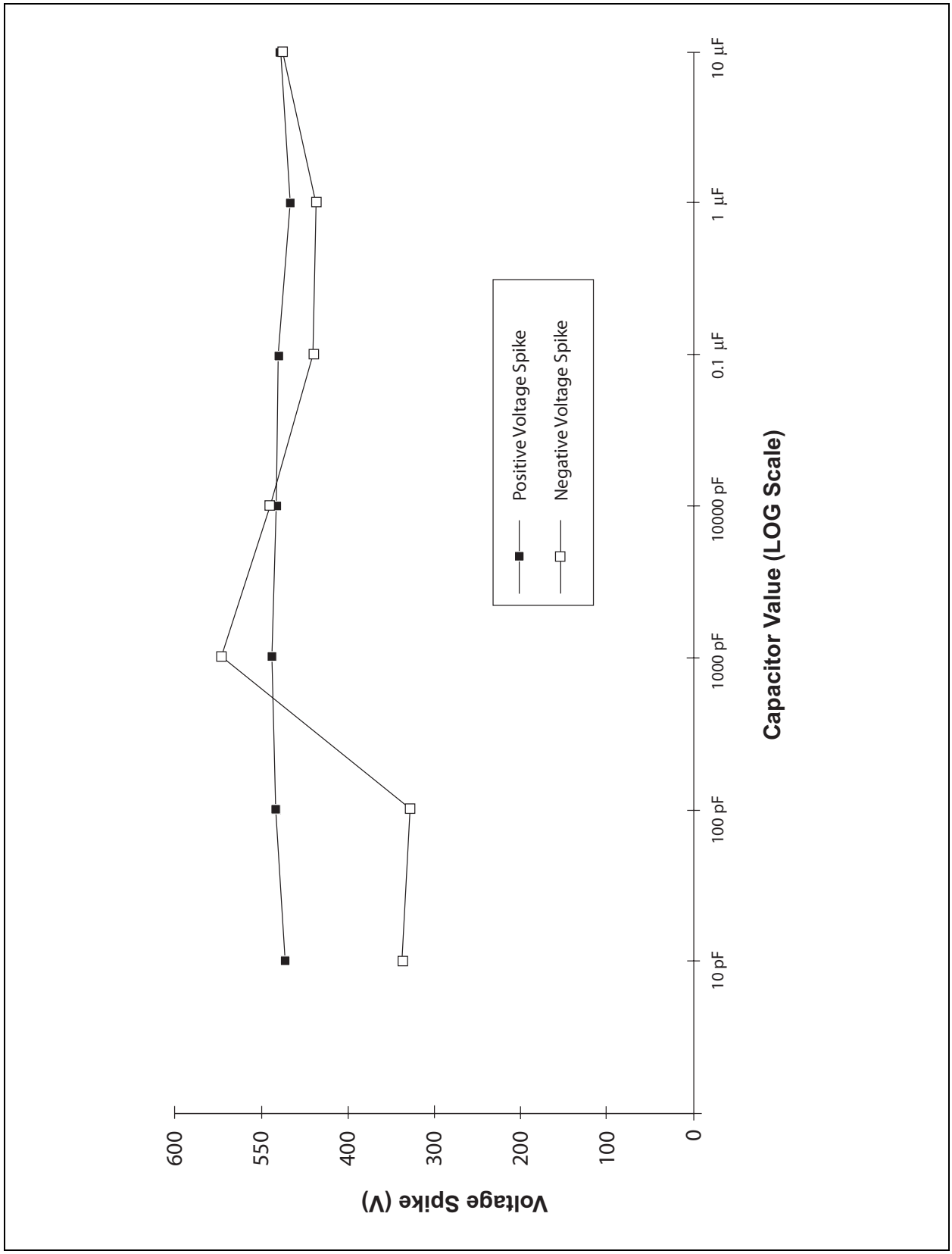


FIGURE 7: 24LC04B PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON VCC. PROTECTION CAPACITOR BETWEEN VSS AND VCC.

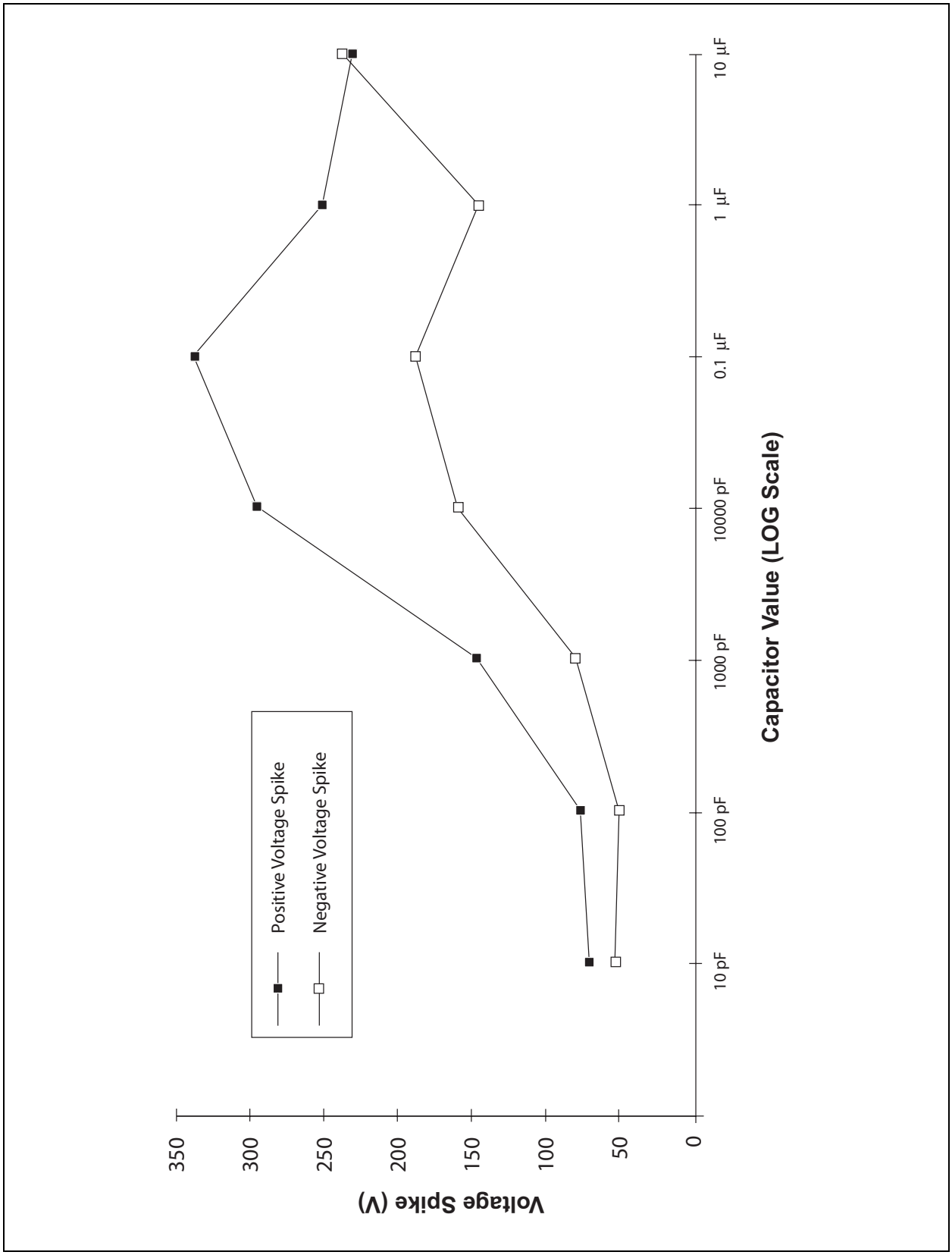


FIGURE 8: PIC16C54-XT PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON RTCC. PROTECTION CAPACITOR BETWEEN Vss AND Vcc.

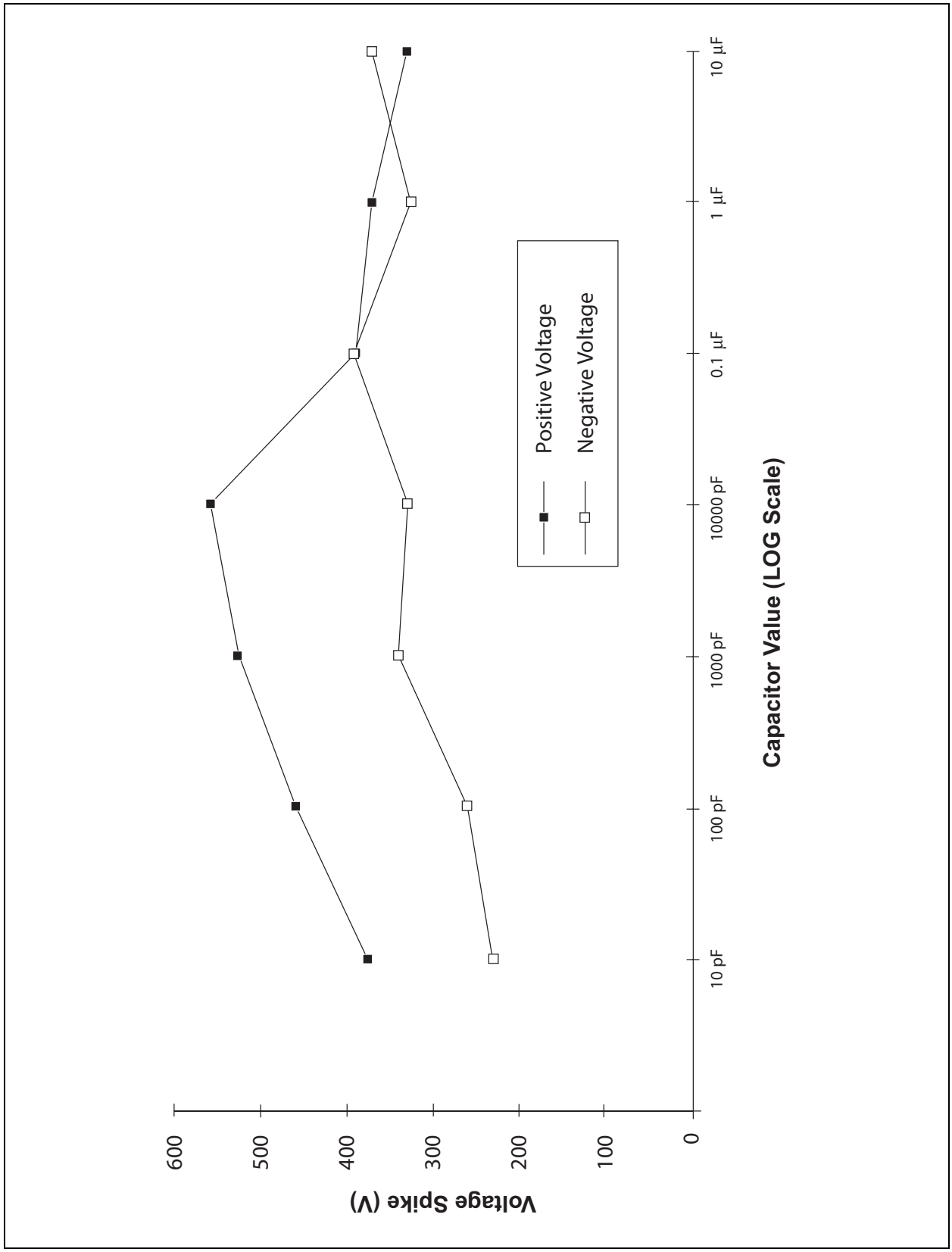


FIGURE 9: PIC16C54-XT PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON MCLR. PROTECTION CAPACITOR BETWEEN VSS AND VCC.

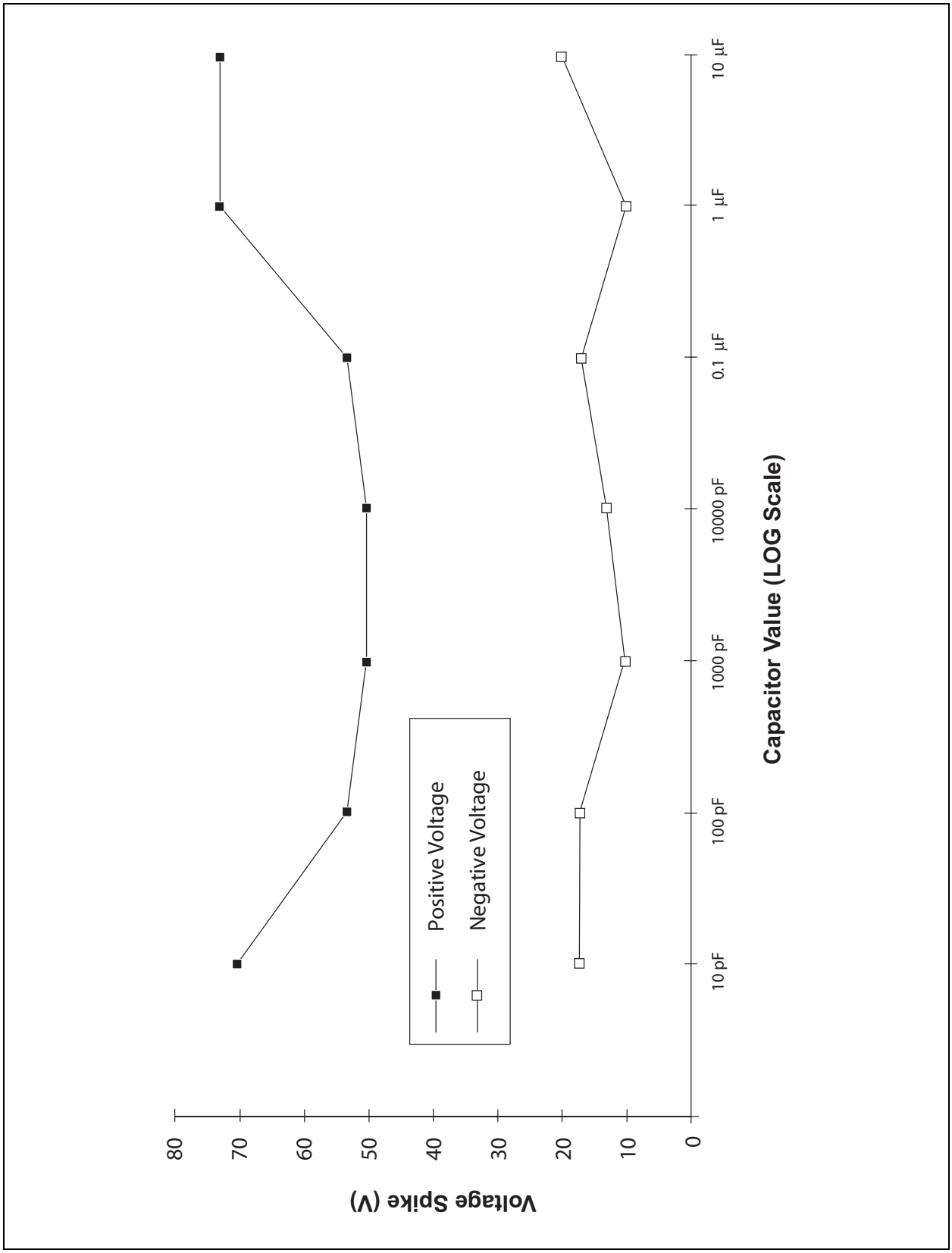


FIGURE 10: PIC16C54-XT PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON Vss. PROTECTION CAPACITOR BETWEEN Vss AND Vcc.

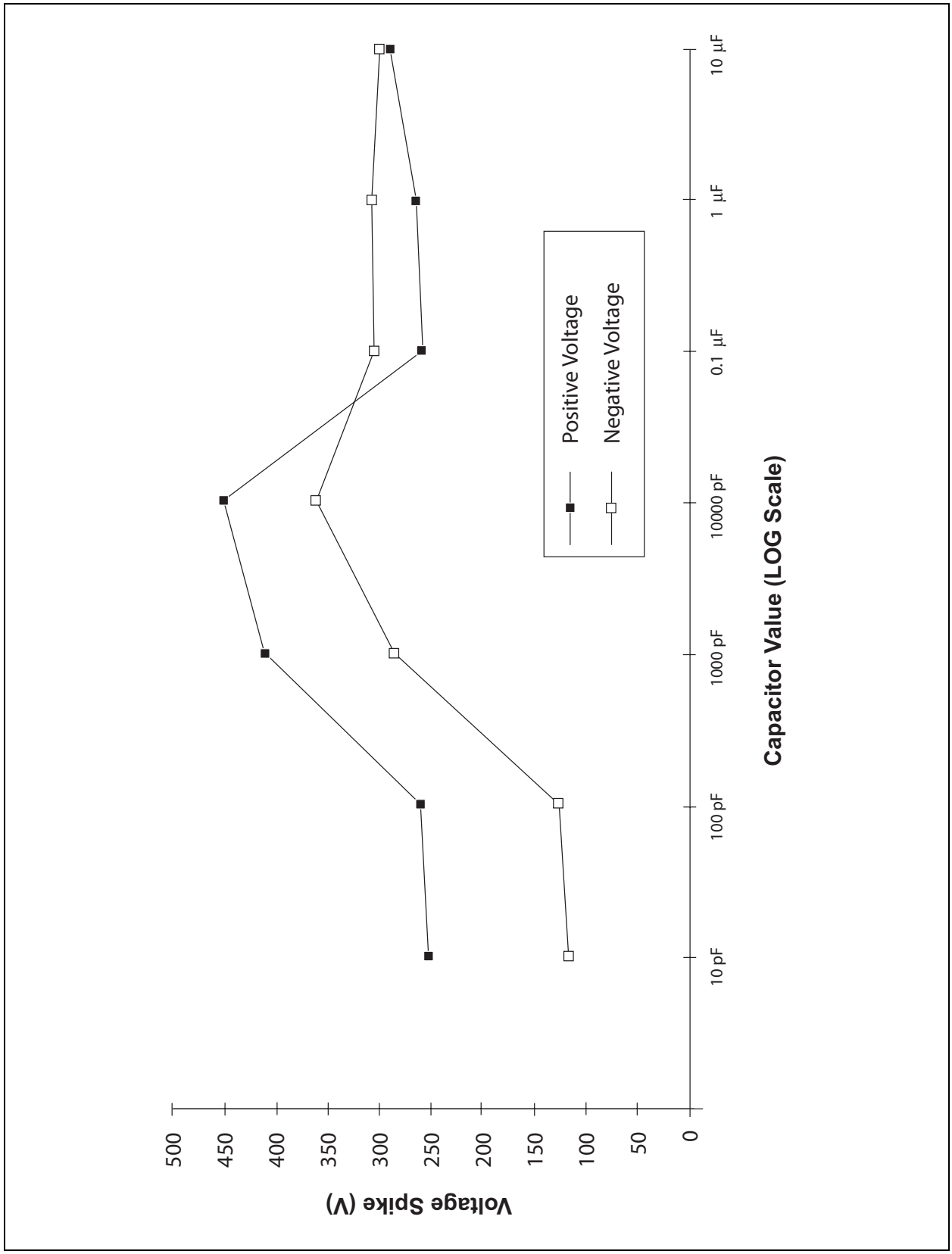


FIGURE 11: PIC16C54-XT PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON RB PORTS. PROTECTION CAPACITOR BETWEEN Vss AND Vcc.

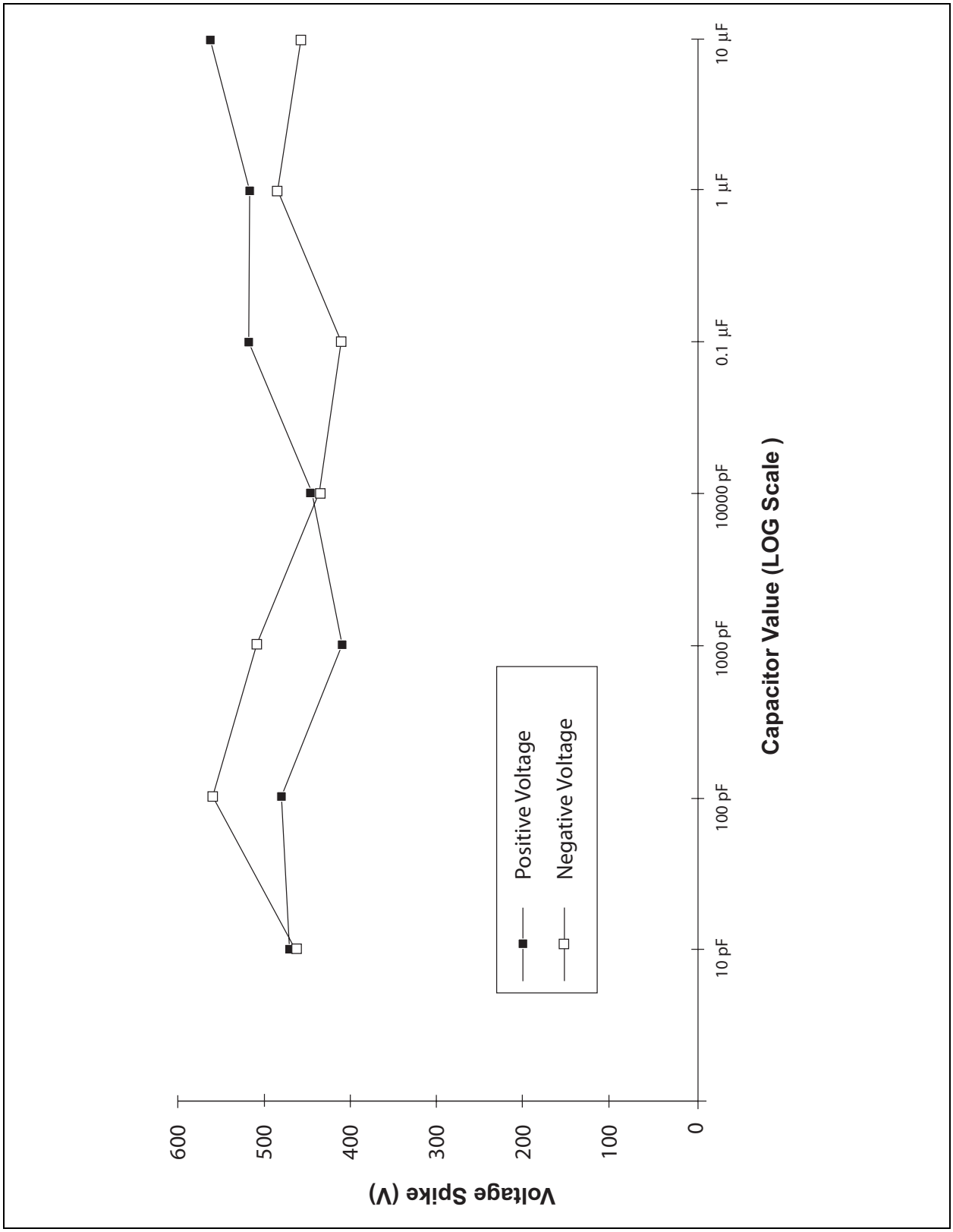


FIGURE 12: PIC16C54-XT PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON RA PORTS. PROTECTION CAPACITOR BETWEEN Vss AND Vcc.

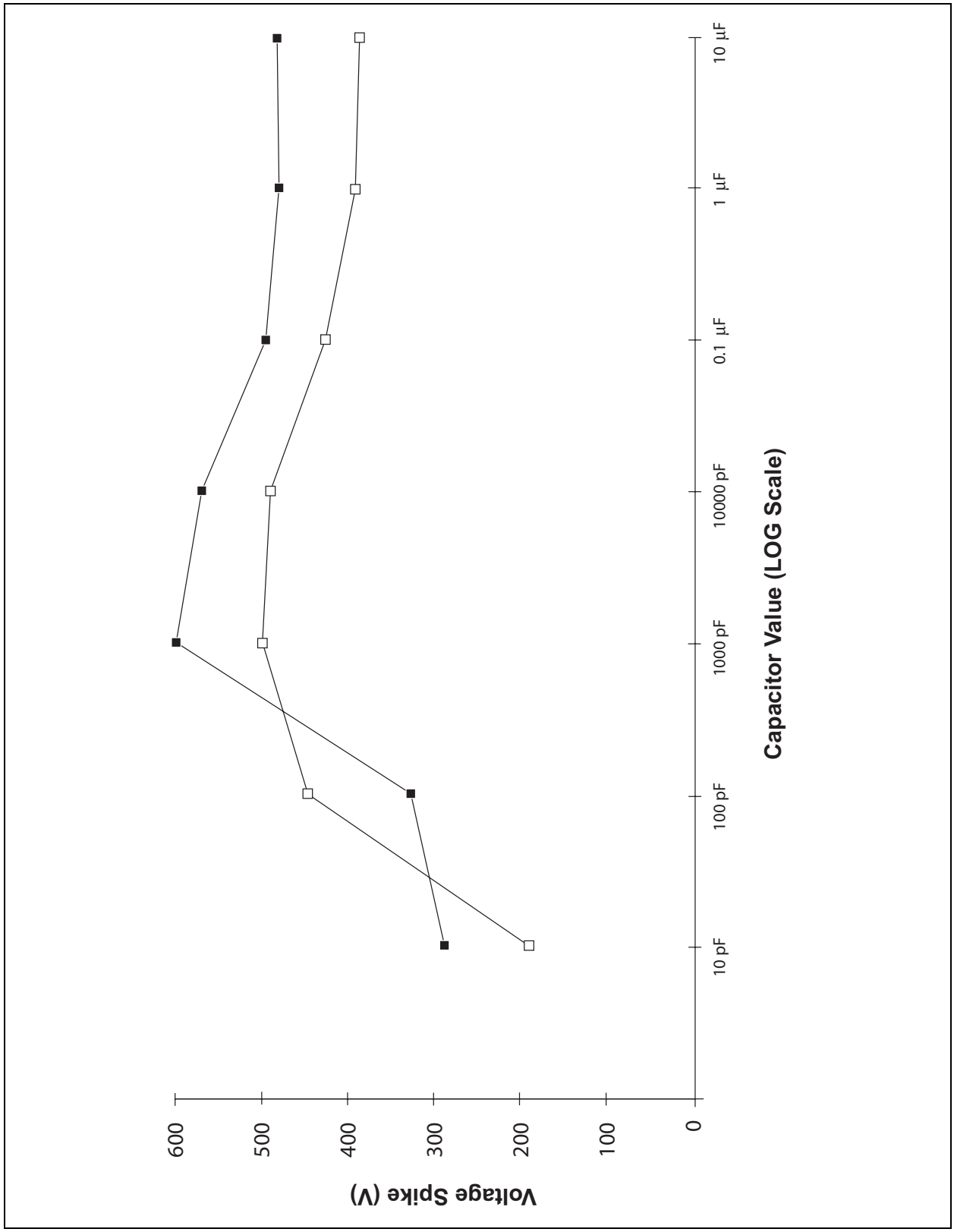


FIGURE 13: PIC16C54-XT PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON OSC1. PROTECTION CAPACITOR BETWEEN Vss AND Vcc.

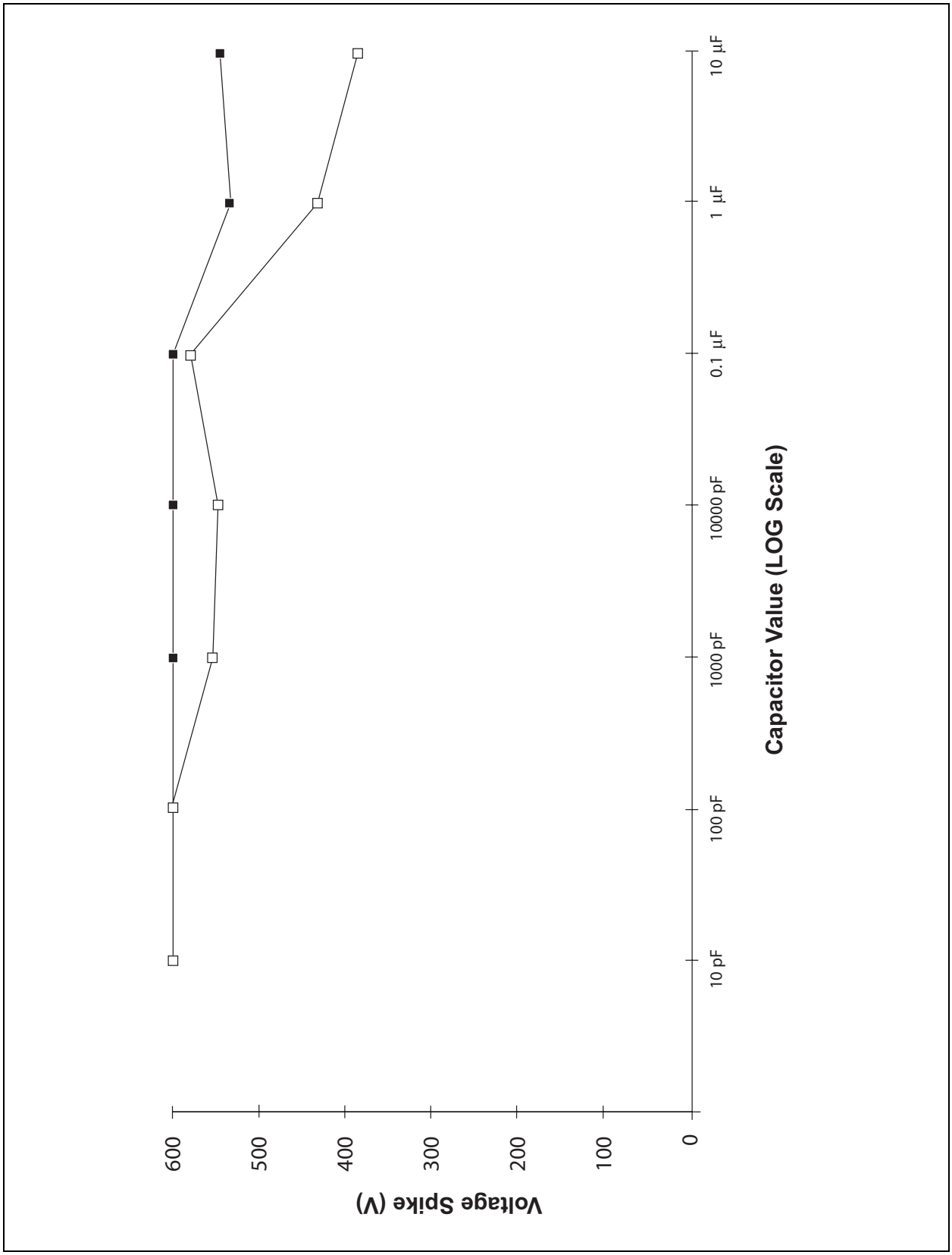


FIGURE 14: PIC16C54-XT PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON OSC2. PROTECTION CAPACITOR BETWEEN VSS AND VCC.

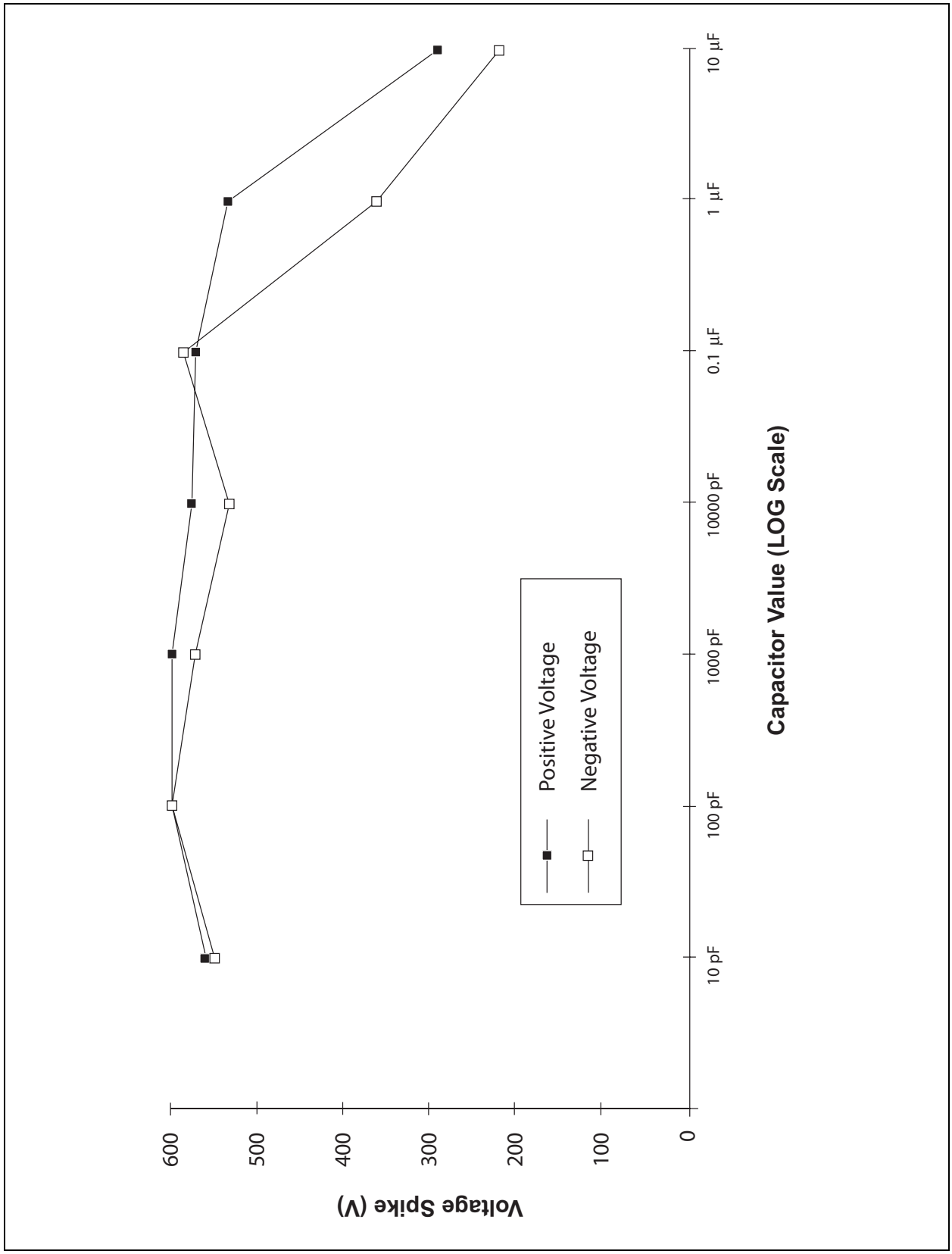


FIGURE 15: PIC16C54-XT PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON OSC1. PROTECTION CAPACITOR BETWEEN Vss AND Vcc.

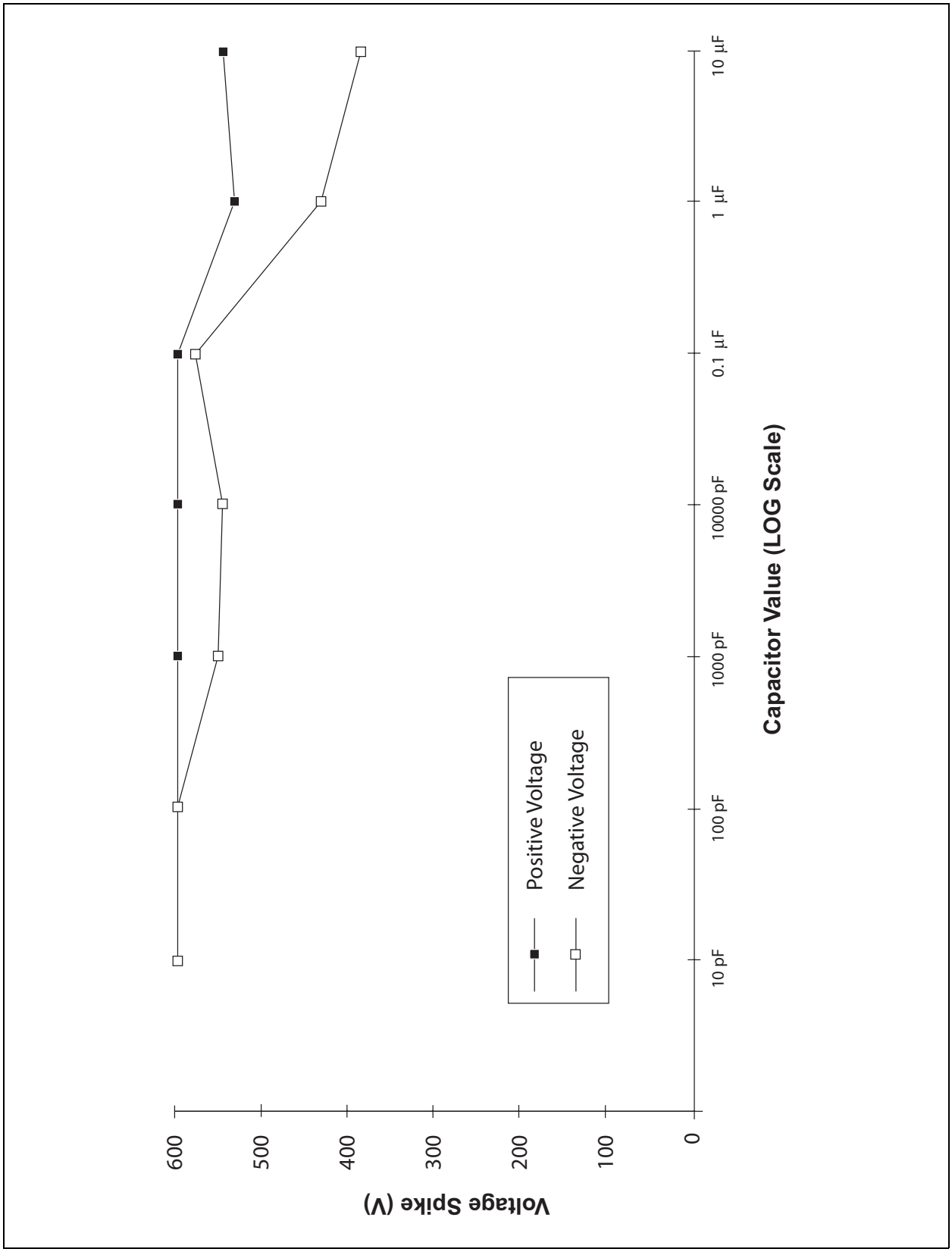


FIGURE 16: PIC16C54-XT PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON RA PORTS. PROTECTION CAPACITOR BETWEEN Vss AND Vcc.

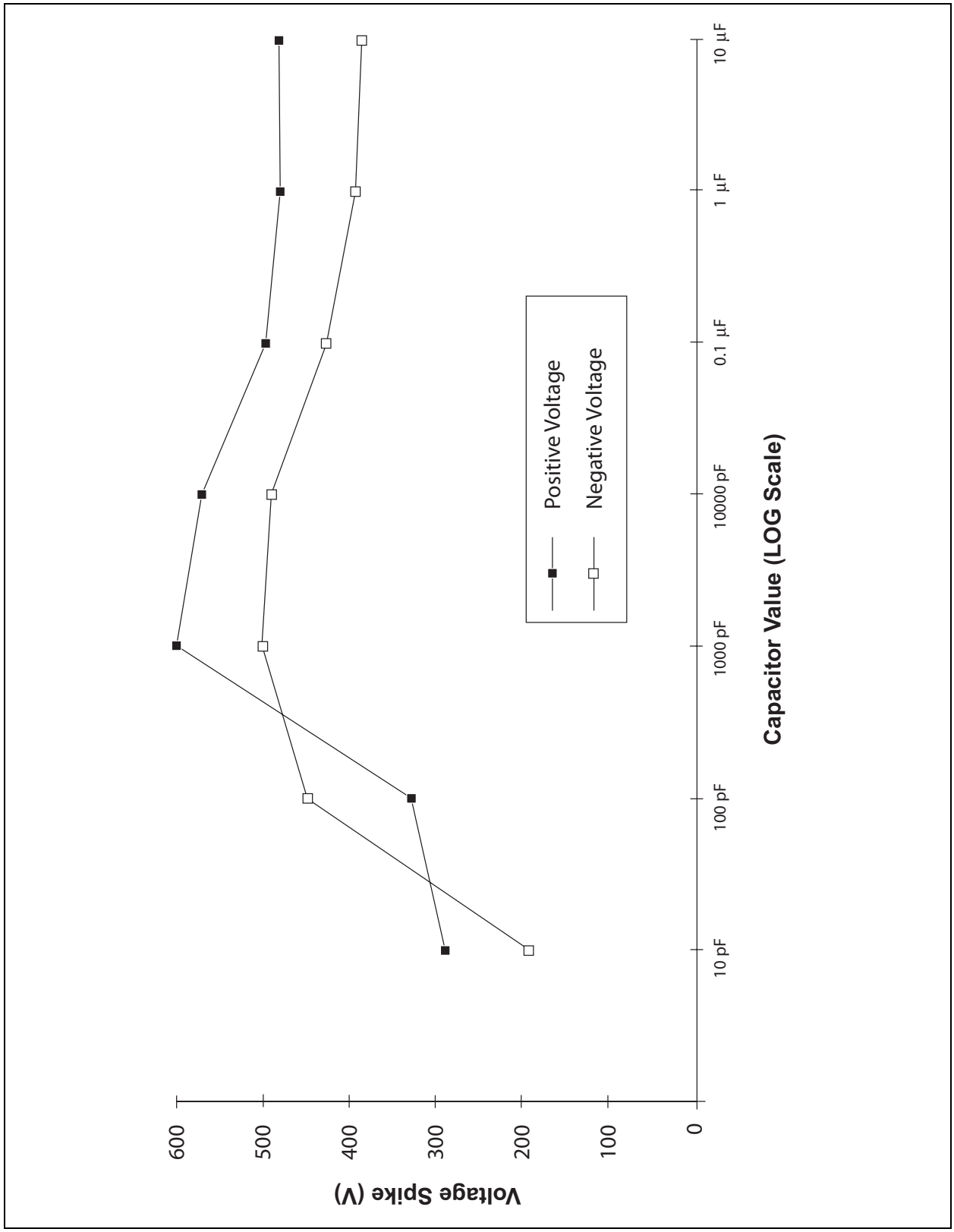
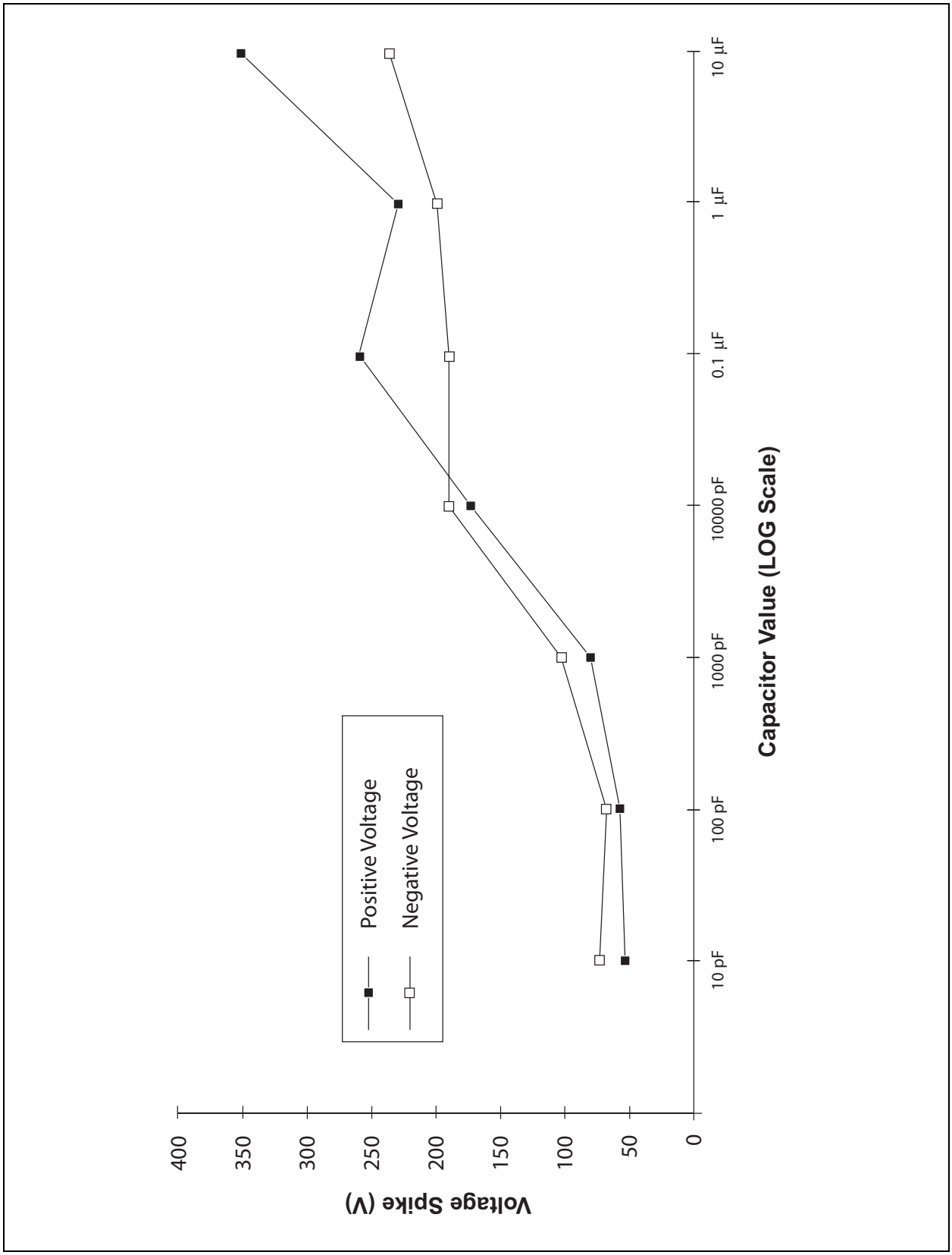


FIGURE 17: PIC16C54-XT PROTECTION LEVELS FOR ESD-INDUCED LATCH-UP WITH VOLTAGE SPIKE ON VCC. PROTECTION CAPACITOR BETWEEN VSS AND VCC.



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