Communicating With EEPROM In MTA85XXX

1.0 INTRODUCTION

The Microchip MTA85XXX family of microcontrollers are multichip modules which contain a PIC16C54A or PIC16C58A microcontroller and a Microchip Technology 24LC01B or 24LC02B EEPROM. This application note is intended to provide users with the most efficient code for 2C™-like communication between the EEPROM and the microcontroller in a PICSEE™ configuration, which will leave the user a maximum amount of code space and data RAM for the core application. The code contained in this application note will allow the PIC16C5XA microcontroller to act as the 2C master. The 24LC0XB EEPROM devices have 2C slave protocol implemented on-chip. Please refer to the Microchip Databook for further details on the 24LC0XB EEPROM. Note that this application note is optimized for use in either the PICSEE, or PIC16C5X plus EEPROM from Microchip. If a discrete PIC16C5X and generic serial EEPROM are to be used, refer to application note AN554 which details a complete 2C implementation.

The files which compose this application note (and their encapsulated post script print files) can be found on the Microchip BBS. The EEPROM communication code contained within this application note can be easily inserted into the users application code. The frequency of operation is assumed to be 4MHz and the code has been verified over the entire operating voltage range of the MTA85XXX. This code was tested with the fuse settings:

OSC = XT, WDT = ON, CP = OFF, CKSUM = 6715

2.0 OPERATION

2.1 General Operation

This application note will function with both bonding options of the MTA85XXX. Please refer to the MTA85XXX datasheet for further details. This application note will light LEDs on port B to indicate that the data is being written to the EEPROM or to output data read from the EEPROM.

The SDA and SCL bits of the EEPROM must be initialized to '1's before calling any of the EEPROM subroutines. This is done in the beginning of the MAIN routine. The start bit will not be initiated properly if these bits are not initialized prior to calling the EEPROM routines.

The registers EADDR and EDATA are used to communicate EEPROM address and data information to and from the EEPROM, as described below.

FIGURE 2-1 SCHEMATIC

NOTE: J1-2 Read EEPROM
2-3 Write EEPROM

J21-21k EEPROM (MTA85XXX1)
2-32k EEPROM (MTA85XXX2)
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2.2 Hardware Configuration
The schematic for this application note is located in figure 2-1. For the user’s application, the pins used for SDA and SCL can be easily redefined and the switches will not be necessary. This application example shows the MTA85XXX driving an array of LEDs to indicate writing to the EEPROM is in progress.

2.3 Switches for array size and to determine read/write
Bits RA0 and RA1 are used to determine if the user would like to read or write the array and to select the array size (1K or 2K). Bits RA2 and RA3 are used for SCL and SDA.
- RA0 = '0' for 1K EEPROM
- RA1 = '0' for read EEPROM
- RA0 = '1' for 2K EEPROM
- RA1 = '1' for write EEPROM

2.4 EEPROM Subroutines
The code in this application note is capable of performing byte writes, current address reads, and random address reads. The names of the subroutines are:
- Write_Byte: Write data supplied in register EEDATA at address supplied in register EEADD
- Read_Random: Read data into register EEDATA from address supplied in register EEADD
- Read_Current: Read data into register EEDATA from current address in EEPROM memory.

Note that the EEPROMs used in the MTA85XXX devices are also capable of page writes, however, page writes are not detailed by this application note. Refer to AN567 for details on page write.

2.5 Write_Byte Operation
During a Write_Byte operation the master will set address and data information into the EEADD and EEDATA registers. After receiving the acknowledge from the EEPROM that the current EEADD and EEDATA have been received, new values will be loaded into the EEADD and EEDATA registers. The EEPROM initiates a self timed write after the acknowledge, during which time it will not accept or acknowledge other input. The master falls into a loop trying to input the new address and data into the EEPROM. This loop will continue until the EEPROM finishes the self timed write and acknowledges receipt of the new address and data information.

This application note uses the 8-bit port B to provide an LED display. During a write, the LEDs should initialize to all ‘1’ and then set to ‘0’, 1 bit at a time, with each bit indicating that another 1/8th of the EEPROM array has been written. The entire operation takes less than 1 second after applying power or resetting the part. The data is initialized to FFH and the address to 00H. The address is incremented by 1 and the data decremented by 1 after each byte is written, until the EE array is full. An AAH is output to port B after the write has completed (actually as the last byte is writing).

2.6 Read_Current and Read_Random Operation
A read operation will attempt to read the data at the supplied or current address until an acknowledge is received. If an acknowledge is not received, the part will time out after a WDT period. If a Read_Random is being performed, the address is supplied in EEADD. If a Read_Current is being performed, the current address pointer inside the EEPROM is used. In both Read_Random and Read_Current the data is read into the EEDATA register.

2.7 Code Size
The total amount of program memory space required is 148 bytes. The major sections are as follows:
- EEPROM Subroutines: 71 bytes
- EEPROM Initialization: 4 bytes
- Read/Write Setup: 13 bytes
- Read Array: 27 bytes
- Write Array: 15 bytes
- 1 second timer: 14 bytes
- End of program loop: 4 bytes
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3.0 TIMINGS (ASSUME 4MHZ)
Detailed timing diagrams are given in Section 8.
Write operation will take approximately 350µs + standard write time (Figure 8-1).
Read random address operation will take approximately 350µs (Figure 8-2).
Read current address will take approximately 250µs (Figure 8-3).

4.0 I²C COMPATIBILITY
NOTE: Code is not strictly I²C compatible on all timing parameters, but is designed to work with a Microchip 24LC01B or 24LC02B EEPROM from 3 to 6.25 volts. Commented NOPs have been included which can be put in place to gain I²C timing compatibility. Also note that '1's are driven onto the bus (not floated) by the master in most write circumstances, except where bus contention from the EEPROM slave could result.

5.0 ASSEMBLY CODE LISTING
TITLE "APP-NOTE PER I²C-BUS"
LIST P=16C54 , C=132
;LIST P=PIC16C58  C=132
; PIC16C5X to 24LC01B or 24LC02B EEPROM communication code.
; Based on Franco code.
; Fuse settings:
; OSC = XT, WDT = ON, CP = OFF, CKSUM =

; Introduction:
; The Microchip MTA85XXX family of microcontrollers are multichip modules
; which contain a PIC16C5XX microcontroller and a 24LC01B or 24LC02B EEPROM. This application note is intended to provide users with highly compressed
; assembly code for communication between the EEPROM and the Microcontroller,
; which will leave the user a maximum amount of code space for the core
; application.

; For use in a users application, the file EEPROM.asm has been generated.
; This file contains the EEPROM subroutines and assembler constants used in
; these subroutines, stripped from this application note. Although the file
; cannot be compiled, it is available for easy insertion into the user's
; application code.

; EEPROM Subroutines:
; WriteByte - Write data supplied in EEDATA at address supplied in EEADD
; ReadRandom - Read data into EEDATA from address supplied in EEADD
; ReadCurrent - Read data into EEDATA from address currently in EEPROM

; Operation:
; For detailed operating information and other important information about
; this application note, read file AN571.doc

***************************************************************************
*************************** Variable Listing ****************************
***************************************************************************
OK          EQU     01H
NO          EQU     00H
;INDIRECT   EQU     00H         ; Indirect Address Register
;RTCLOCK    EQU     01H         ; Real time counter clock
PC          EQU     02H         ; Program counter
STATUS      EQU     03H         ; Status register
;PD         EQU     03H         ; Power down bit in STATUS
PORTA       EQU     05H         ; Port A control register
PORTB       EQU     06H         ; Port B control register
I2C_PORT    EQU     05H         ; Port A control register, used for I2C

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SCL EQU 02H ; EEPROM Clock, SCL (I/O bit 2)
SDA EQU 03H ; EEPROM Data, SDA (I/O bit 3)
EE_OK EQU 07H ; Bit 7 in PC_OFFSET used as OK flag for EE
PC_OFFSET EQU 07H ; PC offset register (low order 4 bits),
; value based on operating mode of EEPROM.
; Also, bit 7 used for EE_OK flag
EEADDR EQU 08H ; EEPROM Address
EEDATA EQU 09H ; EEPROM Data
EEBYTE EQU 0AH ; Byte sent to or received from
; EEPROM (control, address, or data)
COUNTER EQU 0BH ; Bit counter for serial transfer

ORG 0
GOTO START

;***********************************************************************
;***************************  EEPROM Subroutines  **********************
;***************************************************************************
; Communication for EEPROM based on I2C protocol, with Acknowledge.
;
; Byte_Write: Byte write routine
; Inputs:  EEPROM Address   EEADDR
;                EEPROM Data      EEDATA
; Outputs: Return 01 in W if OK, else return 00 in W
;
; Read_Current: Read EEPROM at address currently held by EE device.
; Inputs:  NONE
; Outputs: EEPROM Data       EEDATA
;                Return 01 in W if OK, else return 00 in W
;
; Read_Random: Read EEPROM byte at supplied address
; Inputs:  EEPROM Address    EEADDR
; Outputs: EEPROM Data       EEDATA
;                Return 01 in W if OK, else return 00 in W
;
; Note: EEPROM subroutines will set bit 7 in PC_OFFSET register if the
; EEPROM acknowledged OK, else that bit will be cleared. This bit
; can be checked instead of referring to the value returned in W
;***************************************************************************

;************************** Set up EEPROM control bytes ********************
;***************************************************************************
READ_CURRENT
MOVWF PC_OFFSET ; Load PC offset register, value preset in W
MOVLW B'10000000' ; Control byte with write bit, bit 0 = '0'
START_BIT
BCF I2C_PORT,SDA  ; Start bit, SDA and SCL preset to '1'

;******* Set up output data (control, address, or data) and counter ********
;***************************************************************************
PREP_TRANSFER_BYTE
PREP_TRANSFER_BYTE

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MOV LW .8 ; Counter to transfer 8 bits
MOVWF COUNTER

;*********** Clock out data (control, address, or data) byte ***********
;**********************************************************************
OUTPUT_BYTE
BCF I2C_PORT,SCL ; Set clock low during data set-up
RLF EEBYTE ; Rotate left, high order bit into carry bit
BCF I2C_PORT,SDA ; Set data low, if rotated carry bit is
SKPNC ; a '1', then:
BSF I2C_PORT,SDA ; reset data pin to a one, otherwise leave low
BSF I2C_PORT,SCL ; clock data into EEPROM
DECFSZ COUNTER ; Repeat until entire byte is sent
GOTO OUTPUT_BYTE

;************************** Acknowledge Check **************************
;***************************************************************************
MOVLW B'00001011' ; SDA = input, SCL = output
SKPNC ; if SDA = 1 then tristate port to allow
TRIS I2C_PORT ;   pullup to hold '1', avoiding bus contention
; if EEPROM acks in < 1us after clock goes low
BCF I2C_PORT,SCL ; Set SCL low, 0.5us < ack valid < 3us
TRIS I2C_PORT ; If SDA = '0' wait until SCL is low to set SDA to
;   input. If done above, could have sent STOP bit
; NOP ; May be necessary for SCL Tlow at low voltage,
; also give resistor time to pull up bus if last
; bit written = '0' and there is no ack from slave
BSF I2C_PORT,SCL ; Raise SCL, EEPROM acknowledge still valid
BTFSC I2C_PORT,SDA ; Check SDA for acknowledge (low)
BCF I2C_PORT,SCL ; Lower SCL, EEPROM release bus
BTFSS I2C_PORT,EE_OK ; If no error continue, else stop bit
GOTO STOP_BIT

;***** Set up program counter offset, based on EEPROM operating mode *****
;**********************************************************************
INIT_ADDRESS
INCF PC_OFFSET ; Increment PC offset to 2 (write) or to 4 (read)
MOVF EEADDR,W ; Put EEPROM address in W, ready to send to EEPROM
GOTO PREP_TRANSFER_BYTE

INIT_WRITE_DATA
INCF PC_OFFSET ; Increment PC offset to go to STOP_BIT next
MOVF EEDATA,W ; Put EEPROM data in W, ready to send to EEPROM
GOTO PREP_TRANSFER_BYTE

INIT_READ_CONTROL
BSF I2C_PORT,SCL ; Raise SCL
INCF PC_OFFSET ; Increment PC offset to go to READ_BIT_COUNTER next
MOVLW B'10100001' ; Set up read control byte, ready to send to EEPROM
GOTO START_BIT ; bit 0 = '1' for read operation

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;***********************************************************  Read EEPROM data ***********************************************************
;***********************************************************
READ_BIT_COUNTER
    MOVlw .8 ; Set counter so 8 bits will be read into EEDATA
    MOVwf COUNTER

READ_BYTE
    BSF I2C_PORT,SCL ; Raise SCL, SDA valid. SDA still input from ack
    SETC ; Assume bit to be read = 1
    BTFSS I2C_PORT,SDA ; Check if SDA = 1
    ClRC ; if SDA not = 1 then clear carry bit
    RLF EEDATA ; rotate carry bit (=SDA) into EEDATA;
    BCF I2C_PORT,SCL ; Lower SCL
    DecFSz COUNTER ; Decrement counter
    GOTO READ_BYTE ; Read next bit if not finished reading byte

;******************************************************************************
;******************  Generate a STOP bit and RETURN  ******************************
;******************************************************************************
STOP_BIT
    BCF I2C_PORT,SDA ; SDA=0, on TRIS, to prepare for transition to '1'
    MOVlw B'00000011' ; SDA and SCL set to outputs, Bit0 and Bit1 ' input
    TRIS I2C_PORT
    BSF I2C_PORT,SCL ; SCL = 1 to prepare for STOP bit
    NOP ; 4 NOPs necessary for I2C spec Ts =sto = 4.7us
    BSF I2C_PORT,SDA ; Stop bit, SDA transition to '1' while SCL high
    BTFSS PC_OFFSET,EE_OK ; Check for error
    RETlw NO ; if error, send back NO
    RETlw OK ; if no error, send back OK

;  Note: SDA and SCL still being driven by master, both set to outputs.
;******************************************************************************
;***********************************************************  End EEPROM Subroutines ***********************************************************
;***********************************************************

;****************************************************************************
;*****************************  MAIN routine  *******************************
;****************************************************************************
START
;***********************************************************
;**************** Initialize EEPROM ****************
;***********************************************************

MOVLw B'00000011' ; SDA and SCL = output, Bit0 and Bit1 = input
TRIS I2C_PORT
BSF I2C_PORT,SCL ; Initialize SCL and SDA to '1'
BSF I2C_PORT,SDA

;*** VARIABLE FOR MAIN ROUTINE THAT ARE NOT USED IN EEPROM SUBROUTINES ****
;***************************************************************************
COUNT EQU 0CH ; REGISTER FOR # OF BYTES IN ARRAY WRITTEN OR READ
LEDS EQU 0DH ; REGISTER TO HOLD DATA TO OUTPUT TO PORT
TIMER_DL EQU 0EH ; REGISTER FOR OUTER LOOP VARIABLE FOR TIMER
TIMER_DL EQU 0FH ; REGISTER FOR MIDDLE LOOP VARIABLE FOR TIMER
EE1KPARTIAL EQU 10H ; REGISTER INNER LOOP VARIABLE FOR TIMER
EE2KPARTIAL EQU 12H ; 1/8TH OF 1K ARRAY (128 BYTES TOTAL)
EE2KFULL EQU 00H ; 1/8TH OF 2K ARRAY (256 BYTES TOTAL)
EE1KFULL EQU 00H ; 1/8TH OF 1K ARRAY (128 BYTES TOTAL)
SIZE EQU 00H ; BIT0 ON PORT WILL BE READ TO DETERMINE ARRAY SIZE
READORWRITE EQU 01H ; BIT1 ON PORT WILL BE READ TO DETERMINE IF USER
                   ; WANTS TO READ OR WRITE THE ARRAY
EEVDD EQU 07H ; BIT FOR EEPROM VDD ON MTA85MX DEVICES

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;***************************************************************************
;****************************  Read / Write Set-Up ******************************
;***************************************************************************

    ;***************************************************************************
    ; **********************  Read / Write  Set-Up  *****************************
    ;***************************************************************************

    MOVLW 000H
    TRIS PORTB          ; PORTB = OUTPUT
    MOVWF EEADDR        ; 1ST ADDRESS = 00H
    MOVLW 0FFH          ; INITIALIZE DATA TO 'FF'
    MOVWF LEDS          ; INITIALIZE PORTB OUTPUT FOR % DONE INDICATOR
    MOVWF PORTB         ; SET PORT B TO ALL '1's
    MOVWF EEDATA        ; INITIALIZE DATA TO ALL '1'
    BTFSS PORTA,READORWRITE ; IF RA1 = '1' THEN WRITE, RA1 = '0' THEN READ
    GOTO SETSIZE_READ

SET_SIZE

    MOVLW EE1KPARTIAL   ; INIT COUNTER TO 1/8 OF ARRAY SIZE, 1K
    BTFSC PORTA,SIZE    ; IF RA0 = '0' THEN 1K EEPROM, IF '1' THEN 2K
    MOVLW EE2KPARTIAL   ; INIT COUNTER TO 1/8 OF ARRAY SIZE, 2K
    MOVWF COUNT

    ;****************************  Write Array  ********************************
    ;***************************************************************************

CALL_WRITE

    CALL WRITE_BYTE
    CLRWDT              ; DON'T TIME OUT DURING EE OPERATIONS
    BTFSS PC_OFFSET,EE_OK ; TEST EE_OK BIT DETERMINED DURING ACK CHECK
    GOTO CALL_WRITE      ; IF NO ACKNOWLEDGE, ASSUME PART IS STILL
    INCF EEADDR         ; WRITING AND KEEP TRYING UNTIL GET THROUGH.
    DECF EEDATA         ; IF PART DOES ACK, CHANGE DATA AND ADDRESS
    DECFSZ COUNT        ; EVERY 1/8TH OF ARRAY CHANGE OUTPUT LEDs
    GOTO CALL_WRITE

;    *******  UPDATE LED OUTPUTS TO INDICATE ARRAY BEING WRITTEN *******

    BTFSS LEDS,06H      ; IF BIT6 IS CLEAR BEFORE SHIFT THEN ARRAY IS
    GOTO INFINTELOOP    ; FINISHED WRITING (EXCEPT LAST BYTE STILL NOT
    RLF LEDS            ; DON'T CLEAR BIT7 OR MTA85X1X PRODUCTS
    INCF EEDATA         ; WILL LOSE THEIR VDD AND NOT FINISH LAST BYTE
    BCF STATUS,0        ; SET CARRY BIT TO '0'
    MOVF LEDS,W
    MOVWF PORTB
    GOTO SET_SIZE

    ;****************************  Timer 1-second  ******************************
    ;***************************************************************************

TIMER

    MOVLW .107
    MOVWF TIMER_DL
    OUTER_LOOP
    CLRWDT
    MOVLW .25
    MOVWF TIMER_ML
    MIDDLE_LOOP
    MOVLW .123
    MOVWF TIMER_IL
    INNER_LOOP
    DECFSZ TIMER_IL
    GOTO INNER_LOOP
    DECFSZ TIMER_ML
    GOTO MIDDLE_LOOP
    DECFSZ TIMER_DL
    GOTO OUTER_LOOP
    RETLW 00H

;***************************************************************************
;****************************  Read Array  ************************************
Communicating With EEPROM In MTA85XXX

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
SETSIZE_READ
MOVLW EE1KFULL ; INIT COUNTER TO ARRAY SIZE, 1K
BTFSC PORTA,SIZE ; IF RA0 = '0' THEN 1K EEPROM, IF '1' THEN 2K
MOVLW EE2KFULL ; INIT COUNTER TO ARRAY SIZE, 2K
MOVWF COUNT
CALL_READ_RANDOM
CALL_READ_CURRENT
BTFSS PC_OFFSET,EE_OK ; TEST EE_OK BYTE DETERMINED DURING ACK CHECK
GOTO CALL_READ_RANDOM ; IF NO ACKNOWLEDGE, TRY AGAIN UNTIL RESET.
INCF EEADDR
MOVF EEDATA,W
MOVWF PORTB
CALL TIMER ; SLOW DOWN OUTPUT SO IT IS READABLE ON LEDs
BSF PORTB,EEVDD ; Always set RB7 to '1' for MTA85X1X devices
DECFSZ COUNT ; May see flash on LED. If rise time is
to slow, EEPROM may not be powered-up yet
GOTO CALL_READ_RANDOM ; RESET SIZE_READ
MOVLW EE1KFULL ; INIT COUNTER TO ARRAY SIZE, 1K
BTFSC PORTA,SIZE ; IF RA0 = '0' THEN 1K EEPROM, IF '1' THEN 2K
MOVLW EE2KFULL ; INIT COUNTER TO ARRAY SIZE, 2K
MOVWF COUNT
CALL_READ_CURRENT
CALL_TIMER ; SLOW DOWN OUTPUT SO IT IS READABLE ON LEDs
BSF EEDATA,EEVDD ; Always set RB7 to '1' for MTA85X1X devices
MOVWF PORTB ; or EEPROM internal address will be reset
DECFSZ COUNT
GOTO CALL_READ_CURRENT
; NOTE: Data observed on port B will always show a '1' regardless of what
; was read. MTA85X1X pinout devices (RB7=SVDD) will reset the EEPROM
; internal address pointer if RB7 = 0. If the user has the MTA85X0X
; pinout, the BSF EEDATA,EEVDD line above can be commented out.
;----------------------------------------------------------------------
; End of Program Loop
INFINITELOOP
MOVLW 0AAH ; NOTE: Bit7 = '1' to let EEPROM finish writing, MTA85X1X
MOVWF PORTB
CLRWDT
GOTO INFINITELOOP
;----------------------------------------------------------------------
; End MAIN
END
6.0 TIMING DIAGRAMS

FIGURE 6.1 WRITE_BYTE

WRITE_BYTE

Output Byte: Bit 0
9us / bit

Output Byte: Bit 7

Initalize SCL
and SDA

Stop Bit

PC_Offset
Set-up

Prep

Transfer

Byte

Prep

Transfer

Byte

Output Byte: Bit 1

WRITE_BYTE 5us

Strobe SDA

Prep

Transfer

Byte

If Acknowledge Check OK:
after sending control byte
and after sending address

If Acknowledge Check OK:
after writing data

Start Bit

0x0

PC_Offset
Set-up

Prep

Transfer

Byte

If no acknowledge

Prep

Transfer

Byte

SCL

SDA

Set-Up PC

Stop Bit

Init Add
or
Init_Write_Data

Goto

Output Byte Bit 0

Output Byte Bit 1

Output Byte Bit 2

Output Byte Bit 3

Output Byte Bit 4

Output Byte Bit 5

Output Byte Bit 6
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FIGURE 6.2 READ_RANDOM

- **Output Byte:** Bit 0
- **Output Byte:** Bits 2 - 6
- **Output Byte:** Bit 7
- **Acknowledge Check**
- **Output Byte:** Bit 8
- **Stop Bit**
- **Set-Up PC**
- **Prep Transfer Byte**
- **Transfer Byte**
- **PC_Offset**
- **Set-up**
- **Transfer Byte**

- **Start Bit**
- **Stop Bit**
- **Acknowledge Check OK:** after sending address
- **Acknowledge Check OK:** after sending control byte
- **Acknowledge Check OK:** after sending control byte

- **FIGURE 6.2 READ_RANDOM**
Communicating With EEPROM In MTA85XXX

FIGURE 6.2 READ_RANDOM (CONTINUED)

READ RANDOM

(continued)

STOP BIT

READ BYTE: BIT 0

READ BYTE: BIT 1

READ BYTE: BITS 2 - 6

9us / bit

READ BYTE: BIT 7

ACKNOWLEDGE CHECK

SET-UP PC

IF ACKNOWLEDGE CHECK OK:

BYTE

BIT 0

GOTO

AFTER SENDING READ CONTROL

READ BIT COUNTER

STOP BIT

READ BYTE: BIT 0

READ BYTE: BIT 1

READ BYTE: BITS 2 - 6

9us / bit

READ BYTE: BIT 7

ACKNOWLEDGE CHECK

SET-UP PC
FIGURE 6.3 READ_CURRENT

Initalize SCL and SDA

Start Bit

PC Offset

Init_Read

Control

Stop Bit

Output Byte: Bit 0

Output Byte: Bit 1

9us / bit

344x239
Strobe
Read Byte: Bit 0

Acknowledge Check: OK
after sending read control

Read Byte: Bit 1

Acknowledge Check

If no acknowledge

Acknowledge

Stop Bit

Bit 7

9us / bit

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Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company’s quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001 certified.

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