AN522

Power-up Considerations

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INTRODUCTION

When powering up any microcontroller it is necessary for the power supply voltage to traverse voltage ranges, where the device is not guaranteed to operate, before the power supply voltage reaches its final state. Since some circuits on the device (logic) will start operating at voltage levels lower than other circuits on the chip (memory), the device may power-up in an unknown state. To guarantee that the device starts up in a known state, it must contain a power-up reset circuit. PIC16C5X microcontrollers are equipped with on-chip Power-on Reset circuitry, which eliminates the need for external reset logic. This circuit will function in most power-up situations where VDD rise time is fast enough (50 ms or less). This application note describes the typical power-up sequence for PIC16C5X microcontrollers. Methods of assuring reset on power-up and after a brown-out are discussed and simple, low-cost external solutions are discussed for power-up situations where the PIC16C5X's internal circuitry cannot provide the reset.

POWER-UP SEQUENCE

The PIC16C5X incorporates complex Power-on Reset (POR) circuitry on-chip which provides a solid, reliable internal chip reset for most power-up situations. To use this feature, the user merely needs to tie the $\overline{MCLR}$ pin to the VDD pin. A simplified block diagram of the on-chip reset circuitry is shown in Figure 1. On power-up, the reset latch and the start-up timer are reset to appropriate states by the Power-on Reset (POR). The start-up timer will begin counting once it detects $\overline{MCLR}$ to be high (i.e., external chip reset goes inactive). After the time-out period, which is typically 18 ms long, the timer will reset the reset latch and thus end the on-chip reset signal.

Figure 3 and Figure 4 are two power-up situations with relative fast rise time on VDD. In Figure 2, VDD is stable when $\overline{MCLR}$ is brought high (i.e., reset pulse is being provided by external source). The chip actually comes out of reset about TOST ms after that, where TOST = Time of the Oscillator Start-up Timer. (The timer is called Oscillator Start-up Timer because the time-out was incorporated primarily to allow the crystal oscillator to stabilize on power-up). In Figure 3, the $\overline{MCLR}$ and VDD are tied together and clearly the on-chip reset mechanism is being used. VDD is stable before the start-up timer expires and there is no problem with proper reset.

In Figure 4, where the VDD rise time is much greater than TOST (typically 18 ms) this is clearly a potentially problematic situation. The POR pulse comes when VDD is about 1.5V. Most CMOS logic, including the start-up timer, starts functioning between 1.5V to 2.0V. When the start-up timer times out, the chip reset is ended and the chip attempts to execute. If by this time VDD has reached the VDD min. value, then all circuits are guaranteed to function correctly and power-up reset is successful. If, however, the VDD slope was too slow and had not reached VDD min., then the chip is not guaranteed to function properly.

FIGURE 1: PIC16C5X INTERNAL RESET CIRCUIT

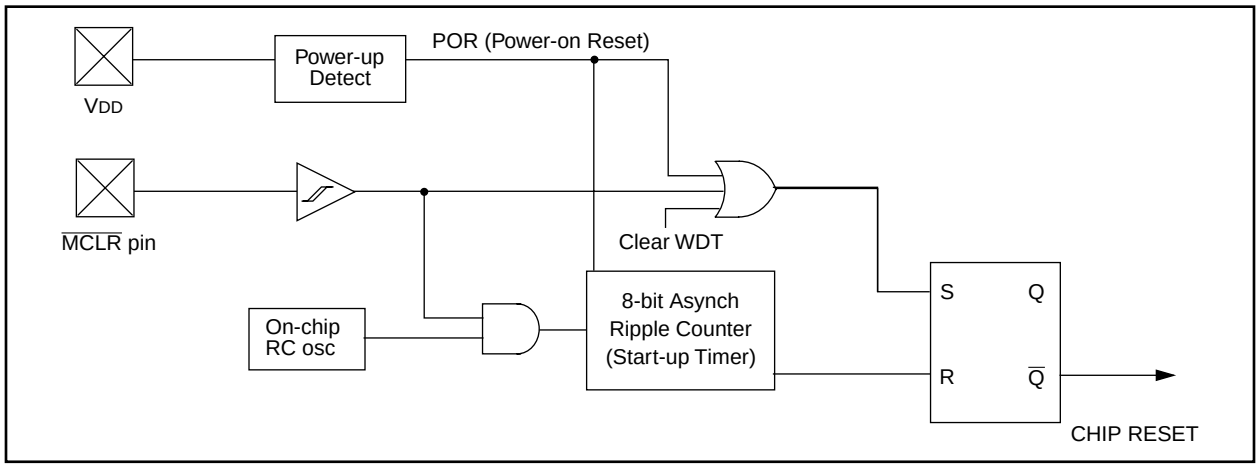


FIGURE 2: EXTERNAL RESET PULSE

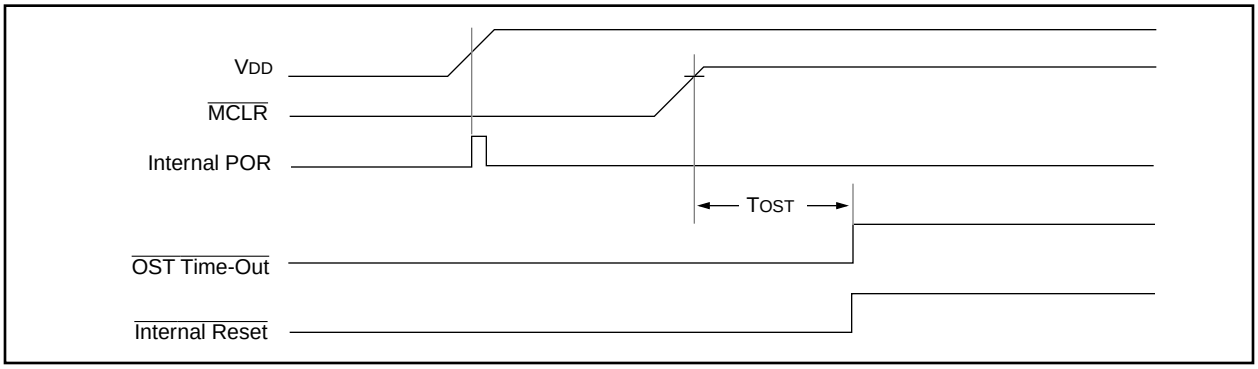


FIGURE 3: INTERNAL RESET (VDD AND MCLR TIED TOGETHER)

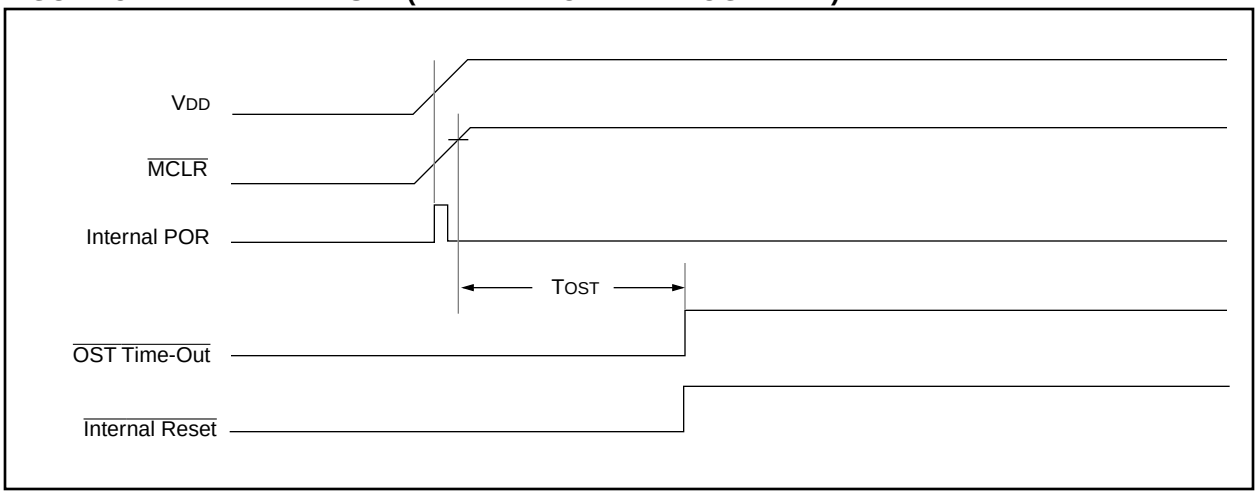
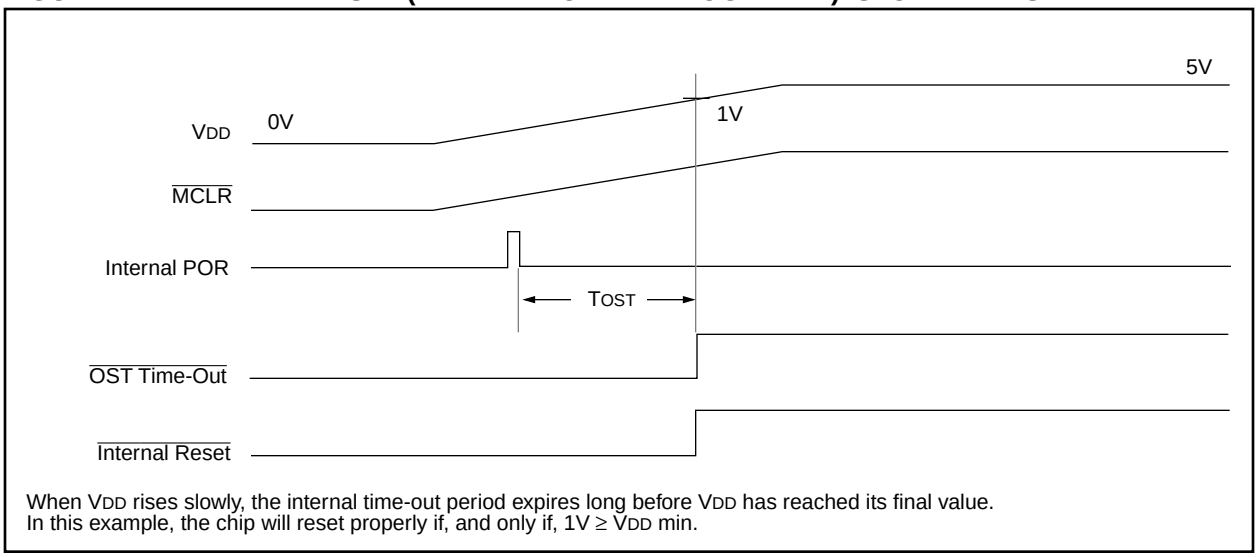


FIGURE 4: INTERNAL RESET (VDD AND MCLR TIED TOGETHER): SLOW VDD RISE TIME

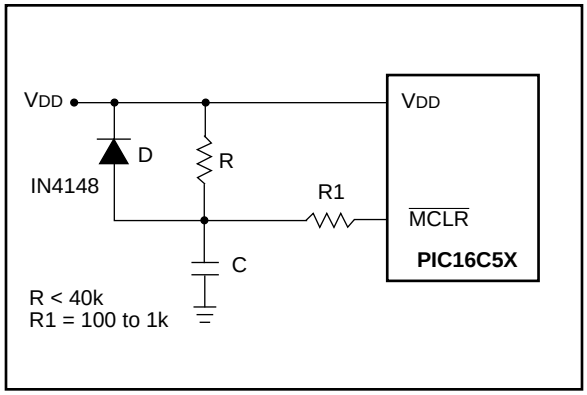


When VDD rises slowly, the internal time-out period expires long before VDD has reached its final value.
In this example, the chip will reset properly if, and only if, 1V ≥ VDD min.

EXTERNAL POWER-ON RESET CIRCUIT

To use power supplies with slow rise times it is necessary to use an external power-on reset circuit such as the one shown in Figure 5. This circuit uses an external RC to generate the reset pulse. The time constant of the RC should be long enough to guarantee that the reset pulse is still present until VDD has reached VDD min. R should be 40k or less to guarantee that $\overline{MCLR}$ will pull to within 0.2 volts of VDD (since the leakage spec on $\overline{MCLR}$ is ±5 µA, a resistor larger than 40k may cause input high voltage on this pin to be less than VDD – 0.2V, the required spec). The diode *(D)* is used to rapidly discharge the capacitor on power-down. This is very important as a power-up reset pulse is needed after a short power-down (less than the time constant of RC) or after a power spike. The resistor *(R1)* protects against a high current flowing into the *$\overline{MCLR}$* pin from fully charged capacitor *(C)*, in the event the $\overline{MCLR}$ pin breakdown is induced via ESD (electrostatic discharge) or EOS (electrical overstress). The circuit, however, does not protect against brown-out situations where power does not drop to zero, but merely dips below VDD min. In such a situation, voltage at the $\overline{MCLR}$ pin will not go low enough (i.e., below VIL) to guarantee a reset pulse. The following section presents an example circuit to protect against such brown-outs.

FIGURE 5: EXTERNAL POWER-ON RESET CIRCUIT



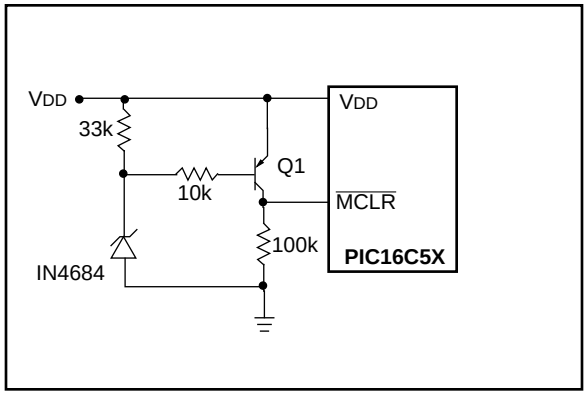
BROWN-OUT PROTECTION

In many applications it is necessary to guarantee a reset pulse whenever VDD is less than VDD min. This can be accomplished using a brown-out protection circuit such as the one shown in Figure 6. This is a simple circuit that causes a reset pulse whenever VDD drops below the zener diode voltage plus the VBE

$$V_{BE} = V_{DD} \bullet R1 / (R1 + R2)$$

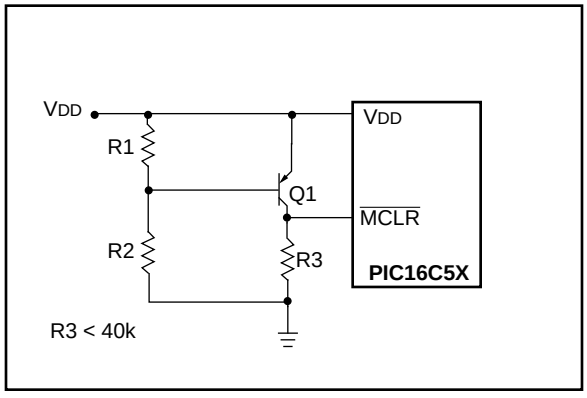
of *Q1*. A 3.3V zener will produce a reset pulse whenever VDD drops below about 4V. This circuit has a typical accuracy of about ±100 mV.

FIGURE 6: EXTERNAL BROWN-OUT PROTECTION CIRCUIT



A less expensive, albeit less precise, brownout circuit is shown in Figure 7. Transistor *Q1* turns off when VBE falls below 0.7V allowing *R3* to pull down the $\overline{MCLR}$ input.

FIGURE 7: EXTERNAL BROWN-OUT PROTECTION CIRCUIT



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