AN246

Driving the Analog Inputs of a SAR A/D Converter

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INTRODUCTION

Driving any A/D Converter (ADC) can be challenging if all issues and trade-offs are not well understood from the beginning. With Successive Approximation Register (SAR) ADCs, the sampling speed and source impedance should be taken into consideration if the device is to be fully utilized. In this application note we will delve into the issues surrounding the SAR Converter's input and conversion nuances to insure that the converter is handled properly from the beginning of the design phase. We will also review the specifications available in most A/D Converter data sheets and identify the important specifications for driving your SAR. From this discussion, techniques will be explored which can be used to successfully drive the input of the SAR A/D Converter. Since most SAR applications require an active driving device at the converter's input, the final subject will be to explore the impact of an operational amplifier on the analog-to-digital conversion in terms of DC as well as ac responses.

A typical system block diagram of the SAR converter application is shown in Figure 1. Some common SAR converter systems are Data Acquisition Systems, Transducers Sensing Circuits, Battery Monitoring applications and Data Logging. In all of these systems, DC specifications are important. Additionally, the required conversion rate is relatively fast (as compared to Delta-Sigma converters) and having a lower number of bits that are reliably converted is acceptable.

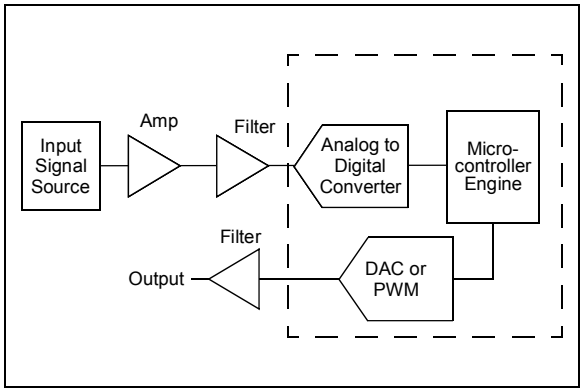


FIGURE 1: *Block diagram of an application that has a SAR ADC in the signal path.*

For the converter shown in Figure 1, the input signal could be ac, DC or both. The operational amplifier is used for gain, impedance isolation and its drive capability. A filter of some sort (passive or active) is needed to reduce noise and to prevent aliasing errors.

The ADC in Figure 1 could be external or, in the case of a SAR converter, internal to the microcontroller. The DAC / PWM block can be implemented internally or externally to the microcontroller as well. This function is used to drive actuators, values, etc. A filter following the DAC / PWM function is usually required to perform a smoothing function. This filter would reduce glitch errors, quantization errors and provide drive or isolation to the actuator. In this discussion we will focus on the input section to the A/D Converter.

BASIC OPERATION OF THE SAR ADC

With the SAR ADC, the input signal should be considered in the DC as well as ac domain. This is true even if you are only interested in a DC response.

DC Errors of the SAR ADC

The offset and gain errors of an ADC can be easily calibrated out of the resulting data using the microcontroller at the output of the converter. But the more difficult DC errors to calibrate out would be Integral Non-Linearity (INL) and Differential Non-Linearity (DNL). In most systems, these errors manifest themselves as incorrect conversions or noise. Of the two specifications, INL is the "Holy Grail" of DC specifications because it describes the entire transfer function. INL is a measure of how close to actual the transition points are to the ideal transfer function. This is a difficult error to calibrate out with a microcontroller because every code needs to be evaluated for proper calibration and this error differs from device to device.

While noise is usually not a topic for DC accuracy, in this case it has merit. It is important to realize that the SAR ADC operates in the frequency domain. This is true even though you may think that you are measuring near DC signals. If there is a noise source in the system, the "DC" conversion from sample-to-sample may not be the same. This phenomena is reduced by using anti-aliasing filters. When digitizing AC signals, other characteristics of the converter come into play. These characteristics include distortion of the input signal and noise levels. Anti-aliasing filters are also useful for these type of problems.

Basic SAR ADC Operation

At the input of a SAR ADC, the signal first sees a switch and a capacitive array, as shown in Figure 2. The capacitors in this array are all connected to each other with the input signal node on one side and the non-inverting input to a comparator on the other.

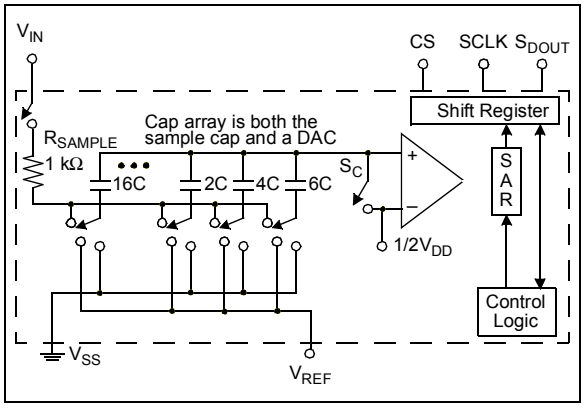


FIGURE 2: *Model of the MCP320X 12-Bit ADC.*

Once the input signal has been sampled to the internal capacitive array of the converter, the switch is open and the bottom side of the MSb capacitor is connected to V_{REF}, while the other capacitors are tied to V_{SS} (or the system ground). With this action, the charge from the MSb capacitor is redistributed among the other capacitors. The non-inverting input of the comparator moves up or down in voltage according to the way the charge is distributed. The voltage at the non-inverting input of the comparator, with respect to V_{SS}, is equal to (1/2 V_{DD} -V_{IN}) + 1/2 V_{REF}. If this voltage is greater than 1/2 V_{DD}, an MSb equal to zero is transmitted out of the serial port synchronized with SCLK through S_{DOUT} and the MSb capacitor is left tied to V_{REF}. If this voltage is less than 1/2 V_{DD}, a MSb bit equal to one is transmitted out of the serial port and the MSb capacitor is connected to V_{SS}.

With the determination of the value of the MSb, the converter then examines the MSb-1 value. This is done by connecting the MSb-1 capacitor to V_{REF}, while the other capacitors are tied to V_{SS} (except for the MSb capacitor). Since you will note that the MSb-1 capacitor is not illustrated in Figure 2, its value is 8C. With this action, the value of the voltage at the non-inverting input of the comparator is [1/2 V_{DD} - V_{IN}] + 1/2 V_{REF} (MSb) + 1/4 V_{REF}. Once again, a comparison of this voltage to 1/2 V_{DD} is performed with the comparator. In this analysis, if this voltage is greater than 1/2V_{DD}, then a MSb-1 equal to zero is transmitted out of the serial port through S_{DOUT} and the MSb-1 capacitor is left tied to V_{REF}. If this voltage is less than 1/2 V_{DD}, a MSb-1 bit equal to one is transmitted out of the serial port and the MSb-1 capacitor is connected to V_{SS}. This process is repeated until the capacitive array is fully utilized.

Effects of Input Source Resistance

A detailed model of the internal input sampling mechanism of a SAR ADC is shown in Figure 3. The critical values to pay attention to in this model are R_S, C_{SAMPLE} and R_{SWITCH}. C_{SAMPLE} models the summation of the capacitive array shown in Figure 2. Errors due to the pin capacitance and leakage are minimal. The internal switch resistance combines with the external source resistance and sample capacitor to form a R/C pair. This R/C pair requires approximately 9.5 time constants to fully change to 12-bits over temperature. For the MCP3201 12-bit A/D Converter, 938 nsec are required to fully sample the input signal assuming $R_S << R_{SWITCH}$.

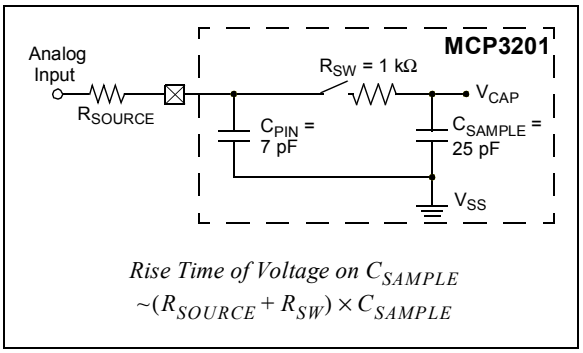


FIGURE 3: *The model of the input stage of the MCP320X ADC can be reduced to a switch resistance and sample capacitor.*

The accuracy of a SAR ADC, such as the 12-bit MCP3201, can be compromised if the device is not given enough time to sample. In the graph of Figure 4, the y-axis is Clock Frequency in MHz and the x-axis is Input (Source) Resistance in ohms. The sampling time of the converter for these clock frequencies is equal to 1.5 clocks. For example, a clock speed of 1.6 MHz would translate to a sample time of (1.5/1.6 MHz) or 937.5 nsec.

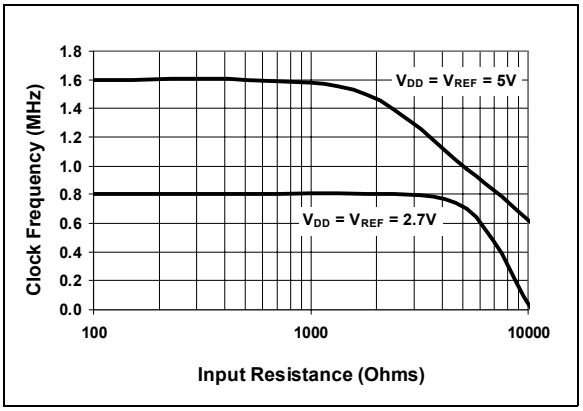


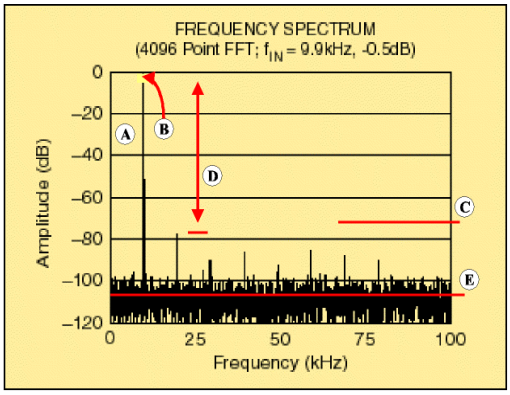
FIGURE 4: *This graph is plotted to indicate where the MCP3201 will continue to operate accurately with in 0.1 LSb.*

In order to keep the source resistance low, it is recommended that the converter be driven by an active element, such as an operational amplifier. In this situation, the input signal could be ac, DC or both. The operational amplifier can be used for gain, filtering, impedance isolation and its drive capability. When you drive the input of an ADC with an operational amplifier, whether it is a gain cell, filter cell or both, offset, noise, gain errors and distortion can be added to the signal prior to the ADC by the amplifier. The investigation of these issues as they relate to the conversion process follows.

Figure 4 illustrates how the source resistance to the ADC can cause conversion errors. There are two obvious solutions to the problem. One would be to reduce the source resistance, while the second would be to increase the sampling time.

AC Performance of the ADC

The ac performance of an ADC can easily be viewed by looking at the FFT results from multiple, periodic conversions. An FFT plot is produced through mathematical calculations performed on a series of repetitive samples. In this calculation, the data is "binned" out into frequencies. The resultant graph produced illustrates the magnitude of the signal frequencies that go through the converter.



A = Fundamental Input Signal
B = Headroom
C = Signal-to-Noise Ration
D = Spurious Free Dynamic Range
E = Average Noise Floor

FIGURE 5: *An FFT plot is used to evaluate an ADC performance over frequency.*

From this calculation, we can extrapulate the fundamental input signal, the harmonics above that signal and the noise floor. These calculations not only give a graphical representation of the signal through the converter, they also allow for the calculation of the Spurious Free Dynamic Range, Effective Number of Bits and Signal-to-Noise Ratio. Refer to AN681, "Reading and Using Fast Fourier Transforms (FFT)", for more information on FFTs.

Although this graph presents a considerable amount of information, the plot does not differentiate aliased signals from real signals.

IMPACT OF THE OPERATIONAL AMPLIFIER

We will start with the operational amplifier block shown in Figure 6 and discuss its characteristics as they relate to this application.

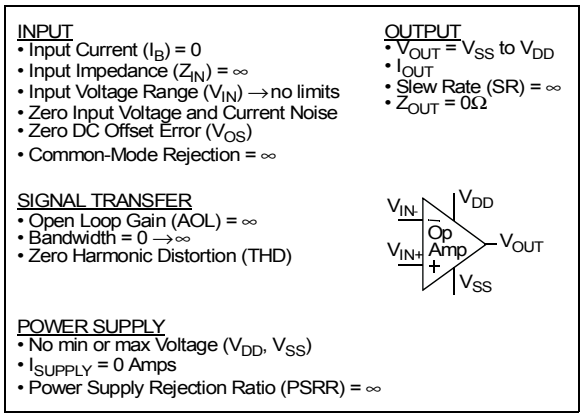


FIGURE 6: *The ideal operational amplifier description can be separated into four basic categories: input, power supply, output and signal transfer.*

While the operational amplifier brings features that are desirable to this application, there are trade-offs to account for in the design. In terms of DC parameters, the operational amplifier will have some limitations with its input and output swings. Additionally, if the wrong operational amplifier is selected, it may not be able to drive the ADC at the speeds required in the conversion process. With noise being an additional error contributed by any element put in the signal path, the operational amplifier is no exception. The ADC will also generate its own noise. The trick we will learn is that the operational amplifier noise must simply be lower than the ADC noise to be useful. Finally, the distortion characteristics of the operational amplifier should be considered. Characteristics like the bandwidth of the operational amplifier and the harmonic distortion near the output rails are candidates for possible degradation of the signal as it travels through the data acquisition system.

Operational Amplifier Input Stage

Each of the two input pins of the operational amplifier has voltage swing restrictions. These restrictions are due to the input stage design and the power supply limitations. In the device product data sheet, the input voltage restrictions are clearly defined as the Input Voltage Range and is a separate line item in the specification table, or as a condition for the CMRR specification (Input Common-Mode Voltage Range, VCM). The more conservative specification of the two is where the input voltage range is called out as a CMRR test condition because the CMRR test validates the Input Voltage Range in test.

The higher input voltage range is more a function of the input circuit topology than it is the silicon process. Again, the product data sheet should be referred to for clarification on how your selected operational amplifier performs across the input range of the operational amplifier.

Operational amplifiers that do not span across the entire power supply voltage range on the input are not useless. As a matter of fact, these operational amplifiers are useful in most circuits except for buffer configurations. Otherwise, if you use these operational amplifiers with a gain of two or higher, you can easily get around the fact that the operational amplifier does not have a rail-to-rail input range.

Operational Amplifier Noise Contribution

Operational amplifier device noise falls into two categories: voltage noise and current noise. Voltage noise is usually specified for all operational amplifiers over the full frequency range, while current noise may or may not be specified for the lower input current devices, such as CMOS amplifiers or FET input amplifiers, but is always specified for Bipolar input amplifiers. The magnitude of the operational amplifier noise is dependant on the input structure and the amount of current being driven internally through that structure.

Noise is gaussian in nature. It is close enough to a normal distribution that many of the calculations to describe a normal distribution are used to describe gaussian noise. For instance, gaussian noise units can be described as root mean square (RMS). This could be considered analogous to the calculation of one standard deviation, referred to as normal distributions. The RMS noise can be referred to the input (RTI) of the circuit or operational amplifier. It can also be referred to the output (RTO). When refering to the output, the operational amplifier gain is included in the RMS number. When defining peak-to-peak noise, a multiplier called the crest factor is used. This multiplier is used when describing non-correlated events like noise. Spot noise will be defined in the next paragraph of this application note.

Spot noise is the last unit of measure that you will find with noise specifications. Spot noise can be found in the noise density plots of product data sheets. Essentially, spot noise is the noise contributed by the operational amplifier in a particular 1 Hz frequency bandwidth. Spot noise is specified in volts or amperes. In both cases, the denominator of these units is a square root of Hertz. This parameter, typically, is referred to the input of the operational amplifier and defined at a particular frequency. To calculate the noise contributed by the operational amplifier across a specified bandwidth, the area under this curve is calculated. This representation of noise provides the flexibility needed to calculate total noise for various gains and systems.

The first step to determining the theoretical RMS or peak-to-peak noise is to calculate the closed loop gain of the noise signal. This may or may not be different than the signal gain. The noise gain is calculated as if there were a signal source at the non-inverting input of the operational amplifier. The area under the noise density curve is calculated and multiplied by the closed loop gain of the circuit.

The area under the noise density curve should be calculated in a piece wise manner. One region is across the 1/f noise region of the noise density curve. The second segment is located where the noise density curve and the operational amplifier gain curve are flat. The third region would be where the operational amplifier curve is starting to fall at 20 dB per decade. In all cases, these areas are multiplied by the square root of the bandwidth of interest.

The different regions are added with a square root of the sum of the squares formula to obtain the entire noise contribution of the circuit. The calculated value in this exercise is the referred to output (RTO) noise in the units V_{rms}. A way to view this noise on the bench is to use a scope and look at the output of the operational amplifier. While the scope photo would not have any significant frequency content, it would, in fact, show a “noisy” view on the screen. Your calculated RMS number would be equivalent to a line at approximately 70% of this signal, centered on the median of the noise on the scope screen.

This type of noise is a statistical occurrence. Hypothetically, one would have to wait an infinite amount of time to determine whether or not the designed system would remain within a set of boundaries. This approach to determining the peak-to-peak noise in a circuit is fairly unreasonable, but because we have characterized this noise as gaussian in nature, we can use a statistical model to predict the peak-to-peak noise with a degree of certainty.

The technique of predicting the peak levels of noise is relatively simple to calculate using a crest factor. If a crest factor is identified, multiplied by 2 times the RMS value, the peak-to-peak noise response of the system can be determined with a level of certainty.

Table 1 has a list of crest factor numbers to work with. In this industry, an acceptable crest factor is 3.3, implying, with a degree of certainty over time of 0.1%, that occurrences would happen outside the boundaries that have been defined.

Crest Factor	% of occurrences where peaks are exceeded
2.6	1%
3.3	0.1%
3.9	0.01%
4.4	0.001%
4.9	0.0001%

TABLE 1: *Crest Factor vs. Percent of occurrences where peaks are exceeded.*

With this style of noise calculation for the operational amplifier, it is easy to determine if the operational amplifier has a possibility of contributing more noise to the system than the ADC. In this evaluation, the Signal-to-Noise Ratio (SNR) at the output of the operational amplifier is assumed to be equal to the RMS Full Scale input of the ADC. Given this criteria, the RMS signal of the ADC full scale input is equal to 5/(2* $\sqrt{2}$). This is equivalent to 1.76 V_{rms}. If the MCP601 operational amplifier, with a gain of 2 V/V, is used in this analysis, the contributed noise from the operational amplifier is 137 mV_{rms}. The overall output signal-to-noise ratio of the operational amplifier cell is equal to 82 dB.

The ADC is evaluated in terms of its referred-to input (RTI) SNR. This is done by accumulating several conversions and calculating the ratio of input noise to the rest of the noise (without including the harmonics) in a FFT plot. In this example, 4096 repetitive samples are accumulated using the 12-bit MCP3201 ADC. The ideal SNR of a 12-bit converter is 74 dB. This level of SNR is a result of quantization noise with the 12-bit converter. The measured SNR of the MCP3201 is 73.03 dB.

The signal-to-noise ratio (RTO) of the operational amplifier is 82 dB. The signal-to-noise ratio (RTI) of the ADC is 73 dB. These two noise sources are added together to determine what the overall noise response of the system will be. With the standard calculation of a square root of the sum of the squares, the overall noise is 72.49 dB. This verifies that the operational amplifier is contributing a minimal amount of noise to the system. If a lower-noise operational amplifier were chosen for the application, the reduction in noise may not be worth the cost because the ADC is the dominating factor in this evaluation. If this lower-noise operational amplifier has a wider bandwidth than the MCP602, it is possible that the lower noise operational amplifier will contribute more noise to this application, particularly if no anti-aliasing filter is used.

Using Operational Amplifiers for Filtering

It is important to recognize and understand that your electronics are not aware of what your intentions are. In other words, some designers think that if they have an intention to measure or convert DC signals, the electronics will perform only that specific task. This is the farthest you can get from reality. The electronics will reliably report everything that is happening in your system to the extent of the capabilities of your electronics.

A good example of this is when your converter aliases higher frequencies into the output. In the example in Figure 6, there are five signals that have a significant amplitude. Four of the five signals are beyond half of nyquist. Since the converter reliably reports the signals within its bandwidth, it will report higher frequencies at a lower frequency because of a fold back phenomena. Once this fold back has occurred (due to the conversion), the higher frequency information can not be discriminated from the in-band information. An effective way to remove the noise is by using a low pass filter. In this example, an MCP601 CMOS operational amplifier is used to implement a 2nd-order, low pass filter. For detailed information about the Nyquist theorem and aliasing problems, refer to AN699, “Anti-aliasing, Analog Filters for Data Acquisition Systems”.

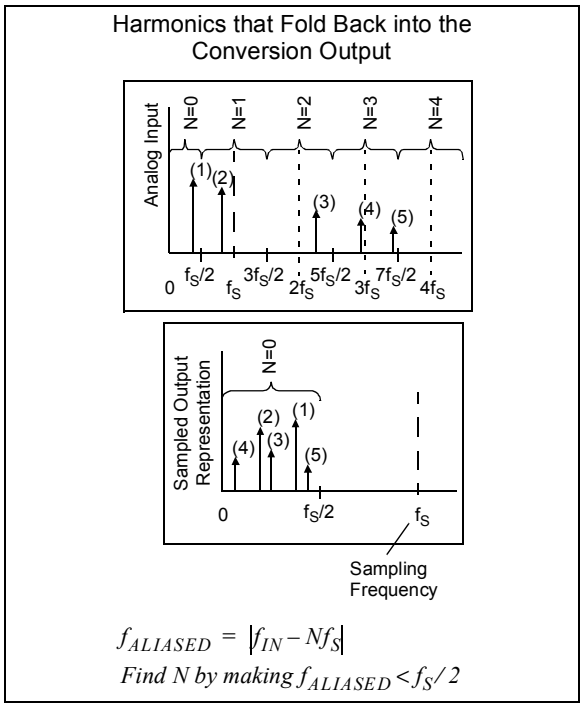


FIGURE 7: *Frequencies in a signal that are above 1/2 of the sampling frequency are aliased back into the output data as erroneous information.*

The filter for this application example can be designed using FilterLAB® from Microchip. This free software is available at www.microchip.com.

Gain and Output Stage of the Operational Amplifier

Another area where the operational amplifier can contribute distortion to the signal is due to the fundamental frequency response of the operational amplifier. The bandwidth of the operational amplifier should be wide enough to accommodate over 100 times the fastest signal going through the operational amplifier.

This implies that the closed loop bandwidth of the operational amplifier should be more than 100x higher than the bandwidth of the signal of interest. For example, at the closed loop gain corner frequency of a unity gain stable operational amplifier, the attention in gain is 3 dB. In this example, that corner frequency is 2.80 MHz. A 3 dB attenuation is analogous to ~ 70.7% attenuation of the gain. If an evaluation of this curve is performed at 280 kHz, the attenuation of the gain would be 99.5%. If that same evaluation of this curve were done at 2.8 kHz, the attenuation of the gain would be 99.995%. For a 12-bit system, the most attenuation that can be measured is 99.97%, which is equivalent to 1 LSb.

The output swing specification of an operational amplifier defines how close the output terminal of the operational amplifier can be driven to the negative or positive supply rail under defined operating and load conditions. Unlike the input voltage range specification, the voltage output swing of an operational amplifier is not as well defined from manufacturer to manufacturer. The output current, as well as the operational amplifier's Open Loop Gain (AOL) are related to this specification. The output current is a test condition for the Voltage Output Swing Specification. It is also a test condition for the Open Loop Gain test, which validates the Voltage Output Swing test with a second operational amplifier specification.

The output swing capability of the operational amplifier is dependent on the output stage design and the amount of current that the output stage is driving under test. With this portion of the specifications, care should be taken when comparing operational amplifiers.

The output swing specifications V_{OH} and V_{OL} are not intended to describe an operational amplifier operation in its linear region. Rather, these specifications tell the user the maximum that the output stage can stretch. If you need to determine to what extent that the operational amplifier remains in its linear region, the better specification is to look at the open loop gain specification.

Figures 8 and Figure 9 illustrate an operational amplifier's level of output stage distortion during the sampling portion of the conversion.

Figure 8 shows the FFT response of an operational amplifier (MCP601) / ADC (MCP3201) combination to a 1 kHz input signal in a 5V system. With the top diagram, the input frequency, operational amplifier gain, and sampling frequency is no different than the FFT plot on the bottom. The difference between these two FFT plots is the output peak-to-peak signal coming out out of the operational amplifier. For the plot on the bottom, the peak-to-peak output swing of the operational amplifier is greater that the response on the top.

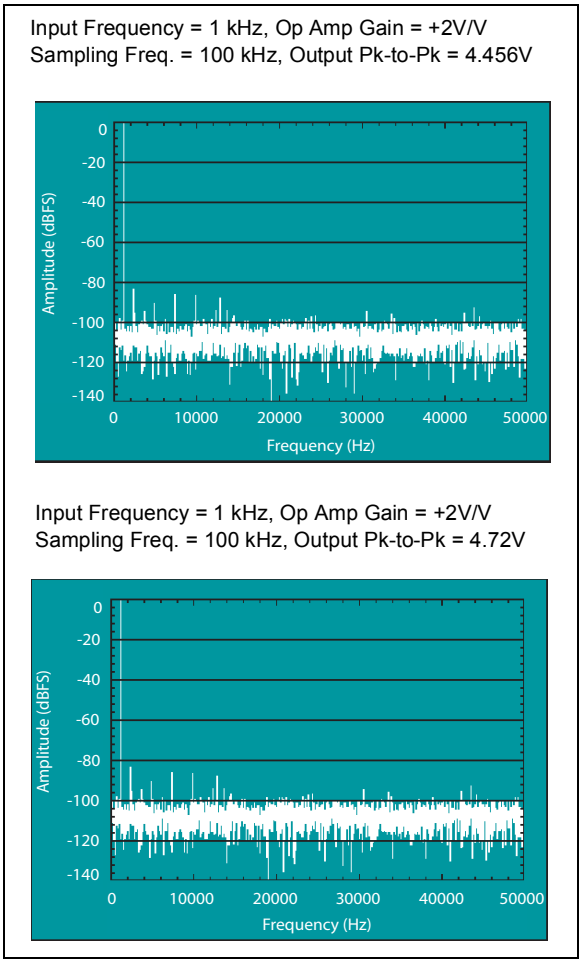


FIGURE 8: *Using the same hardware configuration, input frequency and sampling frequency, the peak-to-peak output of the operational amplifier effects the distortion of the circuit.*

The MCP601 V_{OH} and V_{OL} specs are typically 15 mV to 20 mV from the rail. As can be seen in this test, the output stage of the operational amplifier is becoming non-linear way before this point. In the diagram on the bottom, the distance of the output swing of the operational amplifier from the rails is 140 mV.

In Figure 9, the wide output swing that failed to perform properly in Figure 8 is used again, with the exception that the sampling frequency is changed. For the plot on the top, the sampling frequency is now 50 kHz, as opposed to 100 kHz. As shown in this example, the operational amplifier has been given more time to settle into final value, as shown in the diagram on the top.

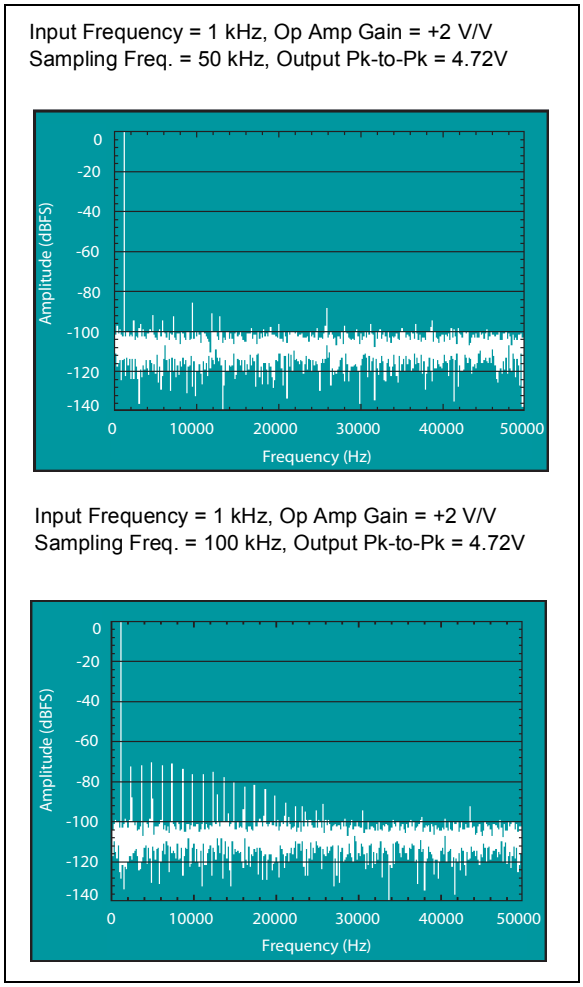


FIGURE 9: *Using the same hardware configuration, input frequency, and peak-to-peak output, the sampling frequency of the ADC effects the distortion of the circuit.*

CONCLUSION

In order to implement a successful circuit the first time with an ADC / operational amplifier combination, you must know your converter first and foremost. Understand the features, as well as limitations in terms of sampling structure, number of usable bits and general specification limits. Once this in known, you can comfortably connect the input to an active input source. With this connection, there are a few performance specifications that should be aware of to insure you have the right operational amplifier. These specifications are rail-to-rail input and output capability, bandwidth and noise.

REFERENCES

AN546, “Using the Analog-to-Digital (A/D) Converter”, Microchip Technology, Inc.

AN693, “Understanding A/D Converter Performance Specifications”, Microchip Technology, Inc.

AN681, “Reading and Using Fast Fourier Transforms (FFT)”, Microchip Technology, Inc.

AN722, “Operational Amplifier Topologies and DC Specifications”, Microchip Technology, Inc.

AN723, “Operational Amplifier AC Specifications and Applications”, Microchip Technology, Inc.

AN699, “Anti-aliasing, Analog Filters for Data Acquisition Systems”, Microchip Technology, Inc.

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