AN230

P4 Calibration Charts

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OVERVIEW

The P4 calibration flow charts describe the algorithms used to calibrate the PS401 Accuron™ battery manager. The PS401 A/D converter can be configured to perform certain measurements using an ADL (A/D converter List). This feature is only available in firmware revisions that are “ADL enabled”. All firmware revisions are ADL enabled for both voltage and current except those in the following table.

TABLE 1: FIRMWARE REVISIONS WITHOUT ADL CAPABILITY

No Voltage ADL	No Current ADL
PS401-0107	PS401-0107
PS401-0108	PS401-0108
PS401-0109	PS401-0109
PS401-0202	PS401-0202
PS401-0203	PS401-0203
PS401-0204	PS401-0204
PS401-0301	PS401-0301
PS401-0302	PS401-0302
	PS401-0303
	PS401-0401

ADL capability is not essential to P4 calibration. The flow charts include information for calibrating all PS401 firmware revisions. The advantages of using the ADL list are quicker calibration (calibration delays are shortened) and improved current calibration accuracy. To set a particular ADL mode for calibration, write to the PS401 using a SMBus Block Write protocol:

data[0] = 0x01

data[1] = 0 (ADL_CURRENT), OR

1 (ADL_CURRENT_OFFSET), OR

2 (ADL_VOLT_OR_TEMPERATURE)

number of bytes = 2

destination SMBus register is 0x24.

The write can be verified by reading RAM register 0xCD (one byte, bank 0/1). The returned value should be the same as the ADL mode number (0, 1 or 2) written to the part.

The part can be returned to ADL_NORMAL mode by again writing to the SMB register 0x24 using the SMB BLOCK WRITE protocol, but the data looks like:

data[0] = 0x00

number of bytes = 1

So, the procedure for using this mode in calibration is:

1. Change P4 to ADL mode of choice using SMB BLOCK WRITE protocol
2. Delay ~500 ms to allow part to update RAM
3. Verify change by reading RAM register
4. Perform calibration
5. Return P4 to Normal mode

The flow charts also use a term “SLEEP factor”, which is a wait state. The calibration procedure should wait before proceeding.

FIGURE 1: P4 CALIBRATION FLOW

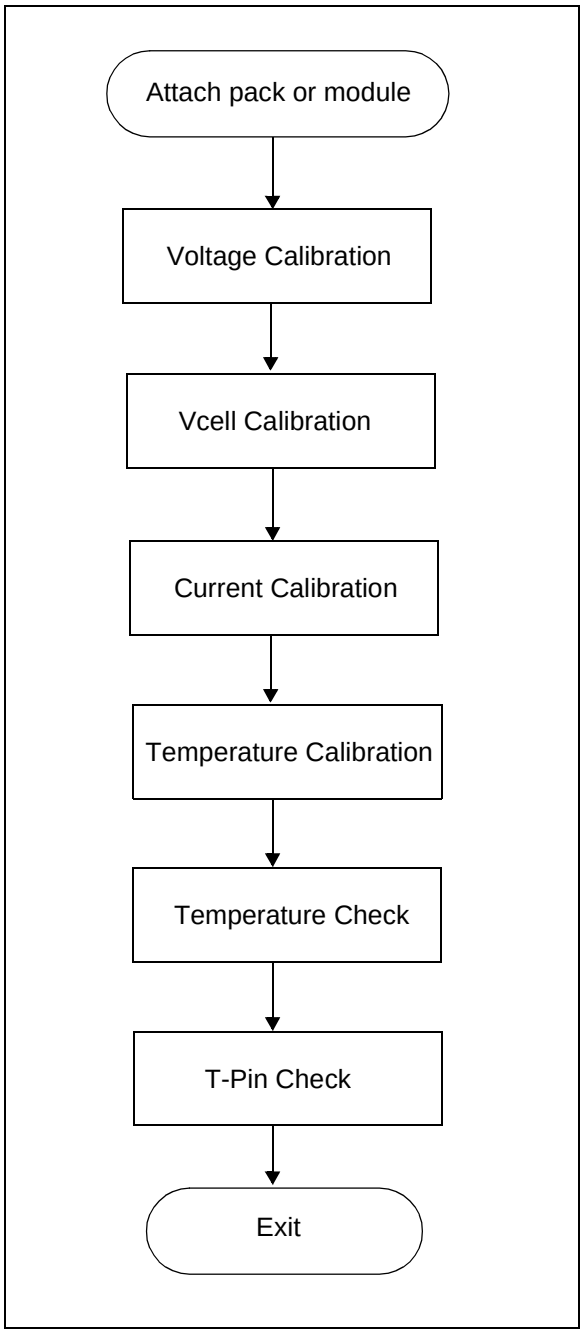


FIGURE 2: PACK VOLTAGE CALIBRATION

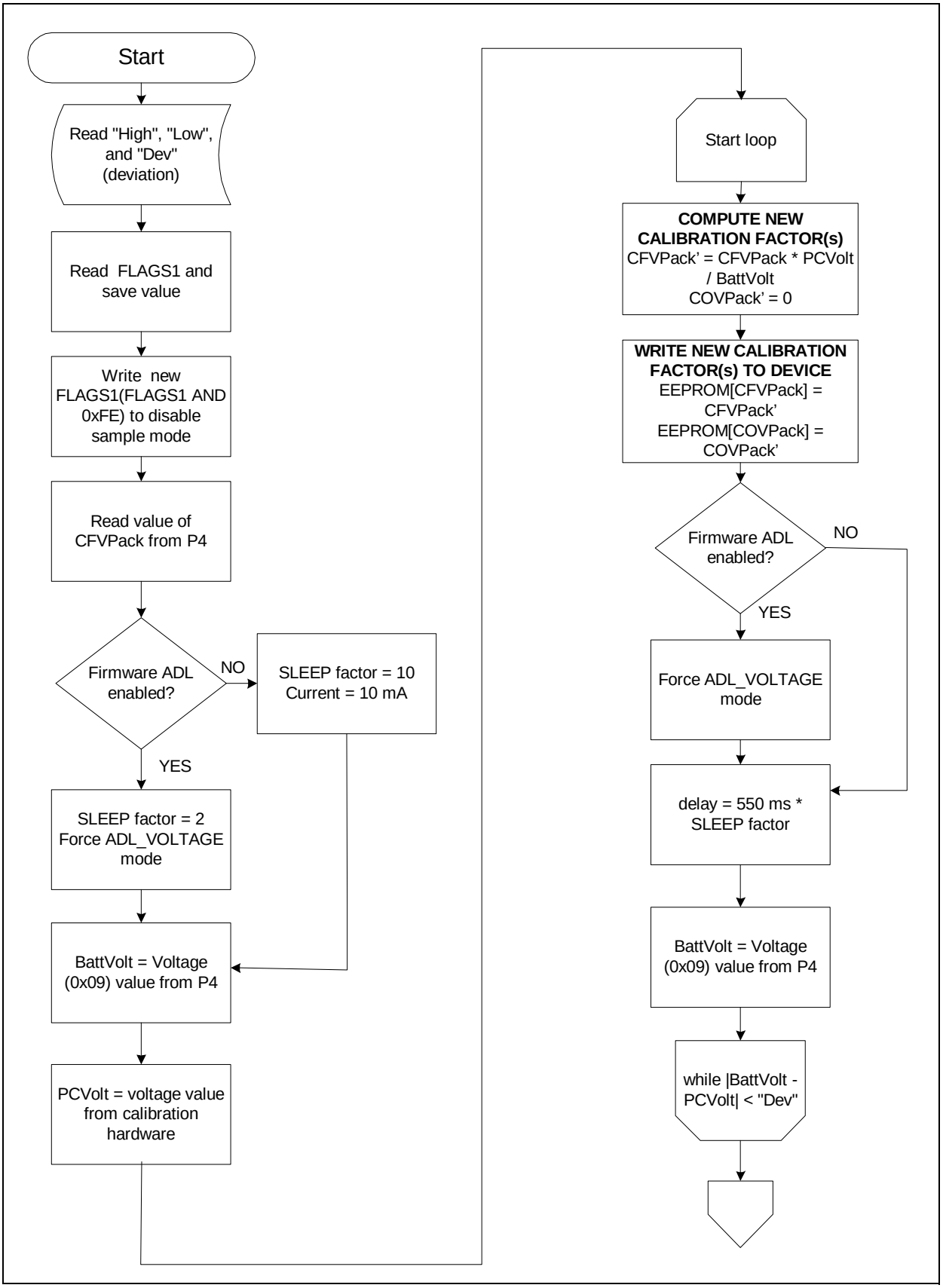


FIGURE 2: PACK VOLTAGE CALIBRATION (Continued)

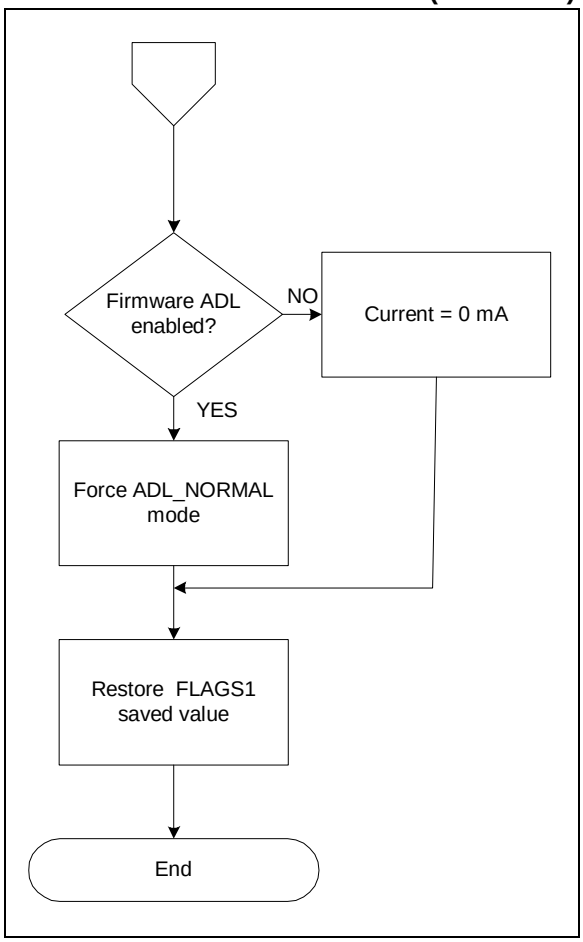


FIGURE 3: CELL VOLTAGE CALIBRATION

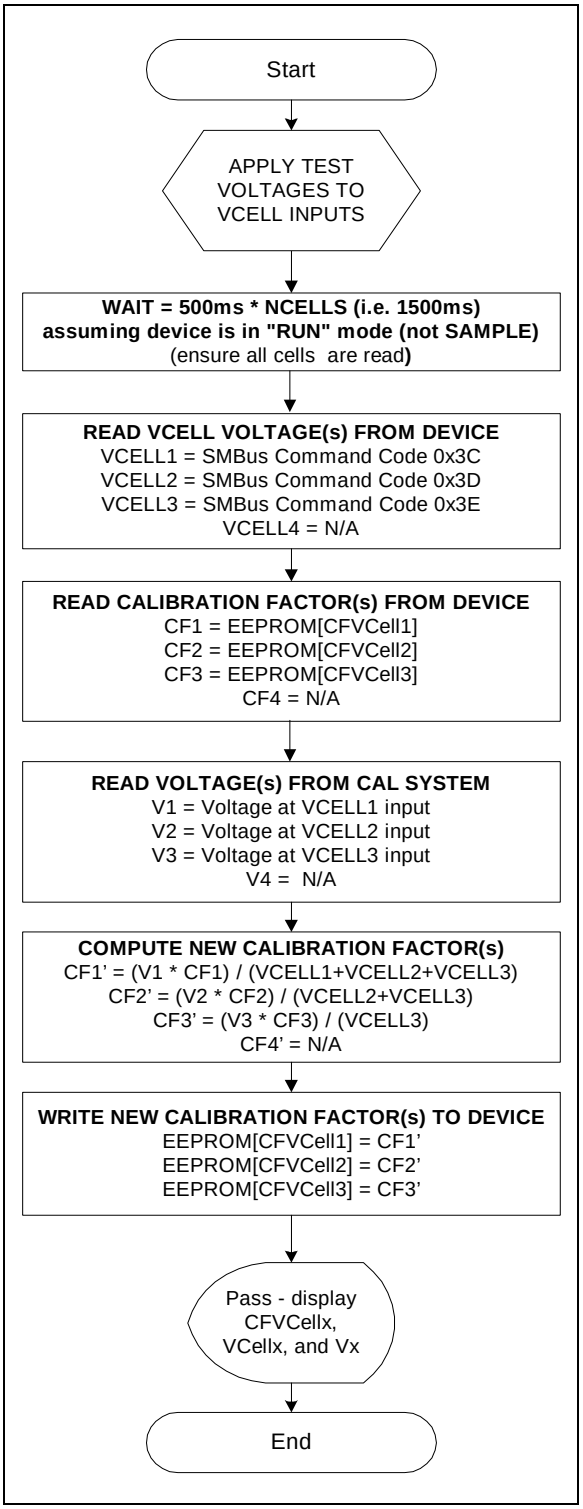


FIGURE 4: CURRENT CALIBRATION

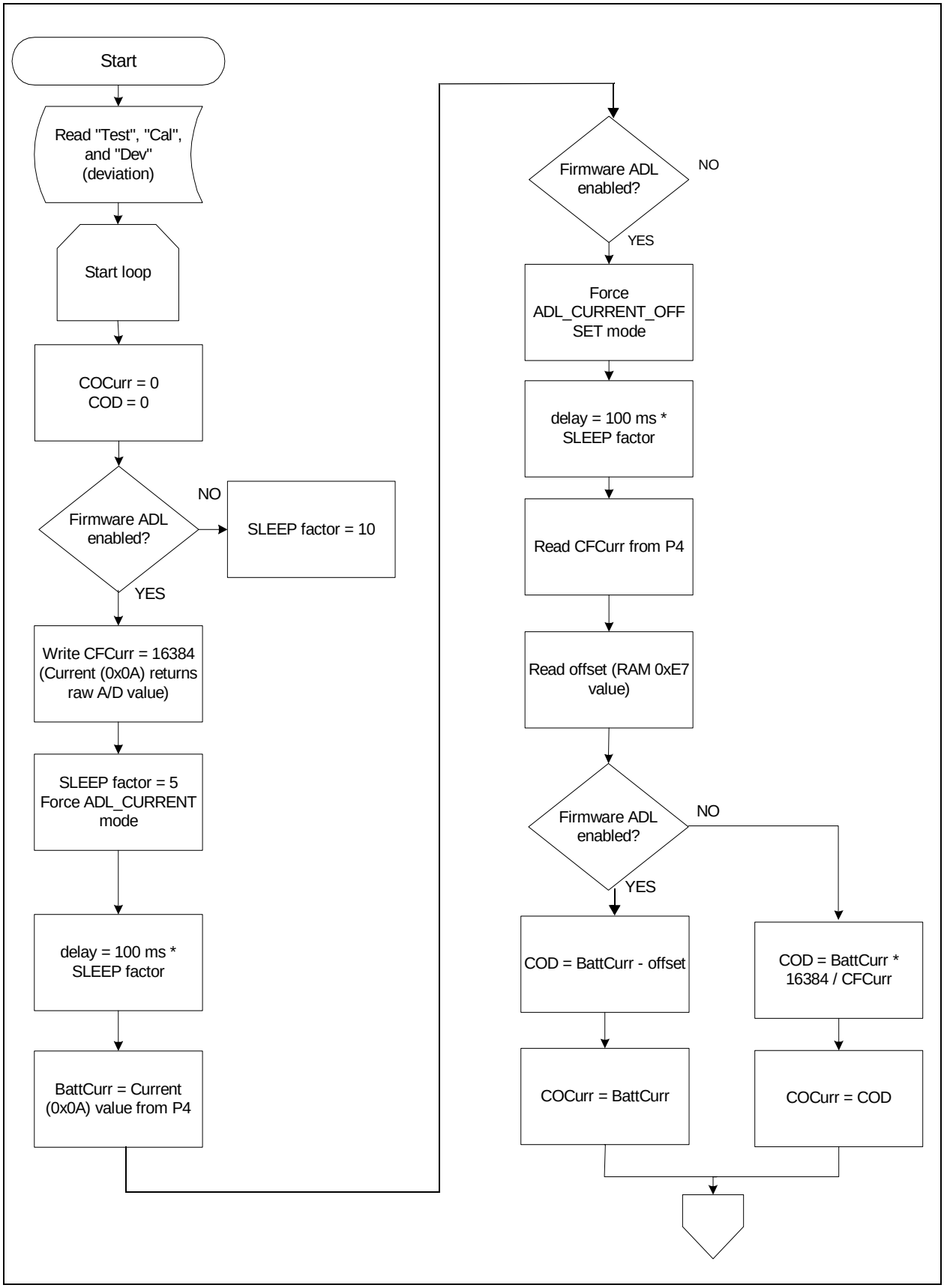


FIGURE 4: CURRENT CALIBRATION (Continued)

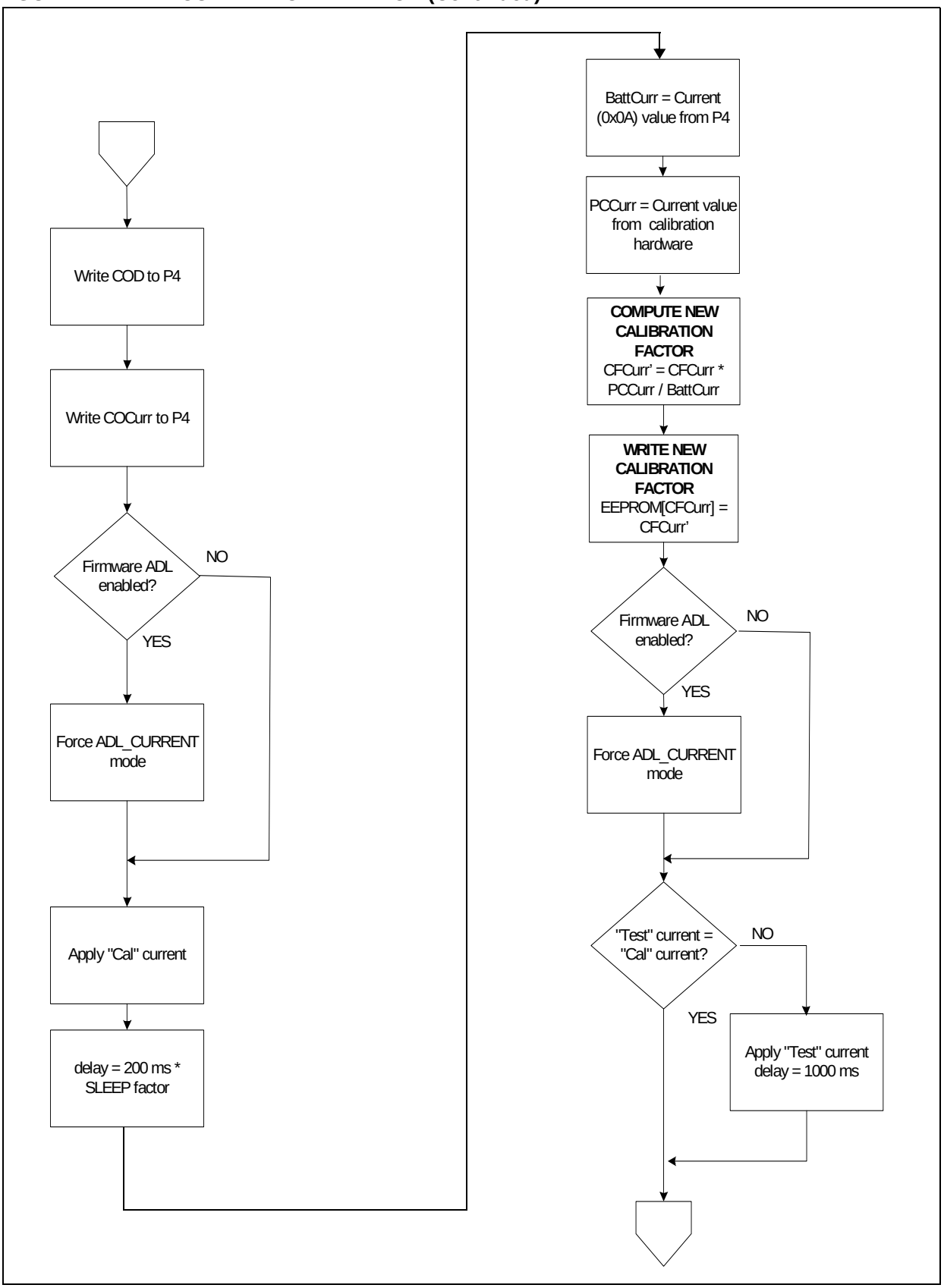


FIGURE 4: CURRENT CALIBRATION (Continued)

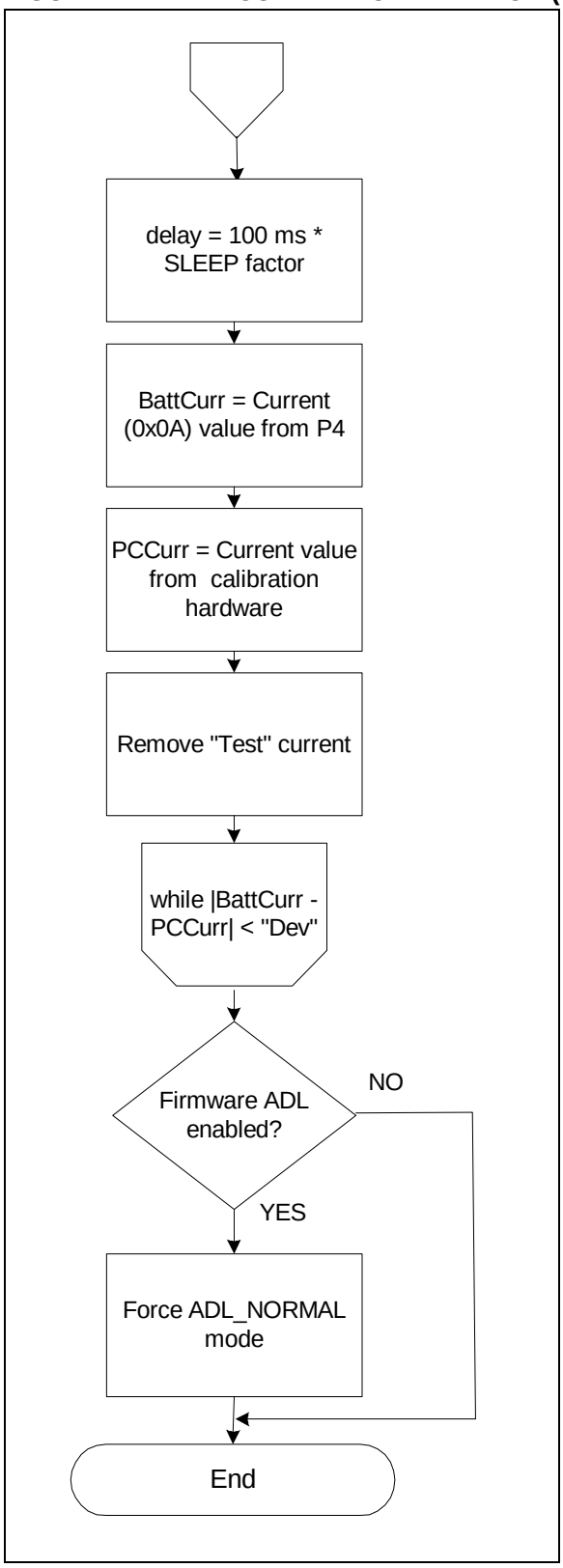


FIGURE 5: TEMPERATURE CALIBRATION

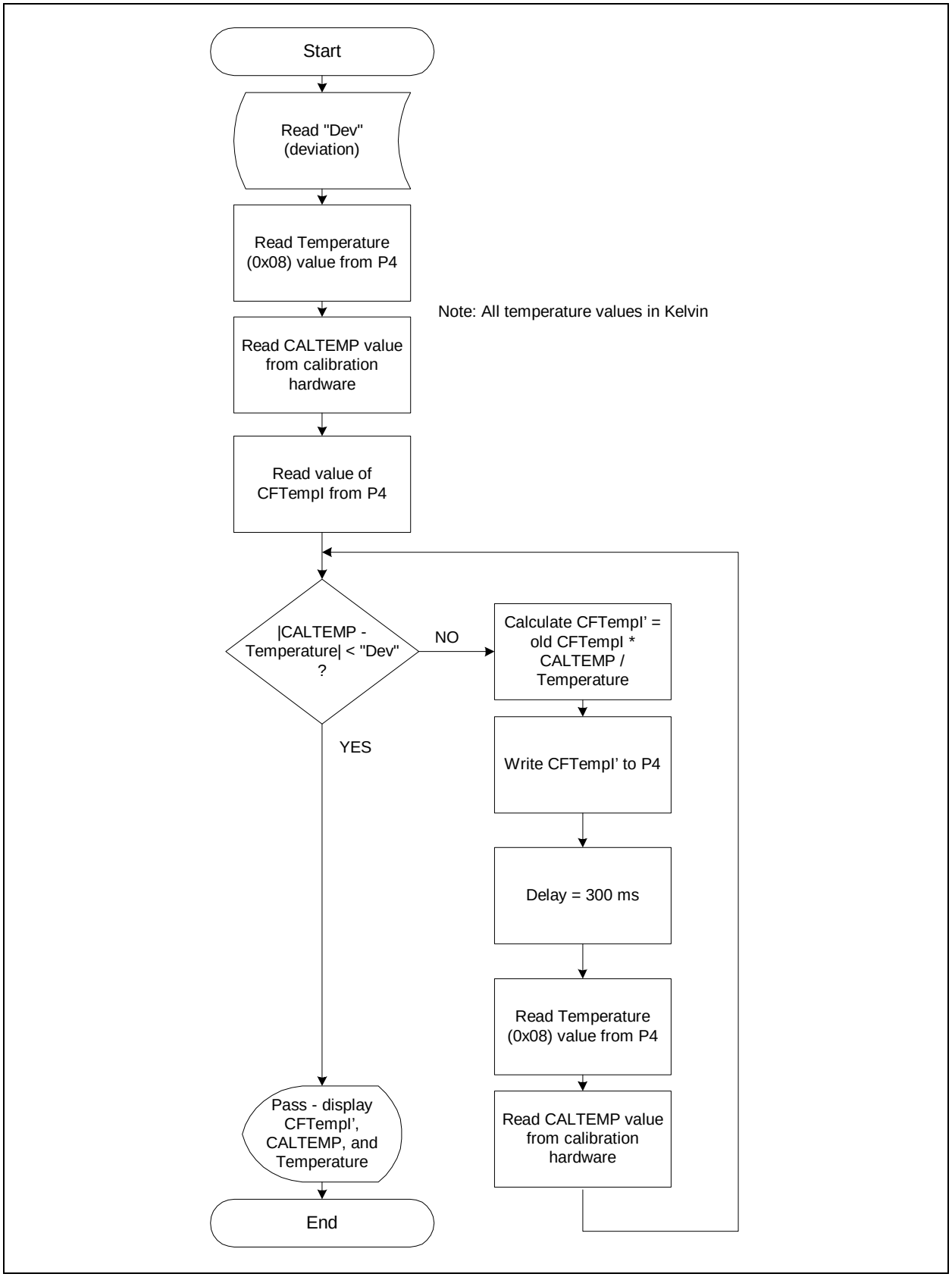


FIGURE 6: TEMPERATURE CHECK

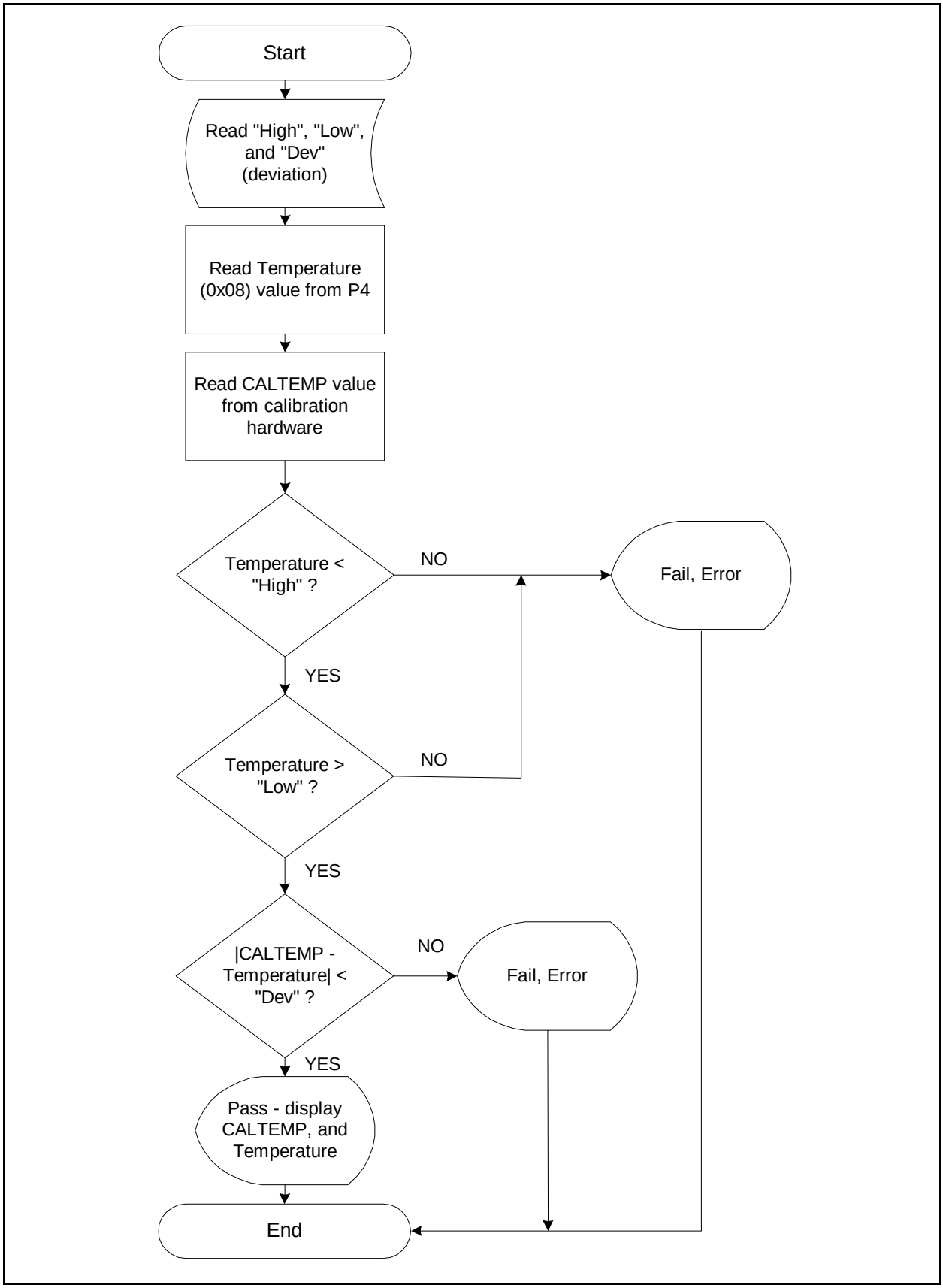
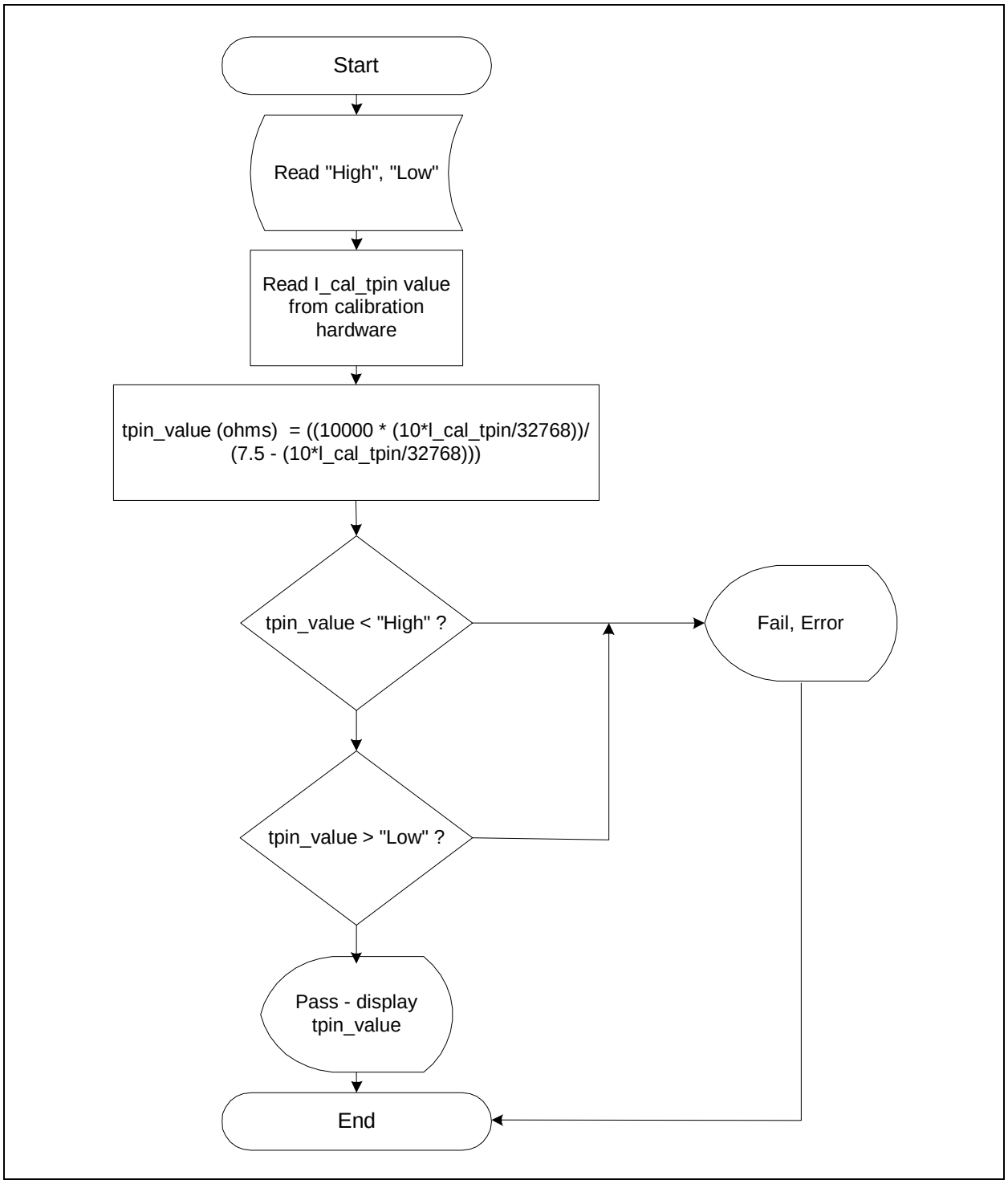


FIGURE 7: T-PIN CHECK



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