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TC7135 Microprocessor Interface

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INTRODUCTION

Many data acquisition systems require both a visual display and a computer interface. The TC7135 from Microchip Technology is a 4-1/2 digit Analog-to-Digital converter (ADC) which can easily provide both of these functions. The TC7135's multiplexed BCD outputs interface easily to low cost LED or LCD decoder/drivers, such as the TC7211A. Also, the TC7135's data outputs simplify computer interfacing.

This application note will present both the hardware and software required to interface the TC7135 to a microprocessor. The circuit was developed for a 6502µP and 6522 I/O port, but the design can easily be modified for other µPs and I/O ports.

The TC7135 has several features which make it an attractive choice for data acquisition where speed is not an overriding consideration. The analog features include:

- High Resolution ..... 20,000 counts
- High Accuracy ..... ±1 count
- Low Roll-Over Error ..... ±1 count
- Valid Polarity at 000 reading (the + and – zero states give an extra bit of resolution.
- Negligible zero drift – definitely not the case with a bipolar DAC/SAR type ADC.
- The dual-slope conversion method rejects 50Hz, 60Hz and 400Hz noise.
- The ratiometric reference and differential inputs provide flexible transducer interfacing.

The TC7135 T also has features that simplify system design:

- Easy µP interfacing
- Overrange and underrange flags for autoranging and process control decisions
- Operation from ±5V supplies, with only 10mW typical power dissipation
- TTL compatible outputs (1.6mA sink current)

The TC7135 provides output signals which, together with one port of an LSI I/O chip, simplify a microprocessor interface. The relationship between the various TC7135 outputs is shown in Figure 1. The specific functions of these outputs are as follows:

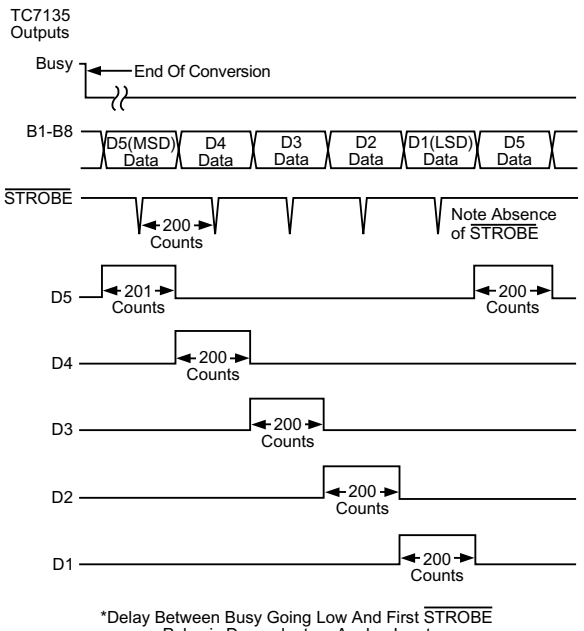


FIGURE 1: *Timing relationship between TC7135 outputs.*

TC7135 Pin Function

B1-B8	BCD coded data is output on the B1-B8 pins.
DS5-DS1	Digit Select 5 (most significant digit) through Digit Select 1 (least significant) go high as data on B1-B8 becomes valid for that digit.
STROBE	For the first digit scan after a conversion $\overline{\text{STROBE}}$ goes low (for 1/2 clock period) in the middle of each digit strobe. After five pulses, $\overline{\text{STROBE}}$ stays high until the next conversion is complete.
BUSY	BUSY is high while the TC7135 is in Integrate or Deintegrate phases of a conversion. The falling of BUSY can, therefore, be used as an end of conversion signal.
POL	POLARITY is high if the analog input polarity is positive.
OR	OVERRANGE goes high if the analog input is greater than full scale (reading >20,000).
UR	While UNDERRANGE goes high if the reading is 1,800 or less.

The TC7135 also has a RUN/$\overline{\text{HOLD}}$ input. If RUN/$\overline{\text{HOLD}}$ is held low, the converter will remain in the auto-zero phase. A new conversion will not begin until RUN/$\overline{\text{HOLD}}$ goes high. This input can be used to generate conversions on command.

INTERFACE HARDWARE

The complete TC7135 to SYP6522 interface schematic is shown in Figure 2. BCD data, POL, OR, UR, and DS5 are connected to the 6522's PA0 through PA7 inputs. The TC7135's $\overline{\text{STROBE}}$ output interrupts the microprocessor via the 6522's CA1 interrupt. RUN/$\overline{\text{HOLD}}$ can be controlled by programming CA2 as an output.

At first glance, the circuit may appear incomplete because digit selects DS4 through DS1 are not connected. However, DS5 is the only digit select required. As mentioned previously, there are only 5 $\overline{\text{STROBE}}$ pulses per conversion cycle, with the first $\overline{\text{STROBE}}$ occurring during DS5. The µP decodes the logical "AND" of DS5 and $\overline{\text{STROBE}}$ (DS5 • $\overline{\text{STROBE}}$) as a conversion complete signal.

If the µP finds (DS • $\overline{\text{STROBE}}$) true upon responding to an interrupt, an "end of conversion" is assumed and assembling of BCD data from the TC7135 begins. Each of the next four interrupts will provide another BCD digit. The µP counts interrupts in a register and stores the corresponding BCD data in successive memory locations. After five $\overline{\text{STROBE}}$ pulses, all BCD data has been transferred to the µP and conversion is complete.

One constraint of this interface method is that the µP must respond to each digit's interrupt before the next digit becomes valid. The 6522's CA1 input can be programmed to latch data into Port A, as well as provide an interrupt to the µP. Since latched data remains valid until the next $\overline{\text{STROBE}}$ pulse, the µP has the full interval between $\overline{\text{STROBE}}$ pulses to service each interrupt. $\overline{\text{STROBE}}$ pulses are 200 clock cycles apart. A TC7135 clock frequency of 100kHz will allow the µP two milliseconds (10µsec x 200 clock cycles) to respond to each interrupt without losing data.

INTERFACE SOFTWARE

Software for the TC7135 to 6502 interface can be divided into three routines: (1) Programming the 6522's Port A for latched input and interrupt from CA1; (2) the interrupt service routine which actually acquires and stores BCD data from the TC7135; (3) display or manipulation of the acquired data. Figure 3 is a 6502 assembly language listing of the first two routines. An interrupt service routine flow chart is shown in Figure 4. Since the end of a digit scan leaves 5 digits of BCD data in successive memory locations, the user will find the interface software easy to incorporate into a specific display or manipulation routine.

The 6522 I/O port must be programmed before data can be received from the TC7135. The code in Figure 3, beginning at location "SET-UP," writes data into the 6522's control registers to enable the following functions (1) Port A will be latched input, controlled by input of CA1; (2) CA2 will be an output, programmed high (TC7135 in "RUN" mode); (3) Interrupt enabled on the falling edge of CA1. The function of data written to each 6522 register is defined in Figure 5.

When programmed for interrupt operation, the 6522 will pull its IRQ output low on the falling edge of each STROBE pulse from the TC7135. Assuming interrupts are enabled, IRQ going low will cause the 6502µP to load the address of an interrupt service routine from memory locations FFFE and FFFF. This routine will typically identify the interrupting device, determine its priority and jump to a program to service the interrupt. The user must provide software to vector interrupts coming from the TC7135 to the service routine located at location "INTVEC" of Figure 3. The TC7135-6522 hardware can accommodate interrupt service delays of up to 2msec, so a relatively low-priority interrupt status can be used.

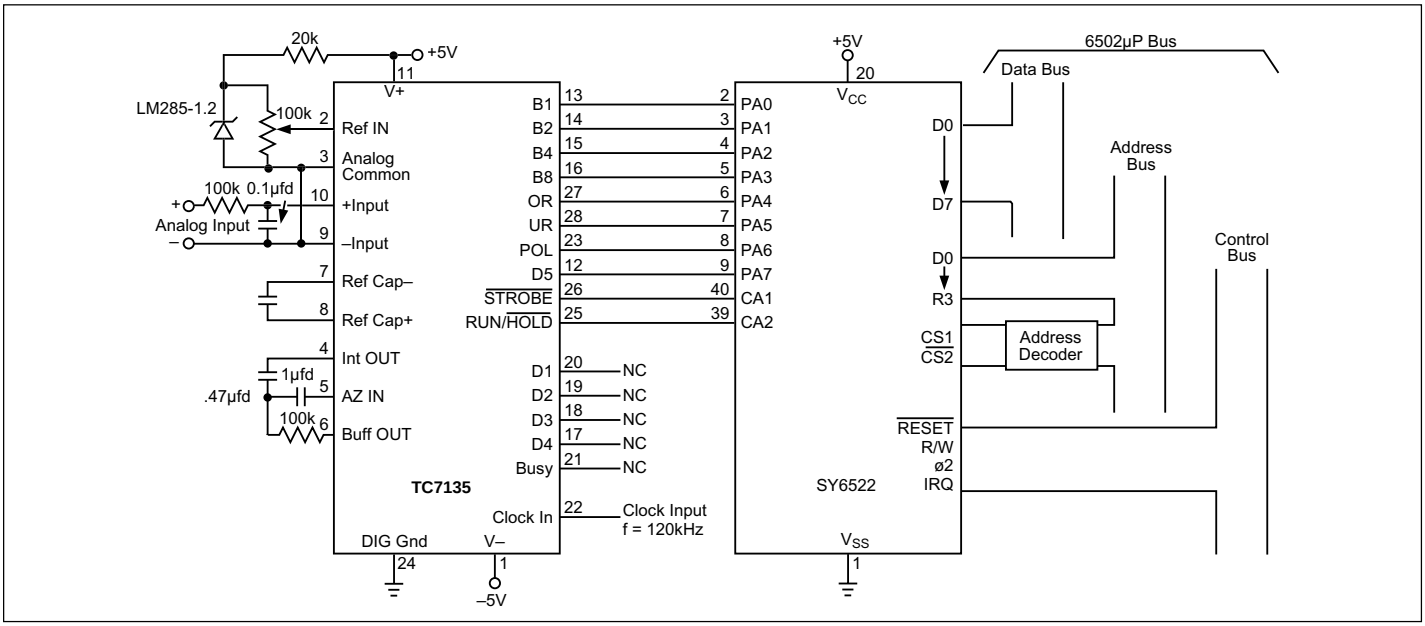


FIGURE 2: *TC7135 to 6502µP interface schematic.*

```
        ;
        ;
        ;-------------------------------------------------
        ; TC7135 INTERFACE TO A 6502 MICROPROCESSOR
        ;  USING A 6522 I/O PORT
        ;
        ; RESULTS ARE STORED IN 5 BYTES OF ZERO-PAGE
        ;  MEMORY, BEGINNING AT LOCATION "DIGSTOR"
        ;  (MOST SIGNIFICANT DIGIT FIRST)
        ;
        ; USER MUST PROVIDE INTERRUPT VECTOR FROM
        ;  THE 6522'S CA1 INTERRUPT TO A ROUTINE
        ;  AT THE "INTVEC"
        ;
        ;-------------------------------------------------
        ;
        ;SET UP 6522 FOR INTERRUPT OPERATION
        ;
IOPRT   .EQU    0A800   ;ADDRESS OF 6522 I/O PORT
SETUP   .EQU    028D    ;ADDR OF 6522 SET UP ROUTINE
        ;
        .ORG    SETUP
        LDA     #01     ;SET PORT A FOR
        STA     IOPRT_0B;LATCHED INPUT
        LDA     #0E     ;CA1-INT ON NEG EDGE
        STA     IOPRT+0C;CA2=HIGH (7135 IN "RUN" MODE)
        LDA     #082    ;ENABLE CA1 INTERRUPT
        STA     IOPRT+0E;
        JMP     MAINPRG ;I/O PORT SETUP COMPLETE, SO
                        ; JUMP TO OPERATING SYSTEM OR
                        ; TO MAIN PROGRAM
        ;
        ;BEGIN INTERRUPT SERVICE ROUTINE
        ;
XSTOR   .EQU    81      ;SAVE X REGISTER
DIGSTOR .EQU    82      ;SAVE RESULTS HERE
INTVEC  .EQU    02E0    ;6522'S CA1 INTERRUPT ROUTINE
        .ORG    INTVEC
        ;
        LDA     IOPRT+1 ;GET DIGIT FROM 6522
        BPL     NXTDIG  ;IF MSB=0, THIS IS NOT THE MOST
                        ; SIGNIF DIGIT. SO CONTINUE
        BIT     OVRBIT  ;CHECK FOR OVERRANGE
        BNE     OVRANG  ;BRANCH TO ERROR ROUTINE
        LDX     #00     ;SET THE DIGIT POINTER
        STX     XSTOR   ; AND STORE
        ;
NXTDIG  LDX     XSTOR     ;GET DIGIT POINTER
        STA     DIGSTOR,X ;STORE DIGIT IN ZERO PAGE
        INX               ; AND POINT TO
        STX     XSTOR     ;  THE NEXT DIGIT
        CPX     #05       ;5 DIGITS COMPLETES ONE SCAN
        BEQ     DONE      ;CONVERSION COMPLETE, PROCESS
                          ;OR DISPLAY DATA
                          ;THE 'DONE' ROUTINE MUST END WITH 'RTI'
        RTI               ;RETURN IF NOT COMPLETE
        ;
OVRANG  LDX     #01     ;SET DIGIT COUNTER SO THAT DIGITS
        STX     XSTOR   ; WILL NOT OVERFLOW ZERO PAGE MEM
        NOP             ;IF REQUIRED, USER PROGRAM FOR
        NOP             ; SERVICING OVERRANGE GOES HERE
        RTI             ;AND RETURN
        ;
        ;
        .END
```

FIGURE 3: *6502 assembly language testing.*

Once the 6522's interrupt has been recognized and vectored to location "INTVEC," a read of Port A loads the TC7135 data in to the 6502 accumulator. Reading Port A also sets the µP's status flags and resets the 6522's interrupt flag.

The µP now tests whether the accumulator contains the TC7135's most significant digit by testing for DS5 being high. Connecting DS5 to PA7 (MSB) of the I/O port allows testing DS5 with a single branch on plus instruction.

If DS5 is high, this data signals the beginning of a new display scan (i.e., an end of conversion has occurred). The µP zeros its X index register, which will be used both to count the digits and to provide an offset for storing each digit in zero page memory. Register X is also stored in zero page memory at location XSTOR, since its contents will probably be lost upon returning from interrupt.

An early indication of an overrange condition can be obtained at this time. A bit mask, stored in memory, is used to test for the TC7135's OVERRANGE input. If OR is high, the program branches to an error routine. An alternative for overrange testing is to wait until all digits have been scanned and then test bit 4 of any digit.

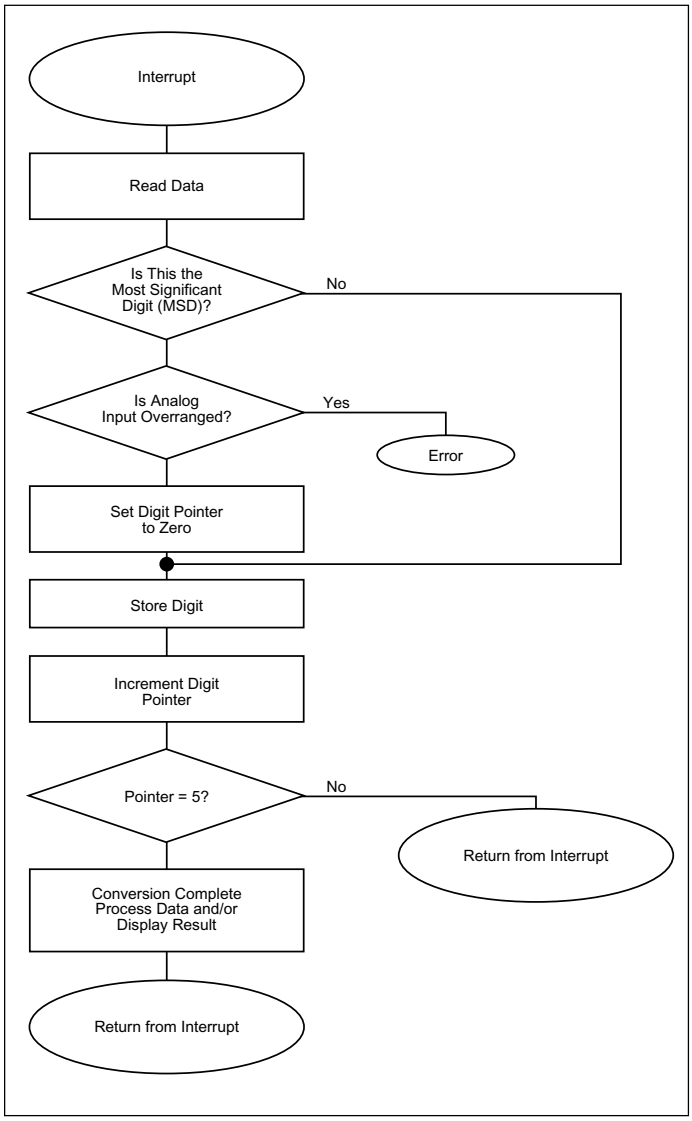


FIGURE 4: *TC7135 to 6502µP interface program flow chart.*

If DS5 is not high, or after register X is zeroed, program execution proceeds to location “NXTDIG.” The BCD data is stored in zero page memory, beginning at location “DIGSTOR” and indexed by register X. After each digit is stored, register X is incremented and compared to five. If register X equals five, the digit scan is complete and data can be processed or displayed. Register X less than five indicates the digit scan is not complete, so an RTI instruction returns operation to the main program to await another digit strobe. Other programs can use memory location XSTOR as a “Data Valid” indication: If XSTOR = 5, then 5 consecutive memory locations beginning at DIGSTOR contain the results of the latest TC7135 conversion.

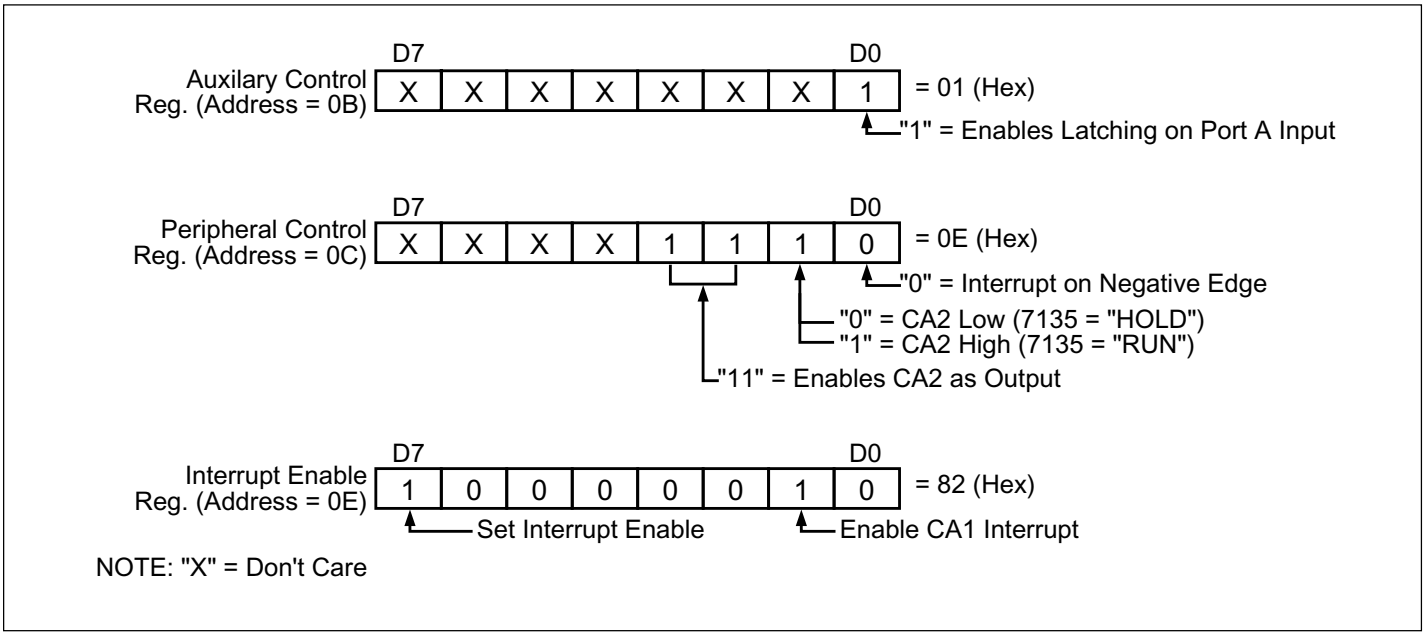
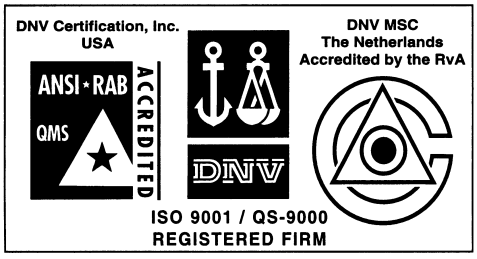


FIGURE 5: *6522 I/O port control register functions.*

Trademarks



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