AN1484

Recommended Usage of Microchip 23XX512/23XX1024 Serial SRAM Devices

Author: *Martin Bowman*
Microchip Technology Inc.

INTRODUCTION

Many embedded systems require some amount of volatile storage for temporary data. This is increasingly true when enabling the “Internet of things”. Because of their small footprint, low I/O pin requirement, low-power consumption and low cost, serial SRAMs are a popular choice for volatile storage. Microchip Technology has addressed this need by offering a line of serial SRAMs using the industry standard SPI-based communication. Serial SRAM devices are available in a number of density offerings, operational voltage ranges and packaging options. The serial SRAM products offer an alternative to the traditional parallel architecture that saves both board area and also I/O count on the MCU.

In order to achieve a highly robust application when utilizing serial SRAMs, the designer must consider more than just the data sheet specifications.

There are a number of conditions which could potentially result in non-standard operation. The most important of them are discussed in this application note. This application note is written for the 23XX512/23XX1024 family of devices. For the 23XX256/23XX640 please refer to AN1245.

This application note provides assistance and guidance with the use of Microchip advanced serial SRAMs. These recommendations are not meant as requirements, however, their adoption will lead to a more robust overall design. This document should be used along with the device data sheet. The following topics are discussed:

- Input Considerations
- Power Supply
- SPI/SDI and SQI High-Speed Serial Connections
- MODE Register
- $\overline{\text{HOLD}}$ Operation
- Operating Modes
- V_{BAT} Operation

Not all of Microchip SRAM devices support all available features. The features supported by each device are summarized in the table below:

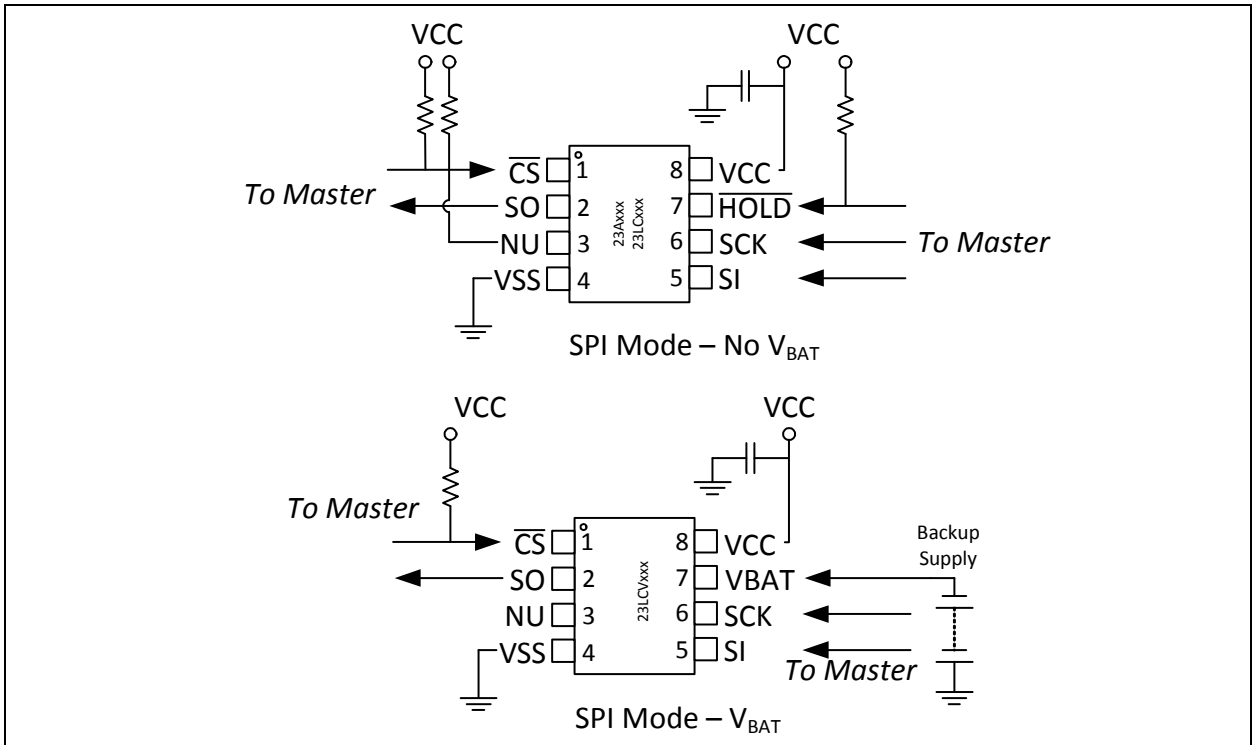
TABLE 1: DEVICE FEATURES

Device	Density	Voltage Range	Hold Pin	SPI	SDI	SQI	V_{BAT} Support	Pages
23A512	512K Bits	1.7-2.2 V	Yes	Yes	Yes	Yes	No	32B x 2048
23LC512	512K Bits	2.5-5.5 V	Yes	Yes	Yes	Yes	No	32B x 2048
23LCV512	512K Bits	2.5-5.5 V	No	Yes	Yes	No	Yes	32B x 2048
23A1024	1024K Bits	1.7-2.2 V	Yes	Yes	Yes	Yes	No	32B x 4096
23LC1024	1024K Bits	2.5-5.5 V	Yes	Yes	Yes	Yes	No	32B x 4096
23LCV1024	1024K Bits	2.5-5.5 V	No	Yes	Yes	No	Yes	32B x 4096

RECOMMENDED CONNECTIONS

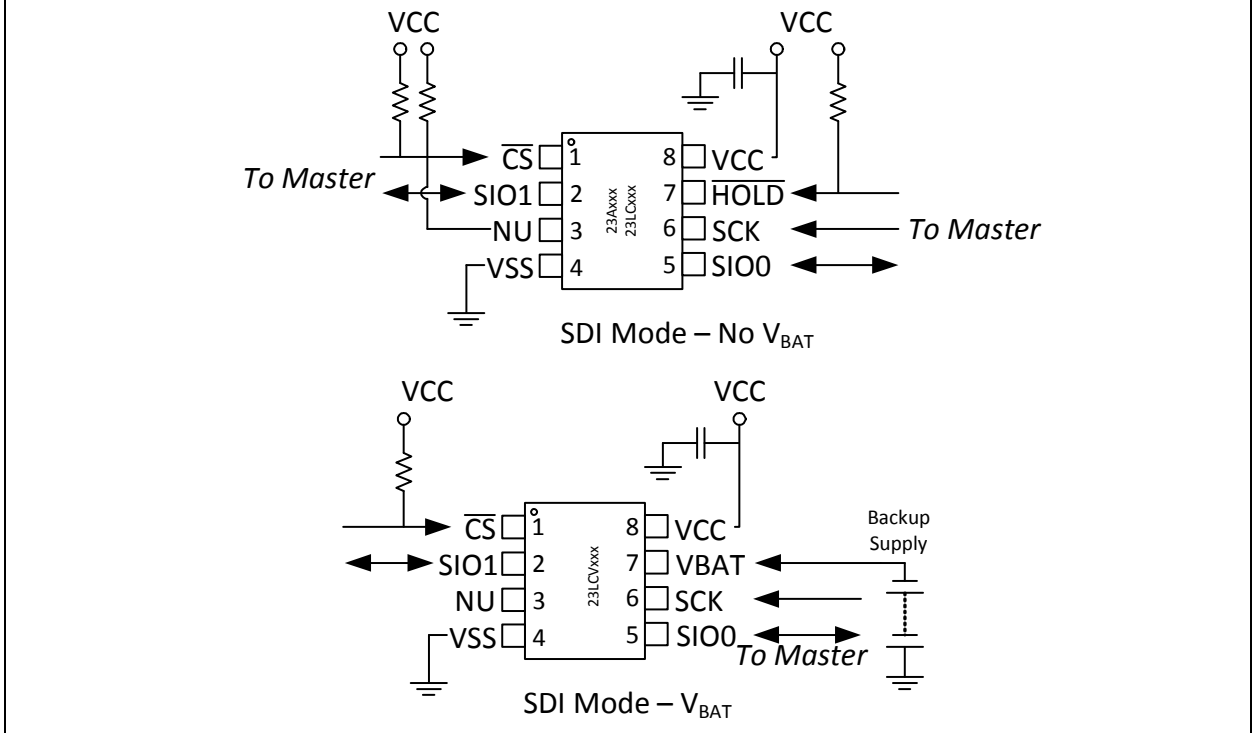
Figure 1 through Figure 3 show the recommended connections for the serial SRAM device when using SPI, SDI and SQI serial communications. The pin designated as NU in the schematics is not used in the referenced configuration and should be treated as shown in the schematic.

FIGURE 1: RECOMMENDED CONNECTIONS FOR SPI OPERATION



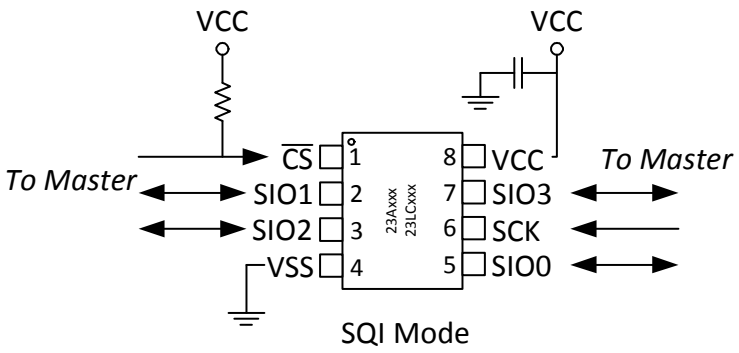
Note : A decoupling capacitor (typically 0.1 μF) should be used on VCC.
Pull-up resistors should be chosen based on the application (10K Suggested).

FIGURE 2: RECOMMENDED CONNECTIONS FOR SDI OPERATION



Note : A decoupling capacitor (typically 0.1 μF) should be used on VCC.
Pull-up resistors should be chosen based on the application (10K Suggested).

FIGURE 3: RECOMMENDED CONNECTIONS FOR SQI OPERATION



Note : A decoupling capacitor (typically 0.1 μF) should be used on VCC.
Pull-up resistors should be chosen based on the application (10K Suggested).

INPUT CONSIDERATIONS

It is never good practice to leave an input pin floating. This can cause high standby current as well as undesired functionality. If a pin is left floating, it can either float low or high. Which direction the signal goes is dependent upon a number of factors, including noise in the system and capacitive coupling. Because of this, the level seen by the input circuitry is relatively random and likely to change during operation.

Such unpredictable input levels can have devastating effects on device operation. For example, Microchip's SPI serial SRAMs feature a $\overline{\text{HOLD}}$ pin on some devices which allows the user to suspend the clock mid-stream. If this pin were to float low (active), the device would no longer react to any clock pulses received, communication would be disrupted and data potentially lost or corrupted.

Therefore, any unused input pins should always be tied to a proper level, such as high for an active-low input. Moreover, it is recommended that, if the microcontroller has extra, tri-state I/O pins available, connections be made to these unused inputs along with a pull-down/pull-up resistor, as shown in Figure 1. This will allow for the inputs to be used at a later date simply by modifying firmware.

Although the $\overline{\text{CS}}$ pin should always be driven by the microcontroller during normal operation, it has potential for floating during power-down/power-up. As such, this pin should also have a pull-up resistor to avoid undesired commands due to noise during these conditions.

POWER SUPPLY

Microchip SPI serial SRAMs feature a robust serial communication protocol that helps to prevent unintentional writes and data corruption while power is within normal operating levels. But, certain considerations should be made regarding power-up and power-down conditions to ensure the same level of protection during those times when power is not within normal operating levels.

As shown in Figure 1, a decoupling capacitor (typically 0.1 μF) should be used to help filter out small ripples on V_{CC}.

Power-Up

On power-up, V_{CC} should always begin at 0V and rise straight to its normal operating level to ensure a proper Power-on Reset. V_{CC} should not remain at an ambiguous level (i.e., below the minimum operating voltage).

However, if V_{CC} happens to fall below the minimum retention voltage of the device (see data sheet DC Characteristics), it is recommended that V_{CC} be brought down fully to 0V before returning to normal operating level. This will help to ensure that the device is reset properly.

Furthermore, if the microcontroller features a Brown-out Reset with a threshold higher than that of the serial SRAM, bringing V_{CC} down to 0V will allow both devices to be reset together. Otherwise, the microcontroller may reset during communication while the SRAM is still in an operational condition.

Power Failure During a Write

During the time that data is being written to the SRAM V_{DD} should remain above the minimum operating voltage. If at any time V_{DD} drops below this minimum voltage but remains above the retention voltage, (as specified in the product data sheet) care should be taken to ensure that the data written to the device is free from errors.

SPI OPERATION

During normal SPI operation the following pins are used for device communication:

- $\overline{\text{CS}}$ – Chip Select active low
- SO – Data from the SRAM
- SI – Data to the SRAM
- SCK – Serial data clock

Pin 3 – SIO2 (available on 23AXXX and 23LCXXX devices) is used for SQI mode of operation. As this is an input pin, this should not be left floating. This pin may be connected to either V_{SS} or V_{CC}. It is recommended that this pin be connected to V_{CC} in the event that the device enters SQI mode, as this pin will need to be high to exit SQI.

For the 23LCVXXX devices, pin 3 is internally tied high, so can be treated as a true No Connect.

SDI OPERATION

SDI operation uses the same physical pins as SPI, however, both the SI and SO pins become SIO0 and SIO1.

Pin 3 – SIO2 (available on 23AXXX and 23LCXXX devices) is used for SQI mode of operation. As this is an input pin, it should not be left floating. It may be connected to either VSS or VCC. It is recommended that this pin be connected to VCC in the event that the device enters SQI mode, as this pin will need to be high to exit SQI mode. The following pins are used in SDI communication mode:

- $\overline{CS}$ – Chip Select active low
- SIO0 – Bidirectional data line (LSB)
- SIO1 – Bidirectional data line (MSB)
- SCK – Serial data clock

To enter SDI mode of operation the EDIO command must be issued. Upon completion of this command, the device will be expecting data and commands to be issued in SDI mode. The device can return to SPI mode by issuing the RSTIO command.

In SDI mode data is sent to the SRAM on the rising edge of the clock, 2 bits per clock, with both the SIO0 and SIO1 pins being bidirectional. In this mode, the data rate to and from the serial SRAM is 2x SPI mode.

As there is a finite time for both the SIO0 and SIO1 lines to change from input to output when reading data from the device, there is a dummy byte inserted between the address and the first data byte clocked from the SRAM, as shown in the product data sheet.

SQI OPERATION

SQI mode operates on the same principle as SDI, however, there are four bidirectional data lines. Because of the extra data line, the $\overline{HOLD}$ function is disabled and VBAT is not available when operating in SQI mode. The following pins are used in SQI communication mode:

- $\overline{CS}$ – Chip Select active low
- SIO0 – Bidirectional data line (LSB)
- SIO1 – Bidirectional data line
- SIO2 – Bidirectional data line
- SIO3 – Bidirectional data line (MSB)
- SCK – Serial data clock

To enter SQI mode of operation the EQIO command must be issued. Upon completion of this command, the device will be expecting data and commands to be issued in SQI mode. The device can return to SPI mode by issuing the RSTIO command.

In SQI mode data is sent to the SRAM on the rising edge of the clock, 4 bits per clock, giving 4x the data throughput of standard SPI mode.

As there is a finite time for the bidirectional data lines to change from input to output when reading data from the device, there is a dummy byte inserted between the address and the first data byte clocked from the SRAM.

MODE REGISTER

Microchip SPI serial SRAMs feature a MODE register. The MODE register is used to control features of the device and is a read/write register. Bits within the MODE register are used to control the operating mode:

- Byte mode
- Page mode
- Sequential mode

The MODE register is accessed through the Read Mode Register (RDMR) and Write Mode Register (WRMR) commands. Unused bits should always be written as '0'.

HOLD FEATURE

The $\overline{HOLD}$ feature is not available on devices with VBAT support (23LCVXXX) or when SQI mode is enabled.

OPERATING MODES

The Microchip serial SRAM has three operating modes.

Byte Mode

Byte mode is selected when bits <7:6> in the STATUS register are set to '00'. In this mode, all read and write operations are limited to the byte that is addressed, with the address clocked into the device after the instruction. The user can read or write to the same byte continuously until the $\overline{CS}$ line is brought high, terminating the command. The internal Address Pointer is not incremented.

Page Mode

Page mode is selected when bits <7:6> in the STATUS register are set to '10'. In this mode, read and write operations are limited to the current page that is addressed, with the address following the instruction.

The serial SRAM has a page size of 32 bytes, with either 2048 pages (23XXX512) or 4096 pages (23XXX1024). In Page mode the user can either read data from or write data to the current page. As the internal Address Pointer is incremented, at the end of the page boundary it will roll over to the beginning of the current page. If a write is being executed, the data at the beginning of the page will be overwritten. The address sent after the instruction does not have to be aligned to a page boundary.

Sequential Mode (Default)

Sequential mode is selected when bits <7:6> in the STATUS register are set to '01'. In this mode, read and write operations can be performed on the whole array.

The address sent after the instruction is the first array location that will be read from or written to. With each subsequent data byte, the internal Address Pointer is incremented. At any point, the read or write sequence can be terminated by raising $\overline{CS}$. At the end of the SRAM array, the internal Address Pointer will roll-over to 0x00000 (23XXX1024) or 0x0000 (23XXX512).

VBAT OPERATION

This section details special considerations for using the VBAT mode of operation. The internal VBAT switch allows the data stored in the SRAM array to be retained when VCC is no longer available. Care should be taken to ensure that the VBAT voltage specification is not exceeded.

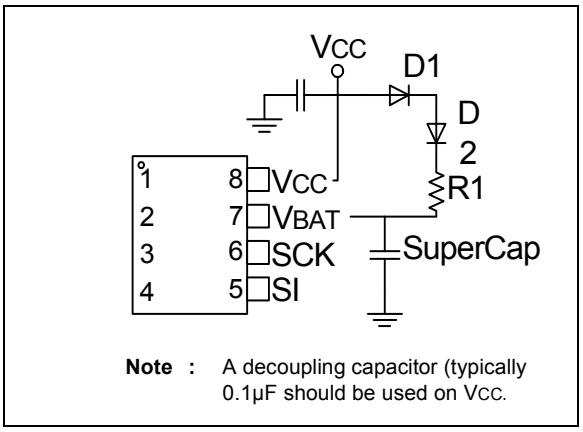
The SRAM array is powered from the external VBAT supply when the VCC voltage drops below the VTRIP level (see data sheet specification). During this time the SRAM will not respond to any communications over the SPI/SDI bus.

The current required to maintain the SRAM contents is significantly lower than the VCC current, allowing the use of a backup battery with a low capacity. Recommended backup supply examples are detailed below – this is not an exhaustive list as other options exist.

The recommended electrical connections for an external primary (non-rechargeable) battery are shown in Figure 1 and Figure 2 for both SPI and SDI operation. No additional components are required for VBAT operation with a primary battery such as a coin cell.

When using a backup supply based around a Super Cap, the following schematic shows the recommended external connections. D1 and D2 are used to both limit the maximum voltage to the Super Cap and the VBAT pin. R1 is used to limit the current to the Super Cap.

FIGURE 4: SUPER CAP SCHEMATIC



Note : A decoupling capacitor (typically 0.1µF should be used on VCC.

Additional care should be exercised when using a backup supply that is designed to be recharged, such as a NiCad backup battery. In this case, care must be taken to ensure that the battery cannot be over charged. The above circuit (Figure 4) can be used for a NiCad battery if the resistor R1 is chosen so that the charge current is within the allowable limits of the battery.

SUMMARY

This application note illustrates recommended techniques for increasing design robustness when using Microchip advanced SPI serial SRAMs. These recommendations fall directly in line with how Microchip designs, manufactures, qualifies and tests its serial SRAMs, and will allow the devices to operate within the data sheet parameters. It also serves to explain in detail some of the features of the device and makes the user aware of any potential pitfalls that they may fall into.

NOTES:

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