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Combining the CLC and NCO to Implement a High Resolution PWM

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INTRODUCTION

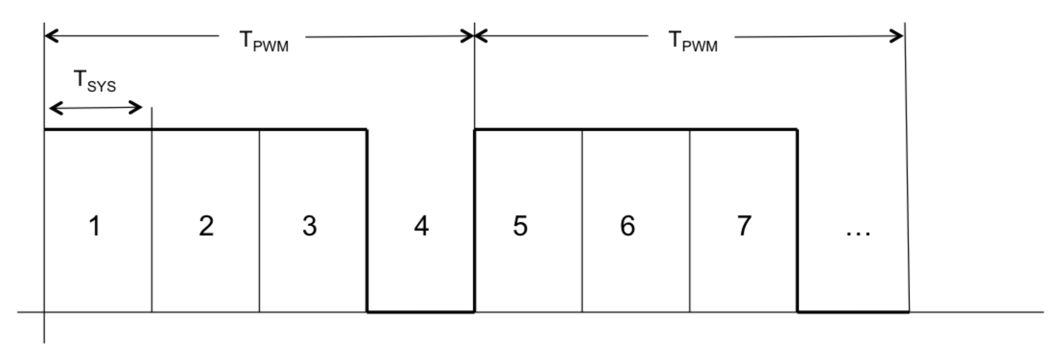
Although many applications can function with PWM resolutions of less than 8 bits, there is a range of applications, such as dimming of lamps, where higher resolution is required due to the sensitivity of the human eye.

BACKGROUND

A conventional PWM uses a timer to produce a regular switching frequency (T_{PWM}), and then uses a ripple counter to determine how many clocks the output is held high before the pulse ends.

The output pulse width is adjusted as indicated in Figure 1 to produce, in this case, a PWM with five possible duty cycle settings (0%, 25%, 50%, 75% or 100%).

FIGURE 1: CONVENTIONAL PWM



The effective resolution (measured in bits) of a PWM can be calculated by taking the base-2 logarithm of the number of pulse width settings (N) possible.

EQUATION 1:

$$Resolution = log_2(N)$$

For a device running at 16 MHz, the smallest duty cycle adjustment increment would be 62.5 ns (one system clock). If the PWM is configured to run at a switching frequency of 200 kHz (switching period of 5 us), 100% duty cycle will be achieved when the duty cycle register is set to 80 clocks (80 x 62.5 ns = 5 us). This would make the effective PWM resolution only slightly more than 6 bits, as we have 80 steps to choose from. This is because one system clock divides into one period 80 times.

Knowing that we have 80 possible duty cycle steps, a precise value for the resolution of the PWM can be calculated as follows (Equation 2):

EQUATION 2:

$$log_2 80 = 6.32 \text{ bits}$$

A PWM running from a 16 MHz clock, which has a 10-bit duty cycle register, will start losing resolution due to this limitation at a 15.6 kHz switching frequency. For higher PWM switching frequencies, the duty cycle will reach 100% before all of the steps in the 10-bit duty cycle register have been used, and for all the remaining values the output will simply remain at 100% duty cycle.

The frequency at which this point is reached can be calculated as follows (Equation 3):

EQUATION 3:

$$\frac{Fosc}{\#\text{Steps}} = \frac{16MHz}{2^{10}} = \frac{16,000,000}{1024} = 15.6\ kHz$$

In most PWM applications, the PWM is switched at a much higher frequency than the output can ever change. By filtering this PWM signal using a low-pass filter, the desired output is obtained. The filter removes the high frequency switching components of the PWM by essentially calculating the average value of the PWM signal, and presents this as the output. For example, if we are constructing a switching power supply, the output voltage will be directly proportional to the duty cycle. The consequence of this relationship is that the smaller the adjustment we can make to the PWM duty cycle, the smaller the resulting change to the output will be resulting in more precise control of the output.

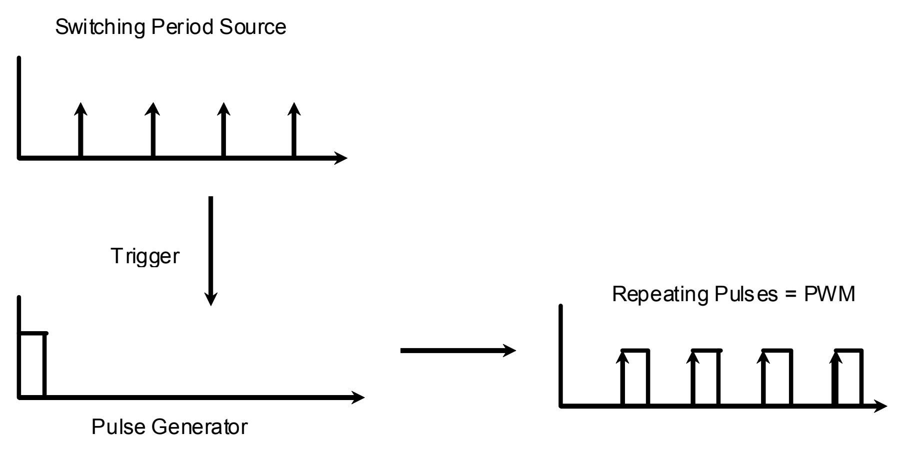
From a control systems point of view, being able to make small adjustments to the output effectively lowers the quantization gain introduced by the PWM. In control systems, this lowering of the gain is important to ensure stability of the system.

DESIGN

PWM Construction

In principal, a PWM is created by the combination of two parameters. The first being a repeating trigger, which determines how often we pulse (the switching period or switching frequency), and the second being a single pulse generator, which determines how wide the pulse is (the duty cycle). This is illustrated in Figure 2.

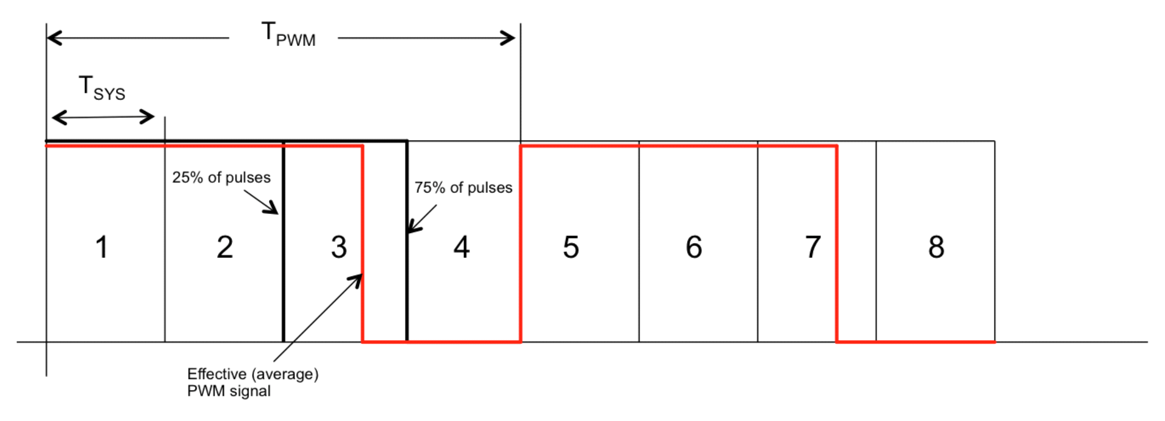
FIGURE 2: PWM CONSTRUCTION



In order to achieve an increase in the effective PWM resolution, we will be using the NCO peripheral on the PIC® device to create a monostable circuit (a circuit that gives a single pulse of fixed duration when triggered).

We will use the ability of the NCO to generate a signal that varies between two values in a defined proportion, creating an average pulse width, which is somewhere in between two system clocks, as illustrated in Figure 3. The PWM signal pulse width will vary (jitter/dither) by one clock period, with the proportion/ratio of the variation precisely determined by the NCO configuration.

FIGURE 3: NCO BASED PWM OPERATION

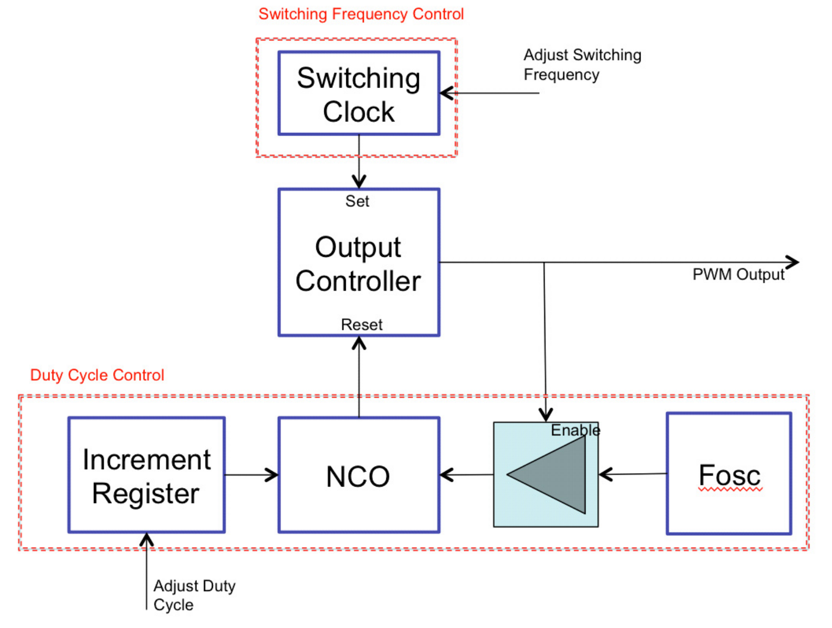


In any application where the output is producing an average value (e.g., average power transfer to the load in SMPS or lighting applications), the variation in pulse width will be perfectly acceptable, because the average pulse width is accurately controlled.

By itself, the NCO peripheral cannot produce a PWM signal, but we will change its behavior by adding some logic using the CLC to produce a PWM output.

We will achieve this by using the conventional PWM as a clock source to trigger the PWM period, and use the NCO to determine the pulse width. Any number of clock sources could be used (e.g., Timers or even external signals), and in some applications we may even desire using an external trigger to start the pulses, such as a zero current detection circuit, if we are building a power supply. A simplified block diagram of how this will work is shown in Figure 4.

FIGURE 4: NCO BASED PWM PRINCIPLE OF OPERATION



The control logic in the CLC is used to set an output when the switching clock indicates that it is time for the next pulse, and clear this output to complete the pulse once the NCO overflows.

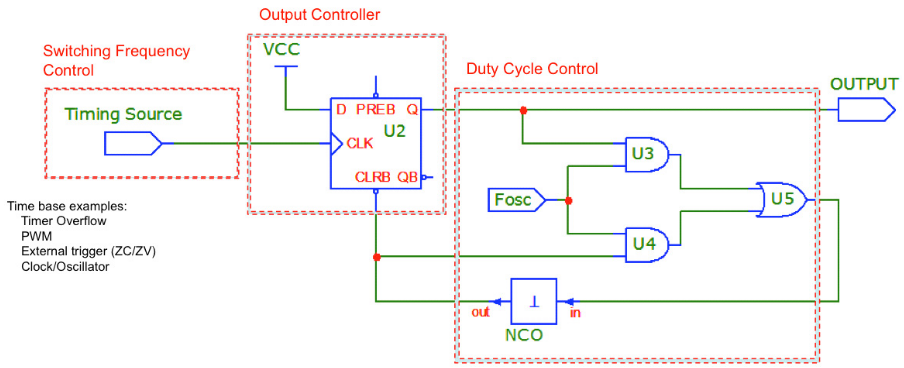
IMPLEMENTATION USING CLC AND NCO

An implementation of this design using the NCO and CLC is shown in Figure 5. For this design, the NCO is placed in Pulse Frequency mode. In this mode of operation, a short pulse is produced when the NCO overflows.

The operation of the circuit can be described as follows:

1. The flip-flop will clock on the positive edge of the timing signal. This will cause the Q output to go high and the PWM pulse to start.
2. As the output goes high, the AND gate U3 combines this output signal with a high-speed clock which is fed into the NCO clock pin via U5. At this point, the NCO output is low and U4 is not producing any output.
3. When the NCO overflows, the NCO output goes high, which resets the flip-flop, forcing the Q output of the flip-flop to go low. U3 is now inactive due one of the two inputs of the gate being low.
4. U4 is used to get the NCO back to a stable state, as it needs an additional clock to return the NCO output to low. Once the NCO output returns to low, U4 will also produce no clock output and the system will be in a stable state with the output low.
5. When the next positive edge from the timing source is received the process is repeated from step 1 above. The amount of time it takes the NCO to overflow will depend on the remainder left in the accumulator after the last overflow, as well as the increment register. Due to the accumulation of remainders the pulse will sometimes be one system clock shorter than usual. By controlling how often this happens (setting the increment register), we can control exactly what the average pulse width will be.

FIGURE 5: PWM IMPLEMENTATION USING CLC AND NCO



CALCULATIONS

The calculation of the pulse width will be according to the NCO overflow frequency calculation, as listed in the data sheet.

EQUATION 4:

$$F_{OUT} = F_{NCO} \times \frac{Increment}{2^n}$$

The average overflow frequency of the NCO will determine the average output pulse width (T_{PULSE}) produced.

EQUATION 5:

$$T_{PULSE} = \frac{1}{F_{OUT}}$$

Table 1 below shows the pulse width, which this circuit will produce using a 16 MHz clock connected directly to the NCO clock input (F_{NCO}), given various increment register values. Note that, for high increment values, a single increment of the register will change the pulse width by a mere 15 ps.

TABLE 1: CALCULATED PWM PULSE WIDTH FOR DIFFERENT INCREMENT REGISTER VALUES

Increment Value	NCO F_{OUT} (Hz)	Average Pulse Width (ns)
65000	991,821	1,008.246
65001	991,837	1,008.231
20000	305,176	3,276.800
20001	305,191	3,276.636
100	1,526	655,360.000
101	1,541	648,871.287

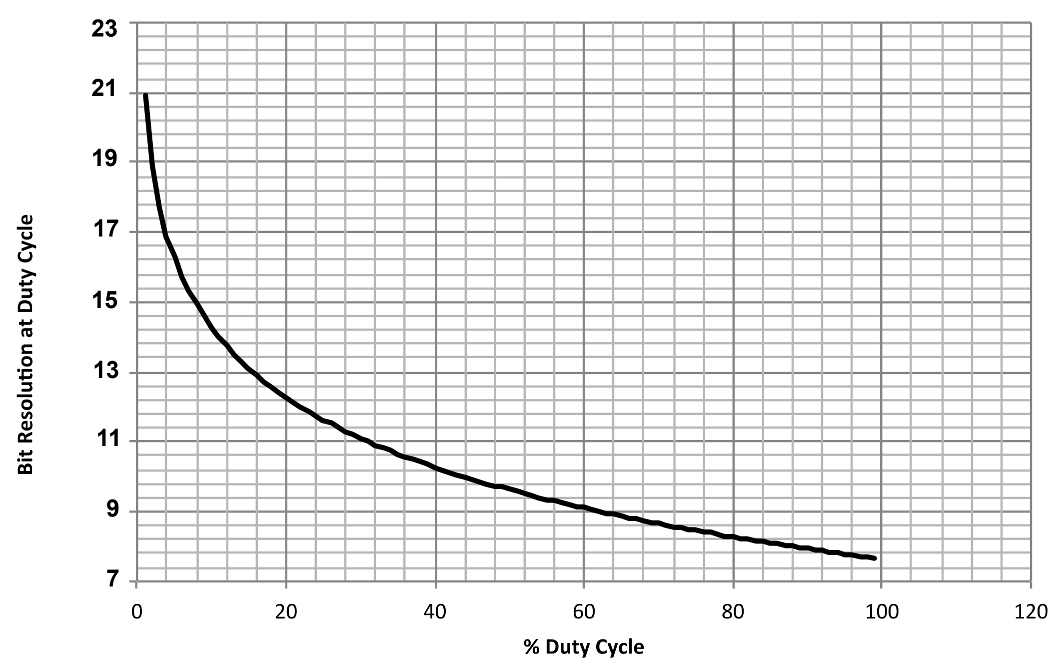
CHARACTERISTICS

It is important to note that the NCO is designed to give linear control over frequency. The control over pulse width is subsequently not linear. As can be seen from the equation for calculating T_{PULSE} above (Equation 5), the pulse width will vary with the inverse of the frequency (1/x).

The result is that the effective resolution of the PWM is not constant over the entire range from 0% to 100% duty cycle.

For every duty cycle setting, we can calculate the effective resolution at this particular point, and plot this on a graphic. This curve will look different depending on what the switching frequency is, because we are adjusting the pulse width independently from the switching frequency. For a F_{SW} = 3 kHz and a 16 MHz clock, the graphic will look as follows (Figure 6).

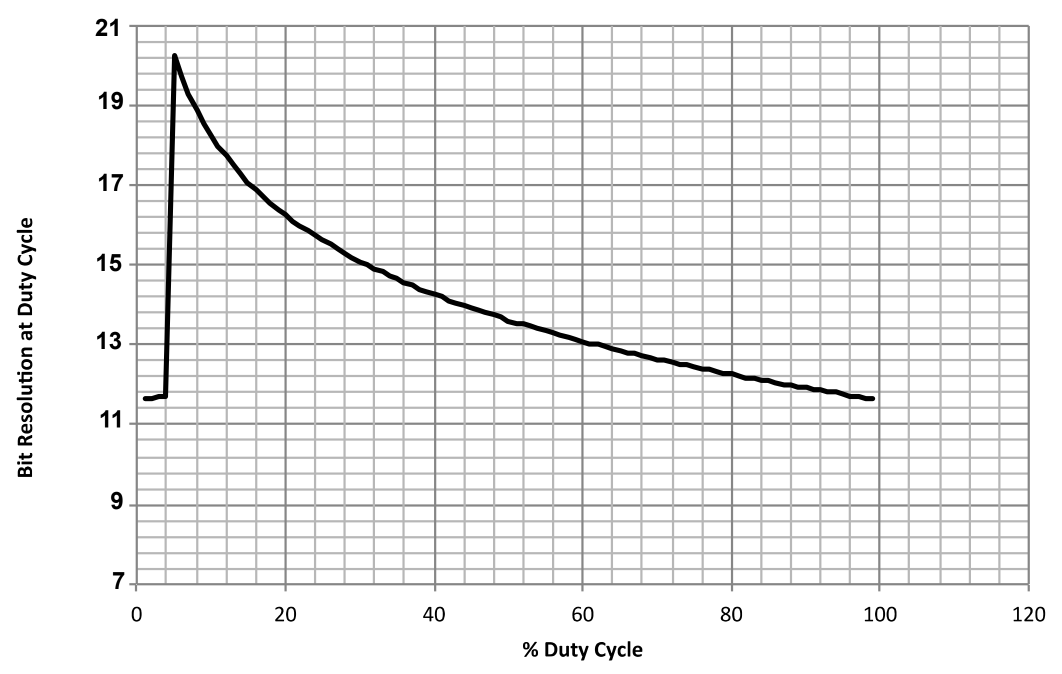
FIGURE 6: HIGH RES PWM RESOLUTION PLOTTED AGAINST DUTY CYCLE (CLOCK = 16 MHz, FSW = 3 kHz)



Although we have an equivalent 21 bits of resolution close to 0% duty cycle, this deteriorates to only 7.5 bits of resolution at 100% duty cycle, at which point the conventional PWM would outperform our High-Resolution implementation.

Interestingly, and perhaps counter-intuitively, we can improve the resolution by decreasing the NCO input clock frequency. Reducing this clock to 1 MHz will have the result shown below (Figure 7).

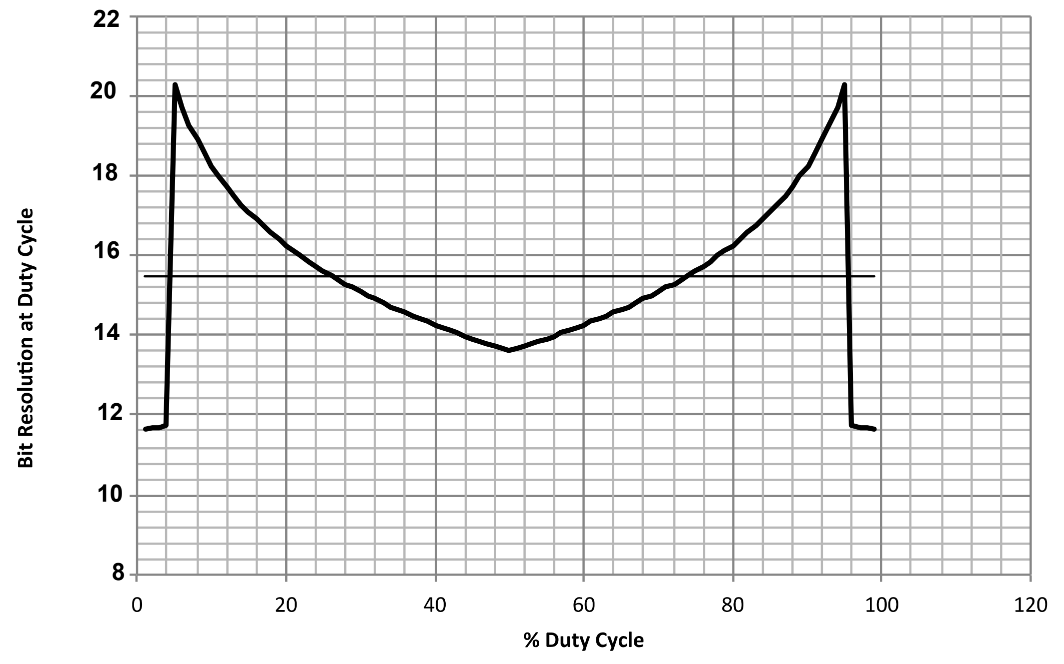
FIGURE 7: HIGH RES PWM RESOLUTION PLOTTED AGAINST DUTY CYCLE (CLOCK = 1 MHz, FSW = 3 kHz)



There is, of course, a limitation, as can be seen, close to 0% duty cycle, where the increment register maximum value is reached and smaller pulses cannot be generated any more, but the resolution now never reduces to less than 11 bits.

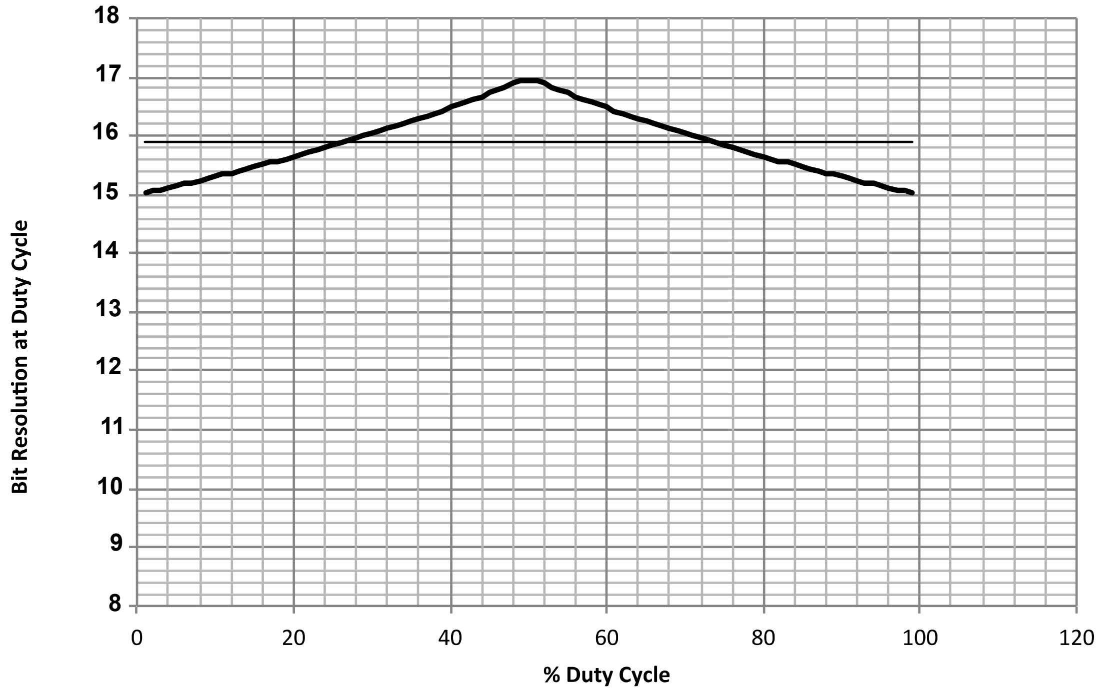
One way to improve the performance would be to invert the PWM signal when we exceed 50% duty cycle. By doing this we can effectively mirror the performance under 50% duty cycle to the region above it, with the higher resolution. We still have the option to use the original curve where the limits of the increment are reached. This results in the following graphic (Figure 8) for the same conditions as the graphic above.

FIGURE 8: RESOLUTION VS DUTY CYCLE WITH SIGNAL INVERSION AT 50% DUTY CYCLE (CLOCK = 1 MHz, FSW = 3 kHz)



When it is our intention to achieve both the highest possible switching frequency, and the highest resolution using this technique, we will use a configuration as shown below (Figure 9). This graphic shows the achievable resolution when using a 16 MHz clock at a switching frequency of 500 kHz.

FIGURE 9: HIGH RES PWM RESOLUTION PLOTTED AGAINST DUTY CYCLE WITH INVERSION AT 50% (CLOCK = 16 MHz, FSW = 500 kHz)



SUMMARY

Conventional PWM's start losing effective resolution at relatively low switching frequencies. For applications where the switching frequencies have to be fairly high, and having as much PWM resolution as possible at these frequencies is necessary, the NCO can be used in conjunction with the CLC to create a very high resolution PWM output.

The smallest incremental change in pulse width achievable by a conventional PWM with a 16 MHz system clock speed would be 62.5 ns. If the fastest available PWM clock is FOSC/4, then this increases to 250 ns.

On the same device, a PWM with an incremental pulse width change of as little as 15 ps can be constructed using the technique described in this application note.

Even if the requirement is not primarily high resolution, this solution may still be attractive for a number of applications, adding an additional PWM to the capability of the device, or having a constant on/off-time variable frequency PWM, where the pulse is triggered externally as required, when doing zero current switching in high efficiency power converters.

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