AN1470

Manchester Decoder Using the CLC and NCO

Authors: *Jatinder Gharoo*
Brian Bailey
Microchip Technology Inc.

ABSTRACT

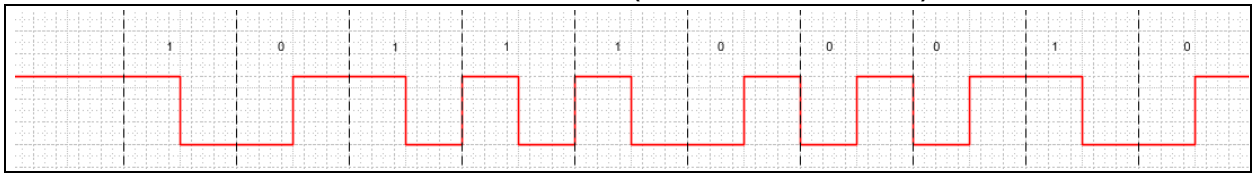
A Manchester decoder can be built using Microchip's award winning CLC (Configurable Logic Cell) blocks and NCO (Numerically Controlled Oscillator) available in the PIC16F150x devices. The PIC16F150x devices are Microchip's new enhanced core devices featuring low-power XLP technology. The decoder requires little firmware support and, therefore, requires very few CPU cycles after the modules are initialized. Data and clock can be directed to the internal SPI module for data capture at rates of up to 500 kbps.

INTRODUCTION

Manchester encoding is used in a wide range of applications in telecommunication and data storage. It is used in systems for its simplicity and synchronization benefits. A transition is ensured at least once every bit, allowing the receiving device to recover clock and data. It has no DC component, which means that it may be coupled inductively or capacitively. A typical application requires a Manchester data encoder used to transmit data, and a receiver on the other end that decodes data. The objective of this document is to demonstrate how the NCO and CLC peripherals found on PIC16F devices can be used as a Manchester Decoder. Traditional algorithms can be firmware intensive and leave very small amount of CPU cycles to service other application needs. The following approach involves using blocks that operate independently of the CPU clock and have zero CPU utilization, allowing designers to service their applications along with data encoding and decoding.

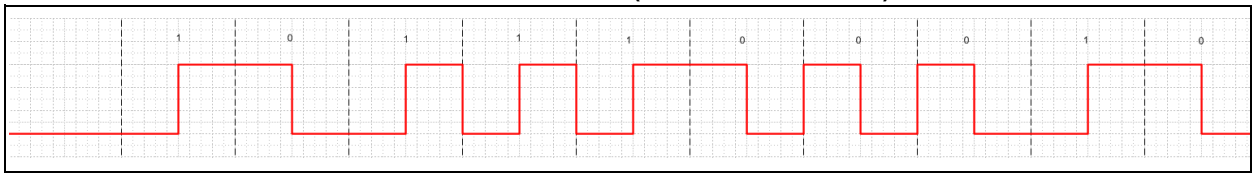
Depending on the encoding standard, data is available during the first or second half of bit time. There are two standards of Manchester encoded signals used in the industry. Manchester encoded signal as per G.E. Thomas (Figure 1), a '0' is transmitted by low-to-high transition and a '1' is expressed by high-to-low transition:

FIGURE 1: MANCHESTER ENCODED DATA (AS PER G.E. THOMAS)



Manchester encoded signal as per IEEE 802.3 (Figure 2) is the opposite of G.E. Thomas, where a '0' is transmitted by high-to-low transition:

FIGURE 2: MANCHESTER ENCODED DATA (AS PER IEEE 802.3)



CONFIGURABLE LOGIC CELL

This section describes a Manchester decoding implementation using the CLC blocks of PIC16F150x microcontrollers. The Configurable Logic Cell (CLC) provides programmable logic that operates outside the limitation of CPU execution. The logic cell allows signal multiplexing from other peripherals, input pins or register bits through the use of configurable gates that drive selectable single-output logic functions. The output of each CLC block can be directed internally to peripherals, other CLC blocks and to an output pin. Possible configurations include eight logic functions:

- AND-OR
- OR-XOR
- AND
- S-R Latch
- D Flip-flop with Set and Reset
- D Flip-flop with Reset
- J-K flip-flop with Reset
- Transparent Latch with Set and Reset

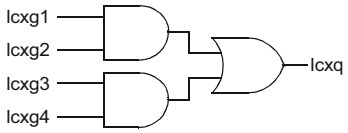
Logic functions are shown in Figure 3. Each logic function has four inputs and one output. The four inputs are the four data gate outputs of the previous stage.

CLC CONFIGURATION TOOL

The CLC is a complex peripheral with multiple combinations and sequential circuits that can be pre-programmed or configured dynamically. This allows flexibility, but also makes configuration and setup very complex. The CLC configuration tool provided by Microchip makes the setup process of the CLC module easier to implement and understand. It is worthwhile mentioning that any gate with an unconnected input will be read as a logic zero. To input a logic one as an input to a gate or latch, the zero can be inverted. See **"Appendix A "** for configuration snapshots of the tool.

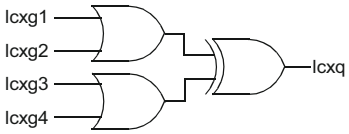
FIGURE 3: CLC FUNCTIONS

AND - OR



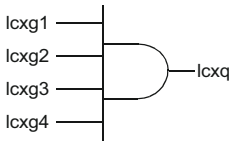
LCxMODE<2:0>= 000

OR - XOR



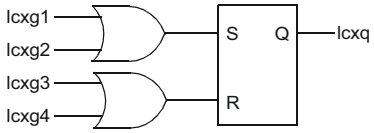
LCxMODE<2:0>= 001

4-Input AND



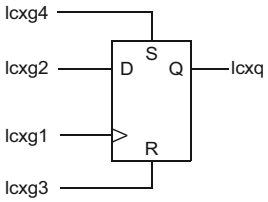
LCxMODE<2:0>= 010

S-R Latch



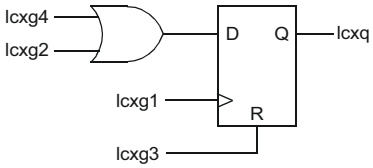
LCxMODE<2:0>= 011

1-Input D Flip-Flop with S and R



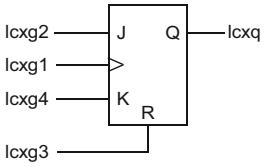
LCxMODE<2:0>= 100

2-Input D Flip-Flop with R



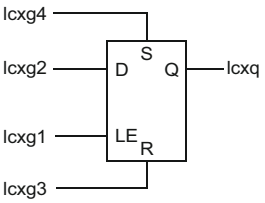
LCxMODE<2:0>= 101

J-K Flip-Flop with R



LCxMODE<2:0>= 110

1-Input Transparent Latch with S and R



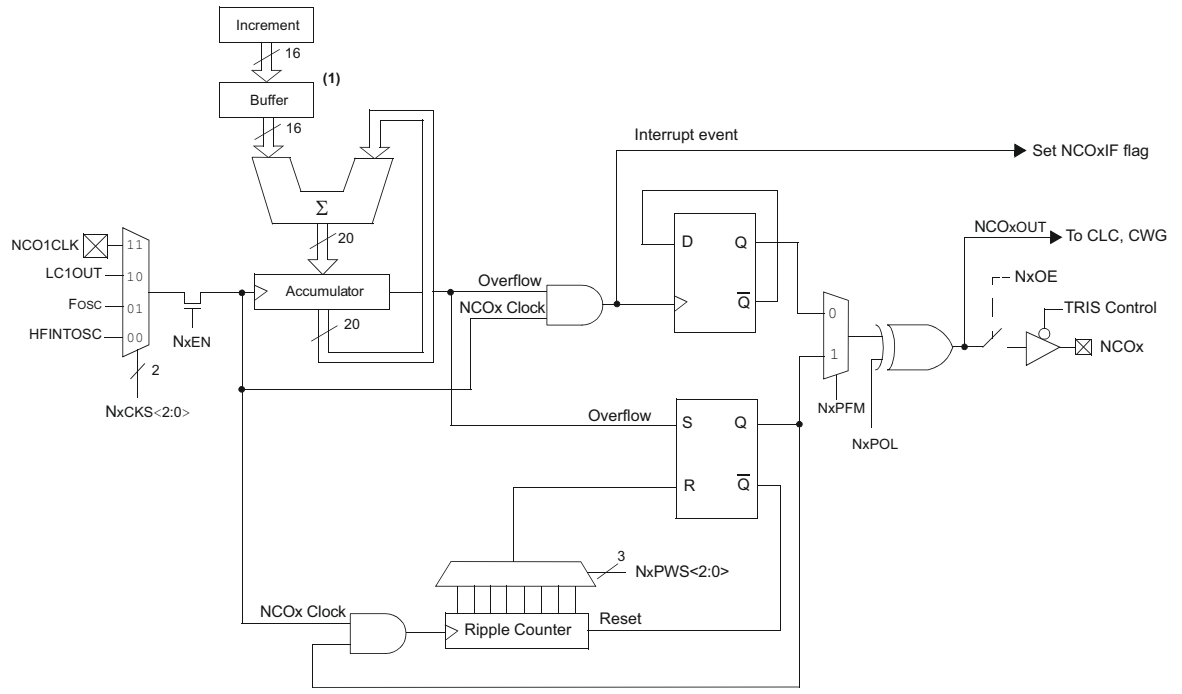
LCxMODE<2:0>= 111

NUMERICALLY CONTROLLED OSCILLATOR

The NCO module as shown in Figure 4 is a timer that uses a 16-bit increment register to add to a 20-bit accumulator to divide the input frequency. The NCO is most useful in applications that require frequency accuracy and fine resolution at a fixed duty cycle. Some features of the NCO include:

- 16-bit increment function
- Fixed Duty Cycle (FDC) mode
- Pulse Frequency (PF) mode
- Output pulse width control
- Multiple clock input sources
- Output polarity control
- Interrupt capability

FIGURE 4: NCO BLOCK DIAGRAM



Note 1: The increment registers are double-buffered to allow for value changes to be made without first disabling the NCOx module. They are shown here for reference. The buffers are not user-accessible.

One of the key features of the NCO is the ability to generate a pulsed output every time the accumulator overflows. The output becomes active for specified clock periods. The output returns to an inactive state once the clock period expires.

MANCHESTER DECODER

The approach described in this section and hereafter is based on Manchester encoding as per G.E.Thomas described in Figure 1. The method is flexible and can be easily ported to IEEE 802.3. There are several variations and considerations required for the first transition based on the Idle states of modules, power-up configuration of microcontroller pins and the first bit received (transition based on encoding method). Start-up and Idle states will be discussed in the **Section "Synchronization"** of this document.

The CLC modules are very flexible and can be easily applied to a wide range of scenarios by inverting the input or output polarities of each individual blocks. The NCO module's Idle state can also be controlled in the software. The methods discussed below assume that data is available during the first half of each bit time.

Let's take an example of the following encoded bit-stream as per G.E. Thomas encoding (Figure 5).

This signal will be decoded into its clock and data line, as shown in Figure 6.

FIGURE 5: ENCODED BIT STREAM

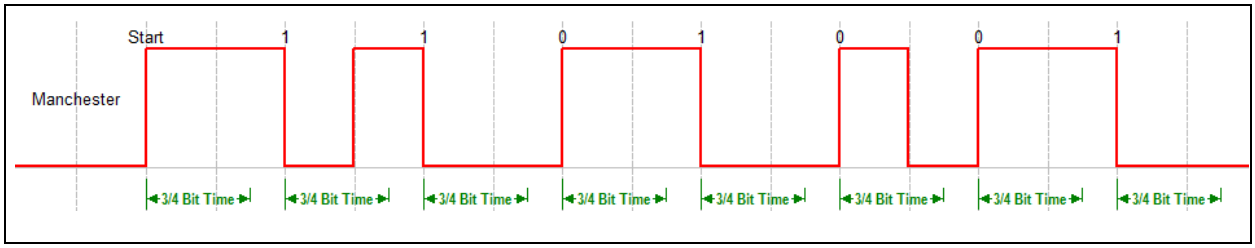
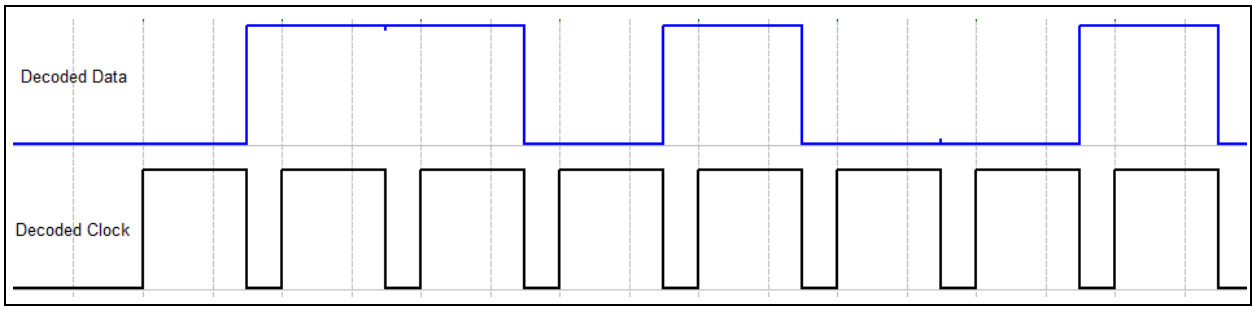
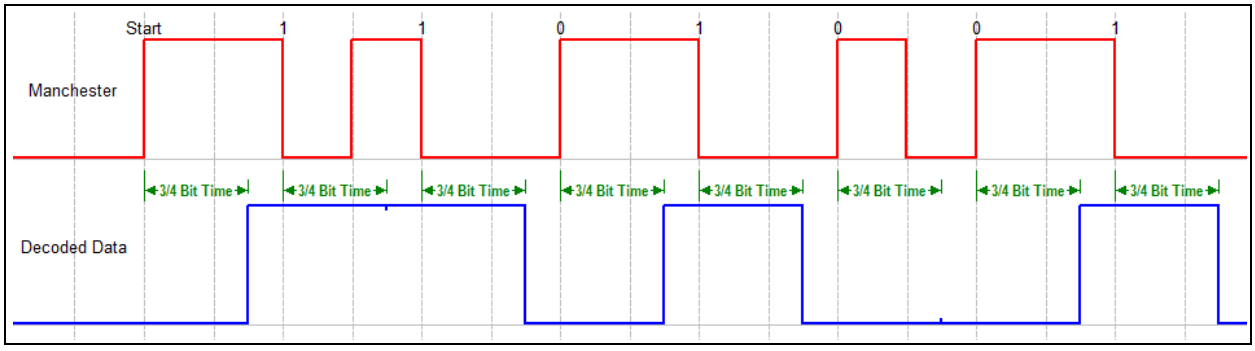


FIGURE 6: DATA AND CLOCK LINE



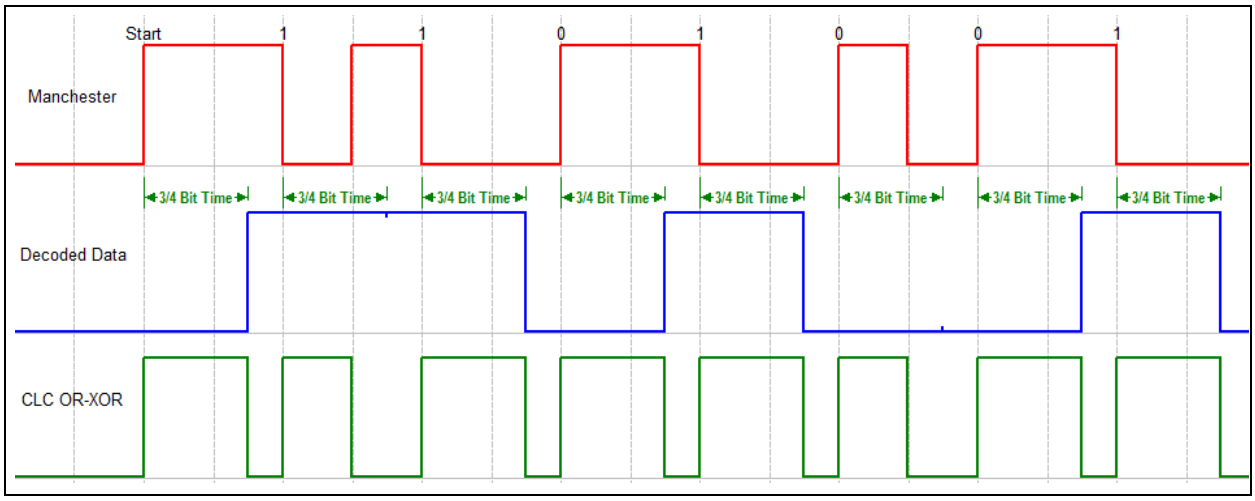
Two key points to note from this bit stream are that the bit value is present in the first half of each bit time, before the mid-bit transition. There is a transition in the middle of each bit period. This allows us to use the mid-bit transition as a trigger for NCO and use ¾ bit time to overflow and capture the next bit value (Figure 7). This ¾ bit time allows up to +/- ¼ bit time of error.

FIGURE 7: DATA CAPTURE



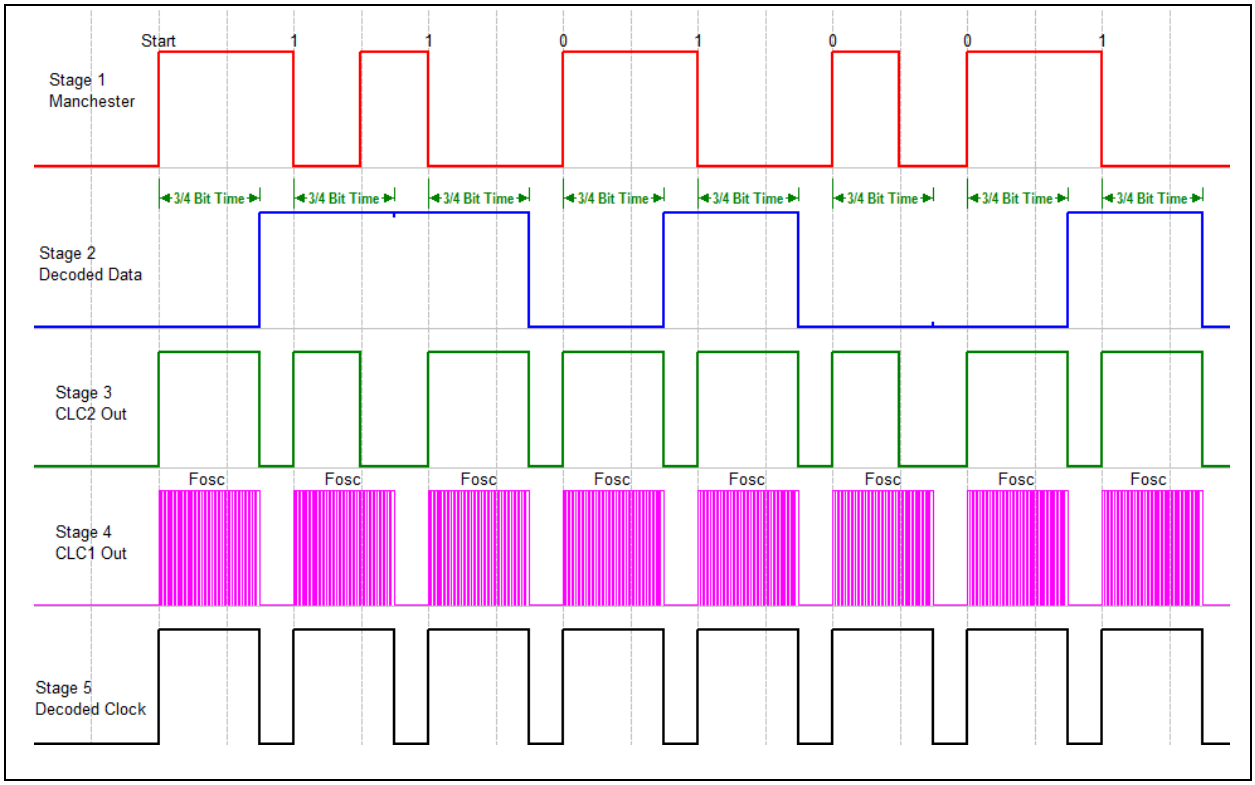
CLC block in OR-XOR configuration is used to extract clock out of this configuration (Figure 8).

FIGURE 8: CLOCK EXTRACTION



This essentially is our Manchester decoder, where CLC OR-XOR is clock and *D* is data. If we use the rising edge of a clock signal to capture data from *D*, we notice that every bit except the first one is decoded. The issue can be resolved in several ways, which will be discussed in the **Section "Synchronization"**.

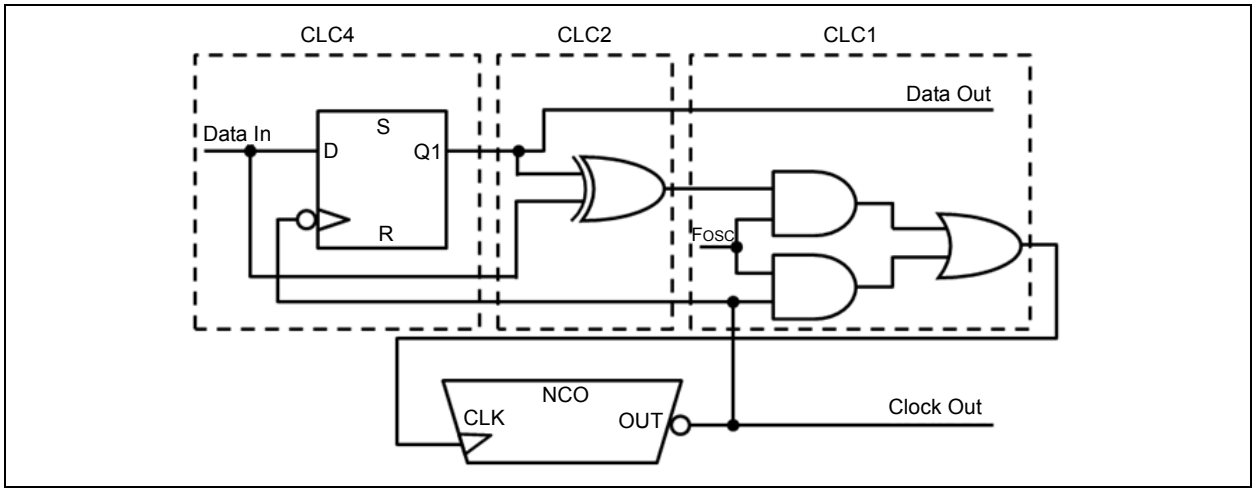
FIGURE 9: MANCHESTER DECODER



The timing diagram above (Figure 9) is decoded into the following block diagram (Figure 10). There are five stages in this diagram:

- Stage 1 – Incoming Manchester Signal
- Stage 2 – D flip-flop that captures input data when NCO is triggered
- Stage 3 – XOR gate to provide start time for NCO
- Stage 4 – AND-OR gate to supply clock to NCO, and to ensure that it clocks for full ¾ bit time
- Stage 5 – NCO to generate ¾ bit time, started in mid-bit transition of previous bit

FIGURE 10: FULL DECODER BLOCK DIAGRAM



PIC16F1509 IMPLEMENTATION

The device chosen for this implementation is PIC16F1509. It has four CLC blocks to implement combinational logic along with NCO to generate specific bit time. The following section covers the implementation of these blocks using the available resources in this device.

Stage 1 – D Flip-Flop (CLC4)

This stage latches in the Manchester data on the falling edge of the clock signal. This output is the recovered data that will be fed into the microcontroller. The data is sampled on the clock falling edge, and is stable to be read on the clock rising edge, because the data line never changes on a rising clock edge.

Stage 2 – XOR Gate (CLC2)

Because a transition is ensured in the middle of every bit in Manchester encoding, we can use an XOR gate to ensure that each mid-bit transition gives us a rising edge for Stage 3. This means that we are synchronizing our decoder in the middle of each bit.

Stage 3 – NCO + AND-OR (CLC1)

The PIC16F1509 has a NCO module that is used to generate ¾ bit-time to capture data value. The NCO is used in active-low Pulse Frequency mode to output a pulse when ¾ bit time expires. The pulse width can be controlled using a Special Function Register. The module also requires a clock source that allows it to repeatedly add a fixed value to an accumulator at the specified clock rate, which will be supplied by CLC1.

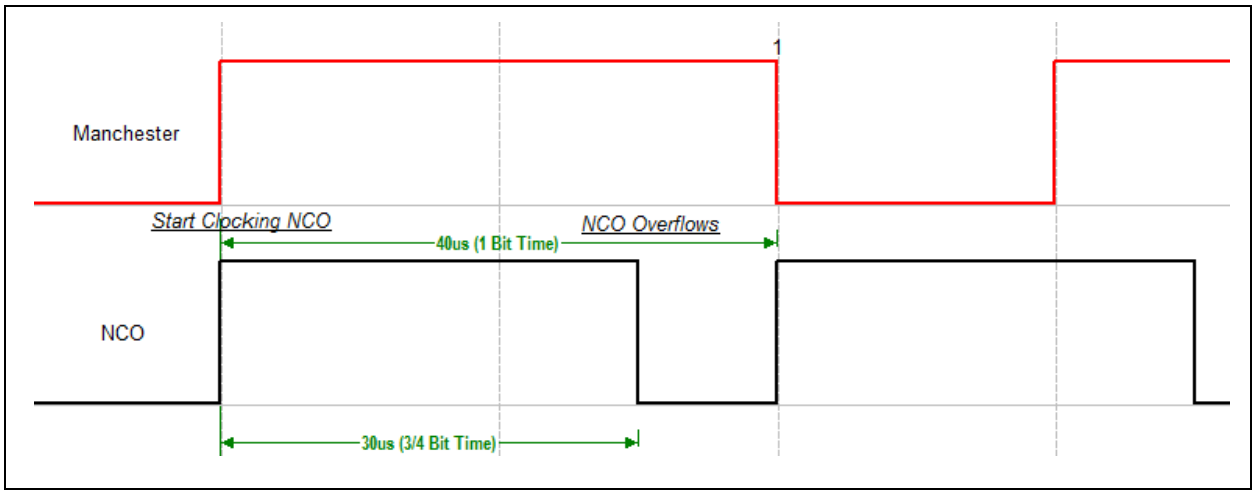
These two blocks together are the most important in the decoder. They create a fixed length pulse for each rising edge coming out of Stage 2. The output of the NCO is fed back into the AND-OR gate, so that when the output of Stage 2 goes to zero, the NCO will continue clocking until it overflows.

When the part is first configured, it will output a single ¾ bit length pulse. This is needed to put the NCO in its active-low state. When it is active, the NCO is waiting on the output pulse width clocks configured in the NCOCLK register.* Once a clock source is supplied, it will finish its active pulse and start counting again.

**Design Tip: By removing the clock source from the NCO and holding it in its active state, you have essentially created a way to control the duty cycle of the NCO.*

Figure 11 uses the example of a 25 kHz Manchester data input. 25 kHz gives us 40 µs bit time, which means that we need to generate a ¾ bit time of 30 µs to capture data and synchronize the NCO clock to the rising edge of the extracted clock.

FIGURE 11: BIT TIMING



To configure the NCO, refer to Equation 25-1 in the PIC16F1509 data sheet on the Microchip web site:

EQUATION 1:

$$F_{overflow} = \frac{NCO\ Clock\ Frequency * Increment\ Value}{2^n} = \frac{16\ MHz(Internal\ Clock\ F_{osc}) * Increment\ Value}{2^{20}}$$

n = accumulator width in bits

$$30us\ pulse = 33.33\ kHz = \frac{16\ MHz * Increment\ Value}{2^{20}} \Rightarrow Increment\ Value = 2184 = 0x0888$$

We are using the NCO in Pulse Frequency mode, where every time the accumulator overflows; the output becomes active for pre-defined clock periods. Keep in mind that these clocks are removed from the NCO to hold it in its active (low) state. They will then be added to the next pulse.

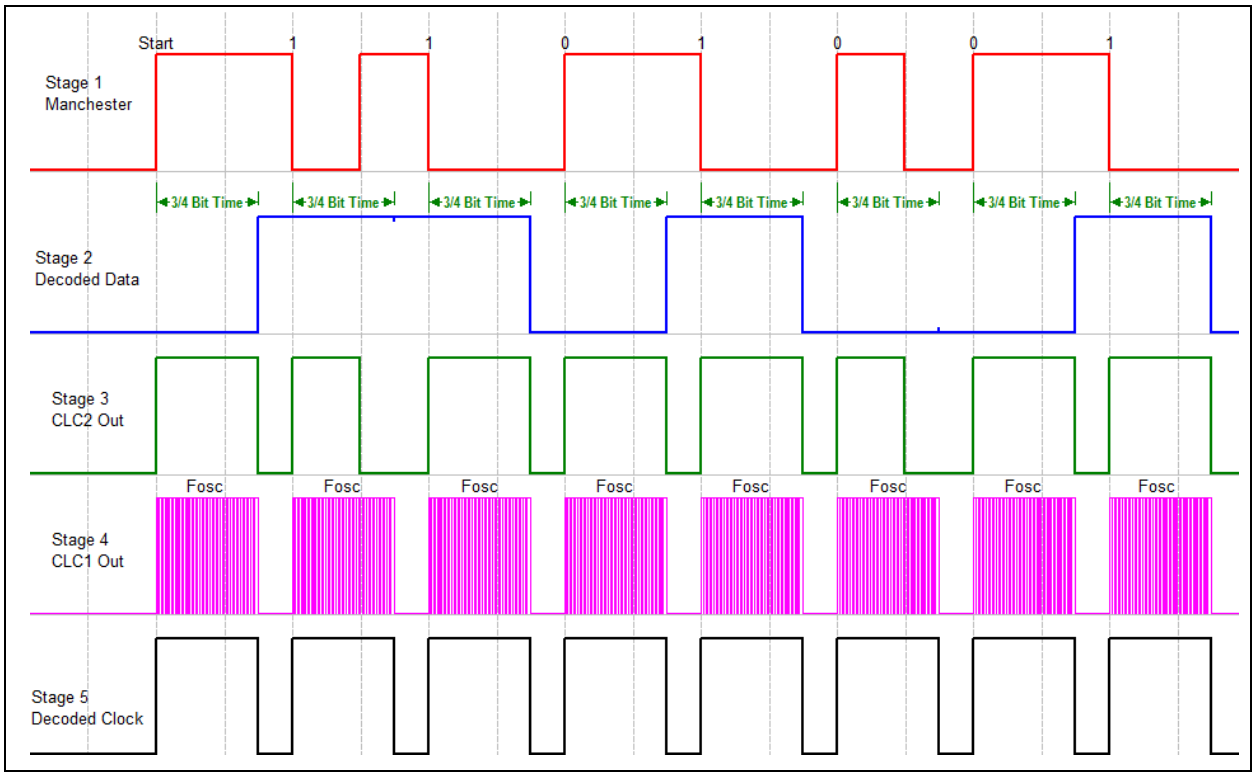
SYNCHRONIZATION

The assumption in the above analysis is that the first edge was a mid-bit transition. The problem is that one ¾ bit length after the first mid-bit transition; you have already missed your first bit of data. There are several methods to overcome this problem.

The first and easiest method is by receiving data with a known first bit. That way you can just mask it in after the data is read.

Another method is by first sending a Start bit. It needs to occur a ½ bit length before the first bit is transmitted, so the remaining data will synchronize with the mid-bit transitions. A Stop bit may be necessary to return the encoded data line back to its default state. Figure 12 again shows the waveform timings of the different blocks in the decoder. Because there is a Start and Stop bit, the first clock and last clock do not contain data and must be filtered out in the software. This can be done using the interrupt-on-change feature (trigger on the Start bit), then fed into the SPI or UART. Or, it can easily be bit-banged.

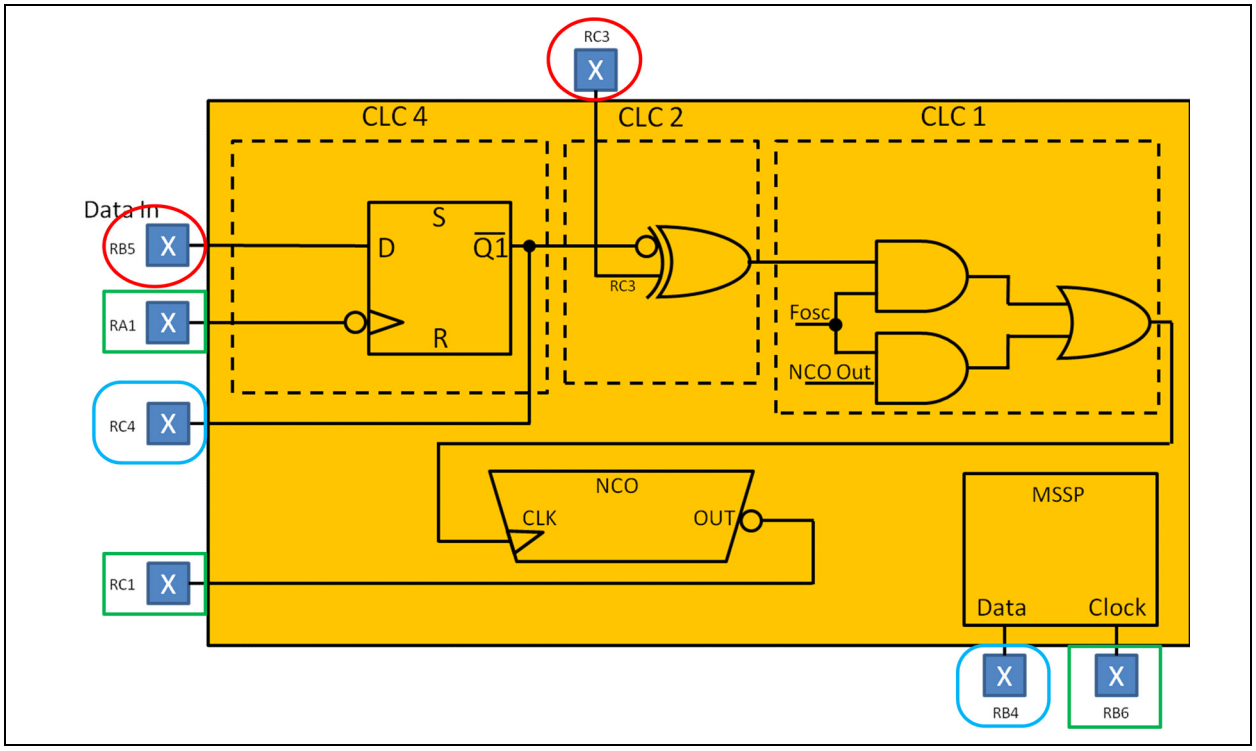
FIGURE 12: MANCHESTER DECODER FINAL TIMING



HARDWARE APPLICATION

The CLC blocks have a variety of inputs and outputs. Figure 13 shows how the three blocks can be wired up to each other externally in order to make the decoder work properly.

FIGURE 13: BLOCK DIAGRAM WITH EXTERNAL PIN CONNECTIONS



CONCLUSION

A Manchester decoder is implemented using Microchip's award winning CLC blocks. In the chosen implementation, the NCO and three CLC blocks were used. Serial data and clock can be fed into an SPI module, UART, or bit-banged to recover data if needed. The implementation chosen is using very few CPU cycles for Manchester decoding, leaving it to process other application tasks. The part can remain in Sleep mode between bytes to save power.

There are plenty of other applications where CLC blocks can be used very efficiently. Manchester encoding and decoding is just one of them. The new enhanced mid-range 8-bit core on PIC16F1509 features Microchip's Extreme Low-Power XLP technology, and is suitable for a wide range of applications.

REFERENCES

Wikipedia: http://en.wikipedia.org/wiki/Manchester_code

Device Data Sheet: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en553474

APPENDIX A

FIGURE 14: CLC 1 (AND-OR)

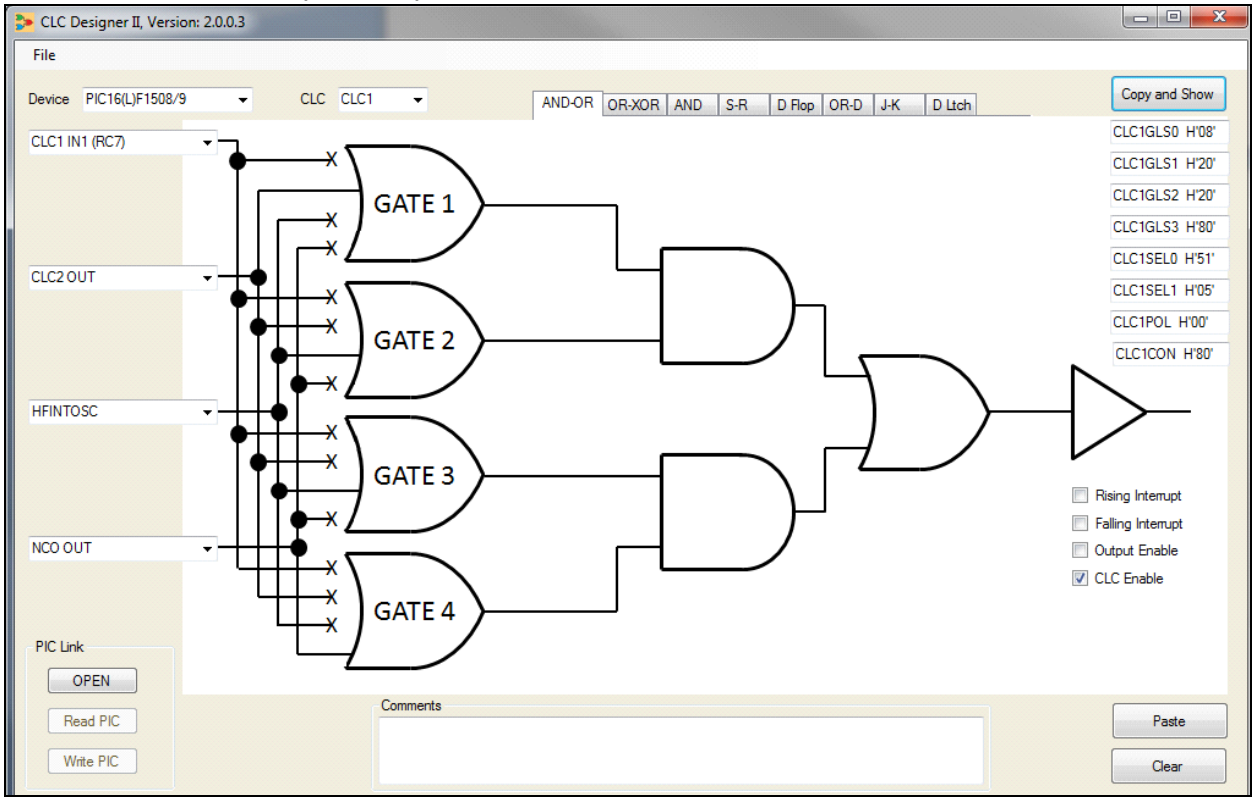


FIGURE 15: CLC 2 (D FLIP-FLOP)

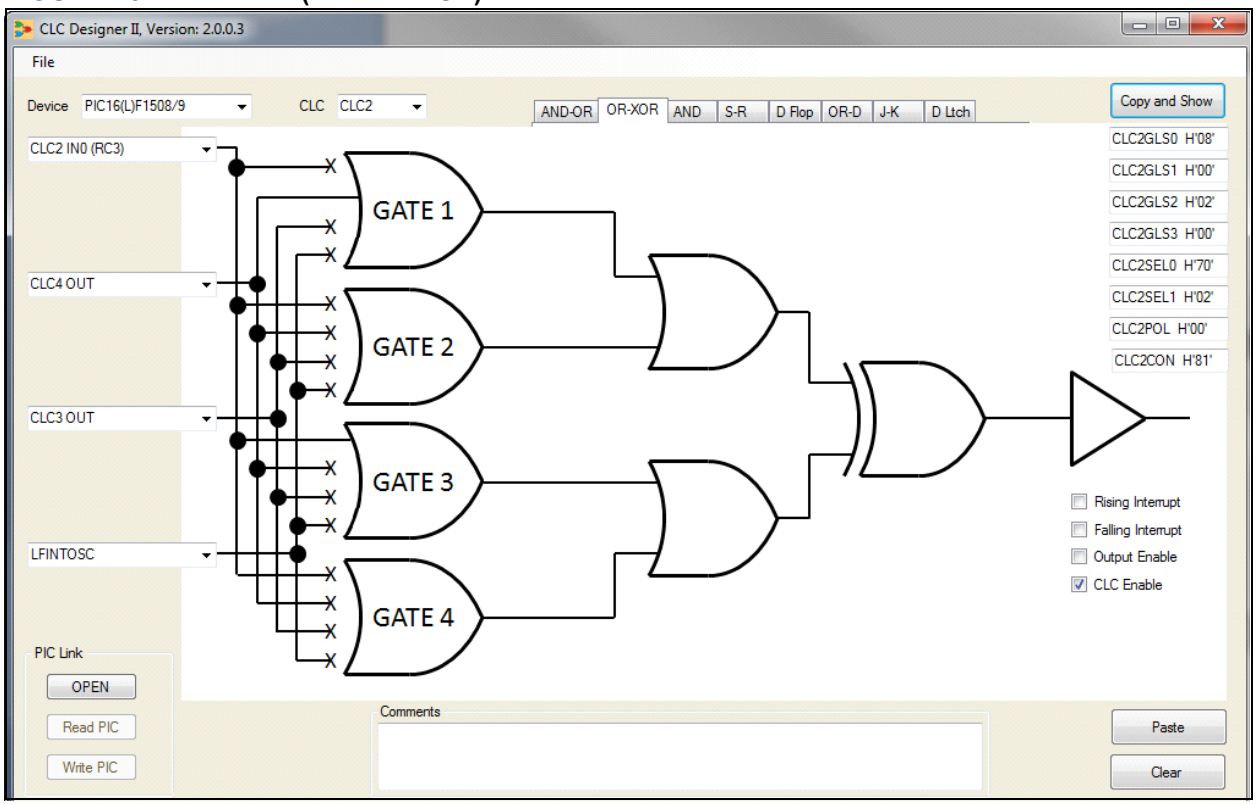


FIGURE 16: CLC4 (D FLIP-FLOP)

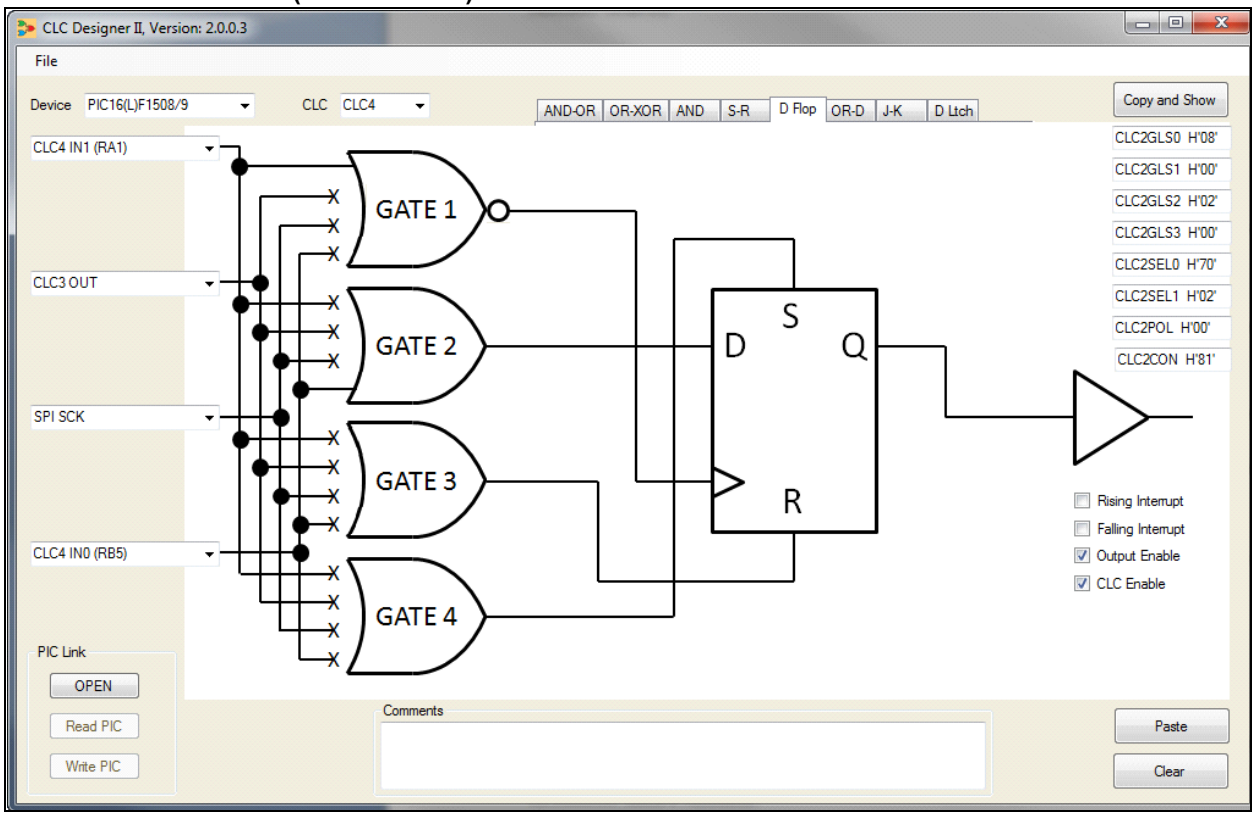
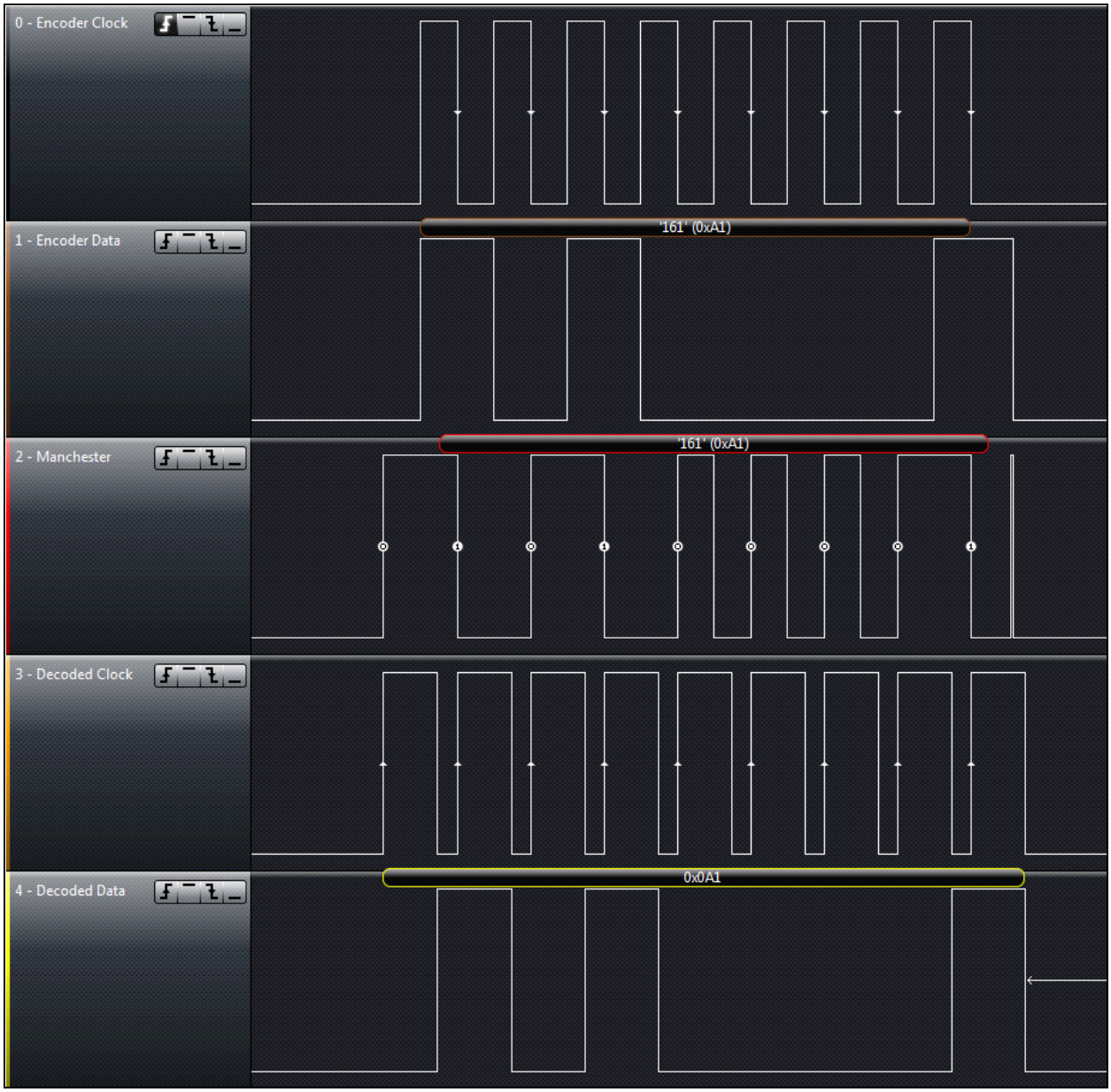


FIGURE 17: DECODED DATA



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Fax: 91-80-3090-4123

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India - Pune
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Japan - Osaka
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Japan - Yokohama
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Korea - Daegu
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Fax: 82-53-744-4302

Korea - Seoul
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Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
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Fax: 60-3-6201-9859

Malaysia - Penang
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Philippines - Manila
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Taiwan - Hsin Chu
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