

## Glitch-Free Design Using the Configurable Logic Cell (CLC)

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### INTRODUCTION

One of the challenges that digital designers run into frequently involves getting rid of glitches in their design. This is typically accounted for by ensuring there is adequate set-up and hold time when data is latched.

A 'glitch' is a signal which does not remain active for a full clock period. If a signal with a glitch feeds the clock line of numerous latches, some of the latches may get updated, while others may not. This is clearly a situation that designers want to avoid.

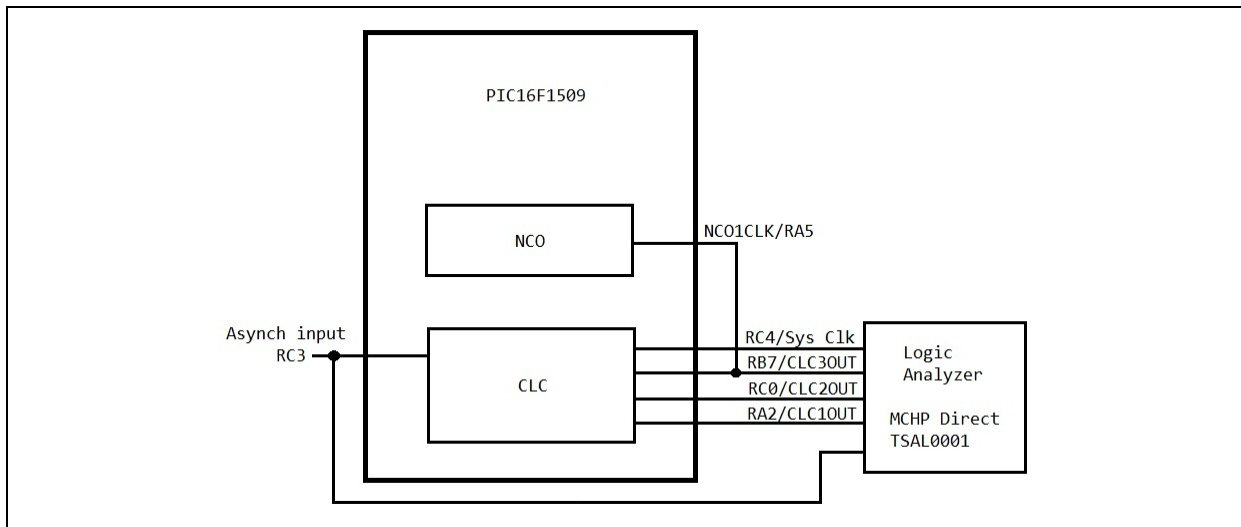
It should also be noted that propagation delay varies with temperature, therefore, a design which does not produce glitches during development may produce glitches under different conditions.

The addition of the Configurable Logic Cell (CLC) to the Microchip set of peripherals allows end-users to essentially "design" a simple peripheral that can interface with the PIC® microcontroller. With the ability to drive signals into the PIC device that can cause interrupts and increment counters, it is necessary to provide some instruction so that stable designs can be created using the CLC peripheral.

A PIC16F1509 was used for this example, and it uses three of the four available CLC modules. The 4th CLC module is being used to route the internal Fosc signal to the RC4 pin, so that it can be viewed with a logic analyzer. Other signals internal to the CLC (XOR output, latch output) have been brought out on external pins to provide greater visibility of how the application is functioning.

The block diagram (Figure 1) shows the asynchronous input signal on RC3, with the CLC outputs feeding the logic analyzer. The CLC3 signal is our glitch-free clock signal and is being fed into the NCO1CLK pad.

**FIGURE 1: GLITCH-FREE BLOCK DIAGRAM – BENCH SET-UP**



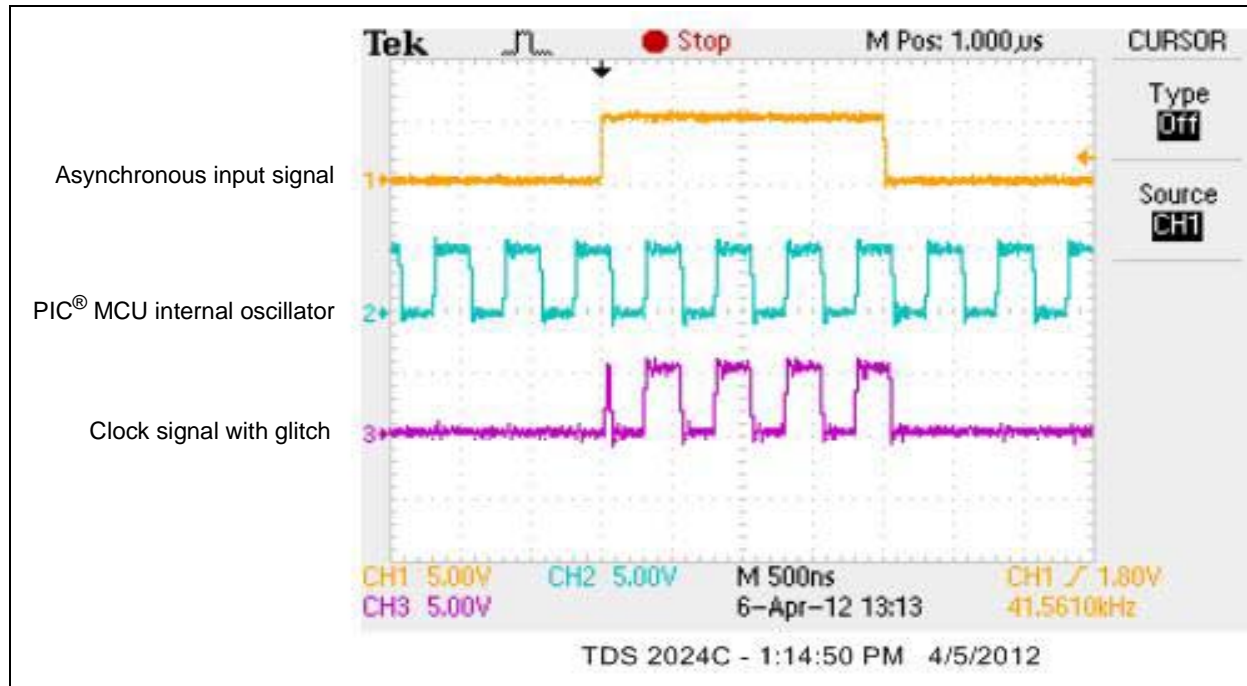
In this example, we will create a high-speed counter which is used to increment the NCO register. The NCO will increment as long as an external pulse signal is high. This creates a high-resolution, long-duration counter, as the NCO counter is a 20-bit wide register. It will take approximately 16 instruction cycles (4  $\mu$ s with 16 MHz clock) for the data to be read and the counter to reset, so it is necessary to have at least 4  $\mu$ s of low time between pulses. A falling edge interrupt flag on CLC2 provides a signal that the pulse width measurement has

been completed. While the NCO register has been designed to be resistant to glitches on the clock input, it is still good design practice to have clean signals feeding into the NCO clock line.



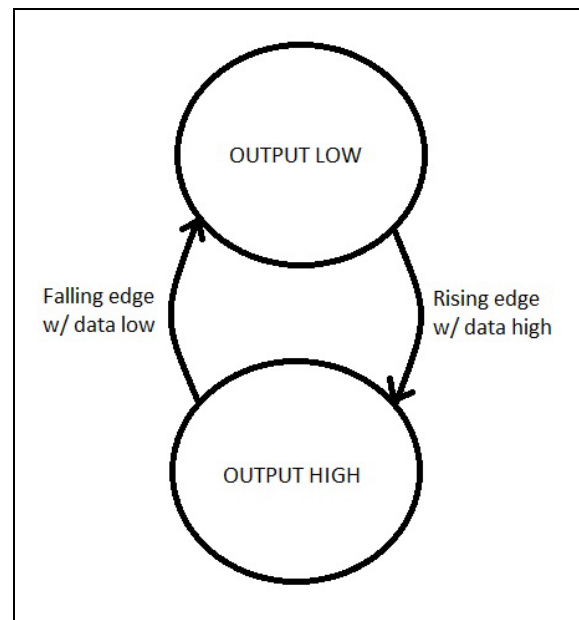
The first design for this circuit does allow glitches to pass in, and is a simple 'AND' of the pulse signal with the system clock. Note how a spike on the clock is created when the pulse signal rises shortly before the clock falls (Figure 2).

**FIGURE 2: LOGICAL 'AND' OF ASYNCHRONOUS PULSE AND SYSTEM CLOCK**



We want to use the 'AND' function to clock the NCO when the pulse is high, but we would like to get rid of the glitches on the clock signal. In order to do this, it would be ideal to create a pulse → new signal that would only rise on the rising edge of the clock, and only fall on the falling edge of the clock. This new signal (CLC2OUT) can be AND'ed with the oscillator clock, and there will never be a glitch on the NCO clock signal. A simple state diagram (Figure 3) shows how this will work.

**FIGURE 3: STATE DIAGRAM FOR CLEAN TRANSITION**

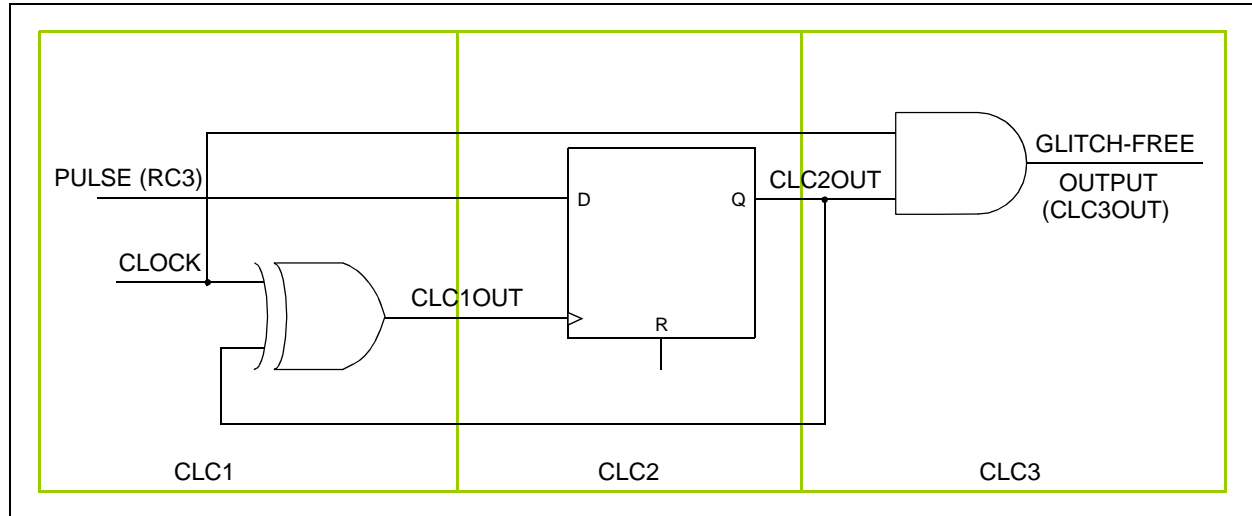




This state diagram can be implemented with a D flip-flop and an XOR gate. The XOR gate will have the function of taking feedback from the D flip-flop and inverting the clock, so that it will trigger on the falling edge once the

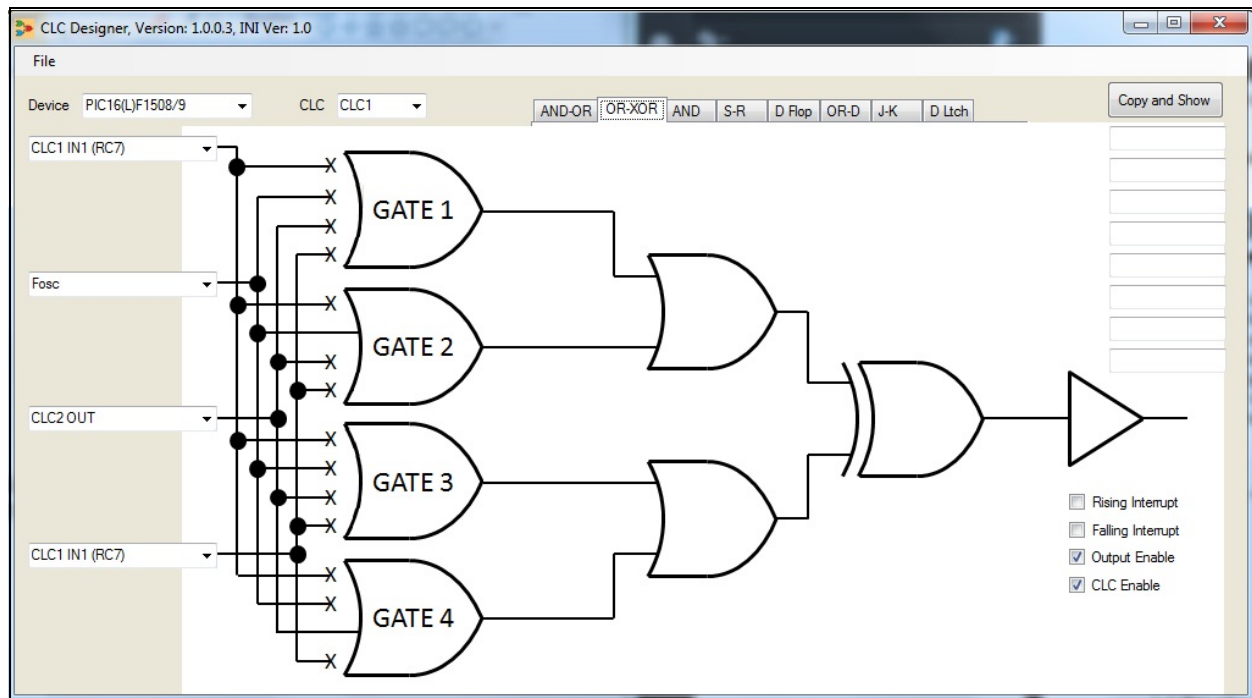
flip-flop has been set. A schematic for this is shown below (Figure 4). This new signal (CLC2OUT) can be AND'ed with the oscillator clock, and there will never be a glitch on the NCO clock signal.

**FIGURE 4: CREATING GLITCH-FREE CLOCK SIGNAL**



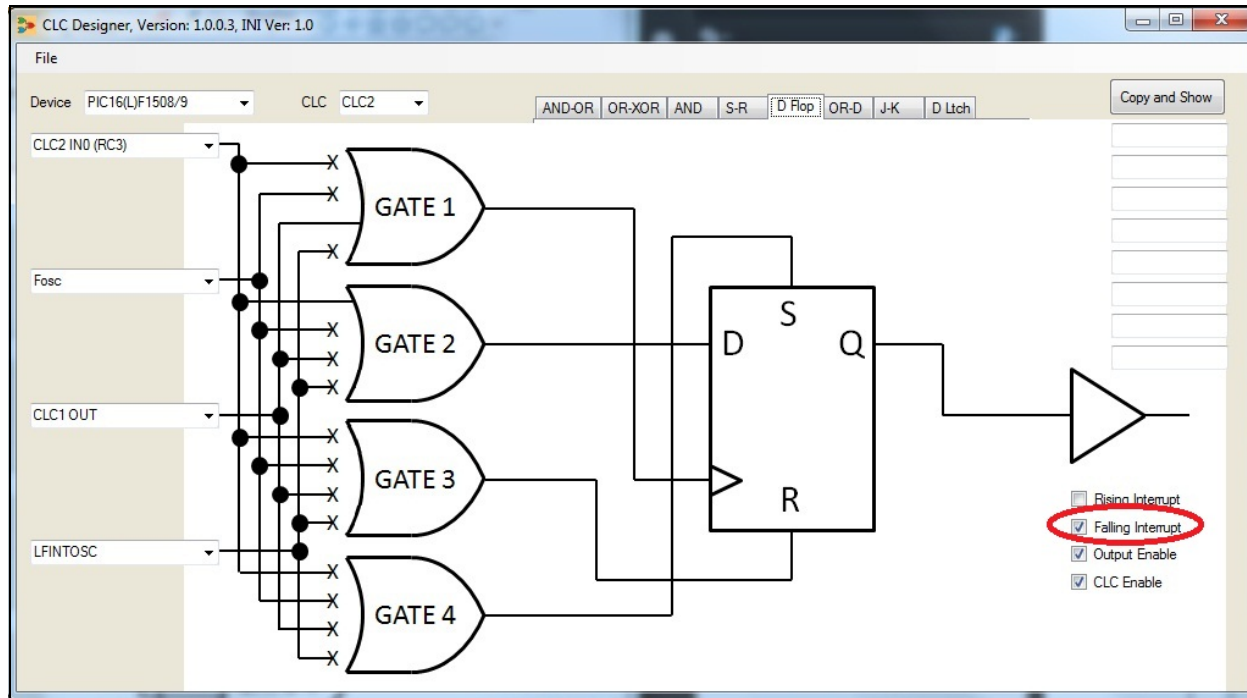
The schematic has been broken down so that each logic function will use one CLC module, and the following screenshots show how the schematic is implemented using the CLC tool → CLC Designer tool (Figure 5, Figure 6, Figure 7 and Figure 8):

**FIGURE 5: CLC1 OUTPUT OF D FLIP-FLOP XOR'ED WITH Fosc**

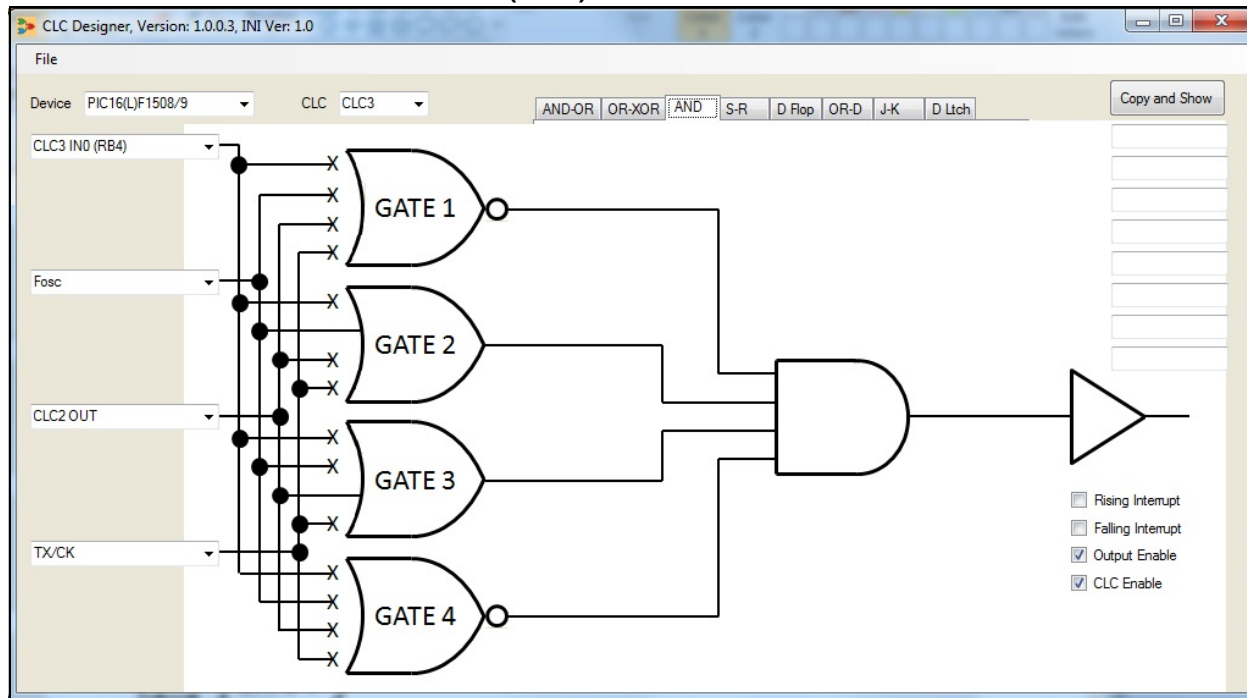




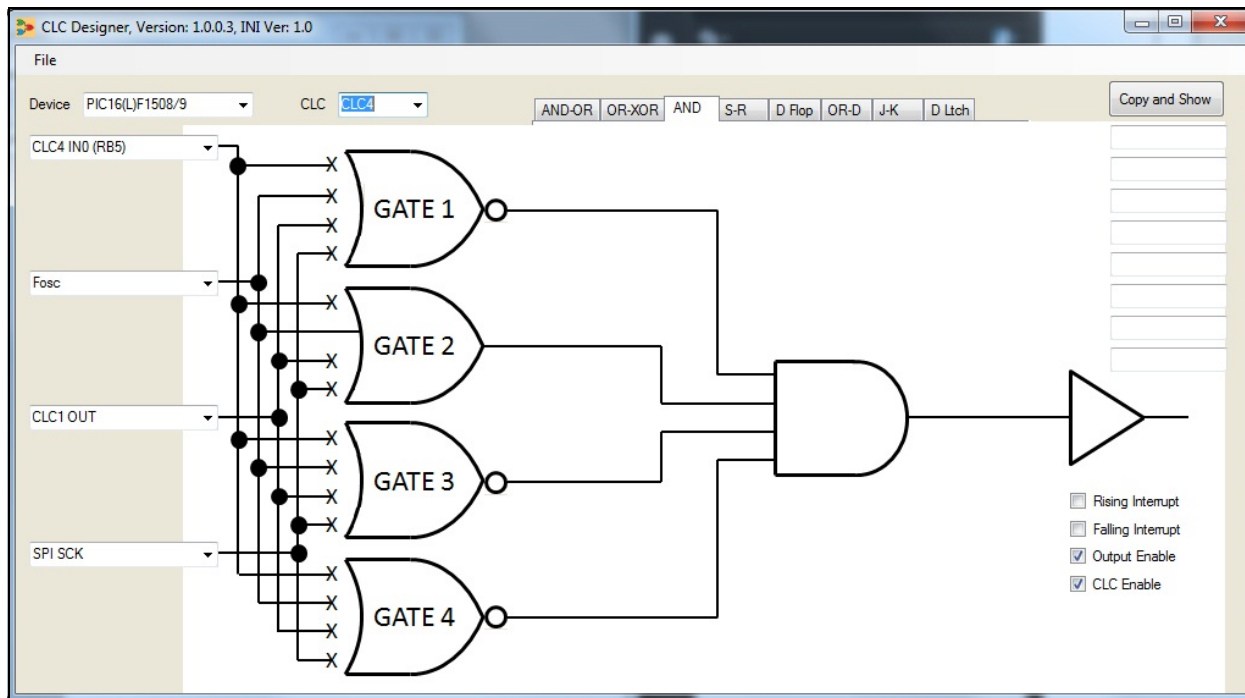
**FIGURE 6: CLC2 D FLIP-FLOP CLOCKED WITH XOR OUTPUT AND RC3 AS PULSE INPUT**



**FIGURE 7: CLC3 CLOCK SIGNAL (Fosc) AND'ED WITH D FLIP-FLOP OUTPUT**

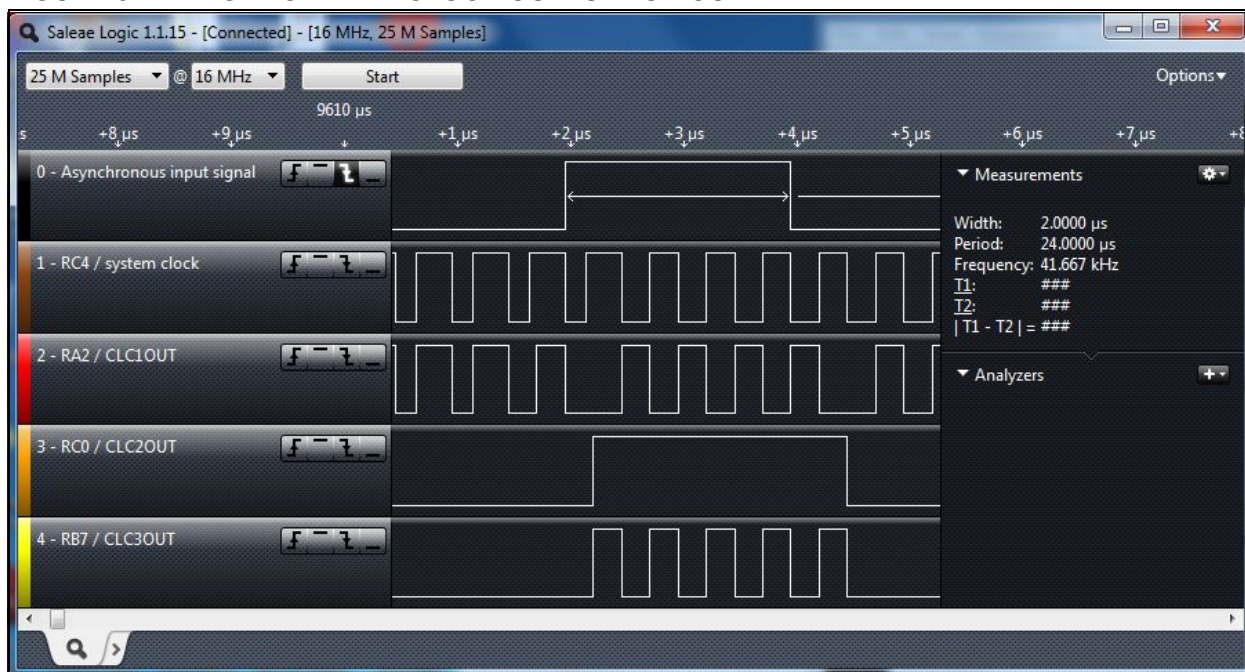




**FIGURE 8: Fosc ROUTED TO RC4 PIN**

Once this logic has been implemented, we now have a glitch-free output to drive our NCO clock signal. The scope plot below (Figure 9) shows the Asynchronous input signal, Fosc system clock, XOR output

(CLC1OUT), latch output (CLC2OUT), and glitch-free output clock (CLC3OUT). The interrupt flag will be set on the falling edge of the CLC2OUT signal (when we are done measuring our pulse width).

**FIGURE 9: GLITCH-FREE CLOCK OUTPUT TO NCO**



## APPENDIX A: ASSEMBLY SOURCE CODE

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FileName: glitch\_free.asm

Dependencies:

Processor: PIC16F1509

Hardware:

Compiler: MPASM 5.45 or later

Company: Microchip Technology, Inc.

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```
#include "p16f1509.inc"
```

```
__CONFIG _CONFIG1, _FOSC_INTOSC & _WDTE_OFF & _PWRTE_OFF & _CLKOUTEN_OFF  
__CONFIG _CONFIG2, _LVP_OFF & _STVREN_ON
```

```
errorlevel -302 ;suppress bank selection not zero warning
```

```
result0 equ 0x20  
result1 equ 0x21  
result2 equ 0x22
```

```
ORG 0x00
```

```
main
```

```
BANKSEL ANSELA  
clrf ANSELA ; all digital pins  
clrf ANSELC  
clrf ANSELB
```



```

BANKSEL    TRISB
bcf        TRISA,2          ; RA2 (pin 17) output - CLC1OUT
bcf        TRISC,0          ; RC0 (pin 16) output - CLC2OUT
bcf        TRISB,7          ; RB7 (pin 10) output - CLC3OUT
bcf        TRISC,4          ; RC4 (pin 6) output - CLC4OUT (used to show internal
                           oscillator clock)

BANKSEL    OSCCON
movlw 0x78
movwf OSCCON                ; go to 16 MHz clock

;; include file generated by CLC Designer Tool
#include "glitch_free_osc_out_clc2_int.inc"

BANKSEL    NCO1INCL        ; bank with NCO registers

movlw 0x00
movwf NCO1INCH
movlw 0x01
movwf NCO1INCL              ; set up increment value for NCO1INCH/L

movlw 0x03
movwf NCO1CLK               ; set up NCO1CLK pad as the clock source
movlw 0xC0
movwf NCO1CON               ; and run the NCO.

wait_initialize
BANKSEL    NCO1ACCL        ; bank with NCO registers
movlw 0x00
movwf NCO1ACCL
movwf NCO1ACCH
movwf NCO1ACCU              ; clear accumulator
bsf        NCO1CON,N1EN    ; turn on NCO

BANKSEL    PIR3
bcf        PIR3,CLC2IF      ; clear interrupt flag.

wait_for_pulse
btfss     PIR3,CLC2IF        ; Has CLC2IF falling edge interrupt flag been set?
goto      wait_for_pulse

                           ; Yes - I am done measuring the pulse width.
BANKSEL    NCO1ACCL        ; bank with NCO registers
bcf        NCO1CON,N1EN    ; turn off NCO

movf      NCO1ACCU,W
movwf     result2
movf      NCO1ACCH,W
movwf     result1
movf      NCO1ACCL,W
movwf     result0           ; pulse width measurement is stored in resultx.

goto      wait_initialize; so that we can do it again.

end

```



## APPENDIX B: CLC CONFIGURATION – ASSEMBLY LANGUAGE VERSION

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### CLC Configuration include files

#### CLC1 Configuration

```
BANKSEL CLC1GLS0
movlw   H'00'
movwf   CLC1GLS0
movlw   H'08'
movwf   CLC1GLS1
movlw   H'00'
movwf   CLC1GLS2
movlw   H'20'
movwf   CLC1GLS3
movlw   H'01'
movwf   CLC1SEL0
movlw   H'51'
movwf   CLC1SEL1
movlw   H'00'
movwf   CLC1POL
movlw   H'C1'
movwf   CLC1CON
```

#### CLC2 Configuration

```
BANKSEL CLC2GLS0
movlw   H'20'
movwf   CLC2GLS0
movlw   H'02'
movwf   CLC2GLS1
movlw   H'00'
movwf   CLC2GLS2
movlw   H'00'
movwf   CLC2GLS3
movlw   H'00'
movwf   CLC2SEL0
movlw   H'00'
movwf   CLC2SEL1
movlw   H'00'
movwf   CLC2POL
movlw   H'CC'
movwf   CLC2CON
```



## CLC3 Configuration

```
BANKSEL  CLC3GLS0
movlw    H'00'
movwf    CLC3GLS0
movlw    H'08'
movwf    CLC3GLS1
movlw    H'20'
movwf    CLC3GLS2
movlw    H'00'
movwf    CLC3GLS3
movlw    H'00'
movwf    CLC3SEL0
movlw    H'01'
movwf    CLC3SEL1
movlw    H'09'
movwf    CLC3POL
movlw    H'C2'
movwf    CLC3CON
```

## CLC4 Configuration

```
BANKSEL  CLC4GLS0
movlw    H'00'
movwf    CLC4GLS0
movlw    H'08'
movwf    CLC4GLS1
movlw    H'00'
movwf    CLC4GLS2
movlw    H'00'
movwf    CLC4GLS3
movlw    H'00'
movwf    CLC4SEL0
movlw    H'00'
movwf    CLC4SEL1
movlw    H'0D'
movwf    CLC4POL
movlw    H'C2'
movwf    CLC4CON
```



# AN1451

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NOTES:



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