AN1444

Grid-Connected Solar Microinverter Reference Design

Author: *Alex Dumais and Sabarish Kalyanaraman*
Microchip Technology Inc.

INTRODUCTION

Renewable resources, such as wind generation systems and Photovoltaic (PV) systems, have gained great visibility during the past few years as convenient and promising, renewable energy sources. There are several benefits for solar power systems, such as:

- Clean and renewable energy that replaces power produced by coal, oil and nuclear power
- Reduction/elimination of electric bills
- Silicon for manufacturing PV panels is the second most abundant element on Earth
- The ability to provide power to remote locations

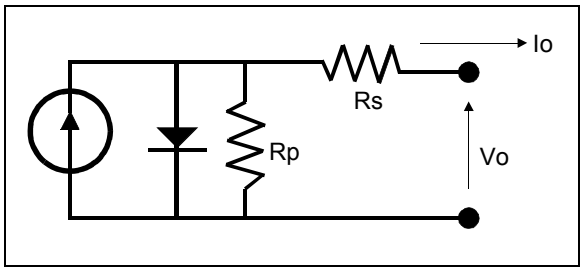
The recent increase in demand for solar power systems is due to enhancements in manufacturing crystalline panels, which reduces overall costs in manufacturing and increases the efficiency of the PV panels. Additional reasons for the demand in solar power are: PV technology is proven and reliable, PV modules have warranties exceeding 30 years and government incentives.

There are two main requirements for solar inverter systems: harvest available energy from the PV panel and inject a sinusoidal current into the grid in phase with the grid voltage. In order to harvest the energy out of the PV panel, a Maximum Power Point Tracking (MPPT) algorithm is required. This algorithm determines the maximum amount of power available from the PV module at any given time. Interfacing to the grid requires solar inverter systems to abide by certain standards given by utility companies. These standards, such as EN61000-3-2, IEEE1547 and the U.S. National Electrical Code (NEC) 690, deal with power quality, safety, grounding and detection of islanding conditions.

Characteristics of Solar Cells

To begin development of a solar microinverter system, it is important to understand the different characteristics of a solar cell. PV cells are semiconductor devices with electrical characteristics similar to that of a diode. However, a PV cell is a source of electricity and operates as a current source when light energy, such as sunlight, makes contact with it. The most common technologies today are the monocrystalline and multi-crystalline silicon modules. A PV cell can be modeled as shown in Figure 1. Rp and Rs are parasitic resistances that, in an ideal world, would be infinite and zero, respectively.

FIGURE 1: SIMPLIFIED MODEL OF A PV CELL

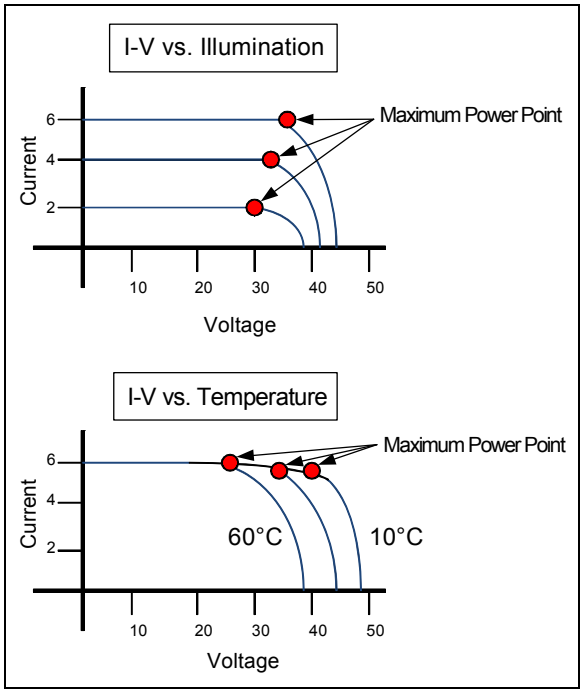


A PV cell will behave differently, depending on its size or type of load connected to it, and the intensity of sunlight (illumination). The characteristics of a PV cell are described by the different operating currents and voltages under different environments.

When the cell is exposed to sunlight, but is not connected to a load, there is no current flowing through the cell and the voltage across the PV cell reaches its maximum. This is known as the Open Circuit Voltage (V_{OC}). When the cell is loaded, current begins to flow through the circuit and the voltage across the cell begins to drop. The maximum current to pass through the cell can be determined when the two terminals are directly connected to each other and the voltage is zero. This is known as Short-Circuit Current (I_{SC}).

Light intensity and temperature largely impact the operating characteristics of a PV cell. Current is directly proportional to light intensity, but the change in illumination has little impact on the operating voltage. The operating voltage is, however, impacted by temperature. An increase in cell temperature will decrease the operating voltage, but will have little effect on the generated current. The influence of temperature and illumination on a PV module is illustrated in Figure 2.

FIGURE 2: PV MODULE ELECTRICAL CHARACTERISTICS



Changes in light intensity will have greater effect on the cell output power than changes in temperature. This is true for all commonly used PV materials. The important result of these two effects is that the power of a PV cell decreases when light intensity decreases and/or temperature increases.

Maximum Power Point (MPP)

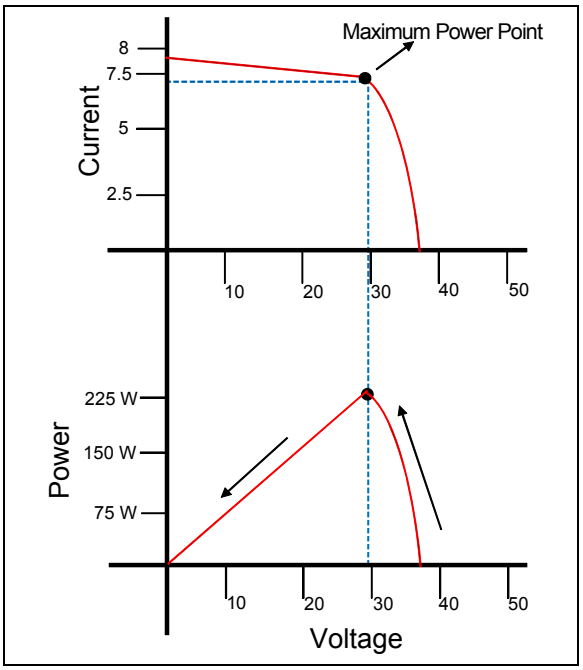
A solar cell may operate over a wide range of voltages and currents. By continuously increasing the resistive load on an irradiated cell from zero (short-circuit event) to a very high value (open circuit event), the MPP can be determined. MPP is the operating point that maximizes, $V \times I$, and delivers the maximum power at that irradiation. The output power in a short-circuit (PV voltage equals zero) or open circuit (PV current equals zero) event is zero.

A high quality, monocrystalline silicon solar cell, at 25°C cell temperature, may produce 0.60 volts open circuit. The temperature on a given cell in full sunlight, with an air temperature of 25°C, may be closer to 45°C which will reduce the open circuit voltage to ~0.55V. As temperature rises, the open circuit voltage continues to drop until there is a short circuit on the PV module.

The maximum power at a cell temperature of 45°C is typically produced with 80% of the open circuit voltage and 90% of the short-circuit current. The short-circuit current from a cell is nearly proportional to the illumination, while the open circuit voltage may drop 10% with an 80% drop in illumination. Lower quality cells have a more rapid drop in voltage with increasing current, which would reduce the usable power output from 70% to 50% or even as little as 25%.

Figure 3 shows the output current and output power of a PV panel as a function of operating voltage for a given illumination.

FIGURE 3: MPPT CHARACTERISTICS OF A PV MODULE



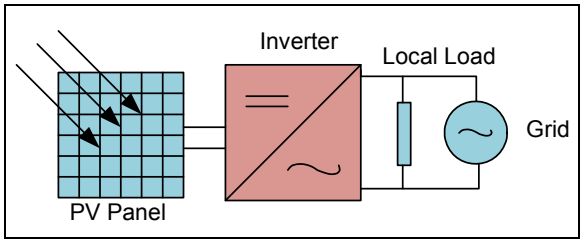
The solar microinverter must ensure that the PV module is operating at the MPP to capture the maximum energy from the PV module, at any given time. This is accomplished by the Maximum Power Point control loop, known as the Maximum Power Point Tracker (MPPT). Achieving a high percentage of MPP tracking also requires the PV output voltage ripple to be sufficiently small, in order to operate around the Maximum Power Point without too much variation in PV current. See the **"Decoupling Capacitors"** section for more details on limitation of the PV module output voltage ripple. Refer to the **"Maximum Power Point (MPP)"** section for more details on implementing MPPT.

A common MPP voltage range for PV modules can be defined in the range of 25V to 45V, at a power generation of approximate 250W, with an open circuit voltage below 50V.

Introduction of a Grid-Connected Microinverter System

A high-level block diagram of a grid-connected solar microinverter system is shown in Figure 4.

FIGURE 4: GRID-CONNECTED SOLAR MICROINVERTER SYSTEM



The term, “microinverter”, refers to a solar PV system comprised of a single low-power inverter module for each PV panel. These systems are becoming more and more popular as they reduce overall installation costs, improve safety and better maximize the solar energy harvest. Other advantages of a solar microinverter system include:

- Improvement of system reliability by reducing inverter temperatures and removing fans
- Replacement of traditional hard switching techniques with soft switching techniques to improve efficiency and reduce heat dissipation
- System designs can be standardized (hardware and software) to improve reliability and reduce costs

This Application Note presents and discusses Microchip’s 215W Solar Microinverter Reference Design in detail.

HARDWARE DESIGN

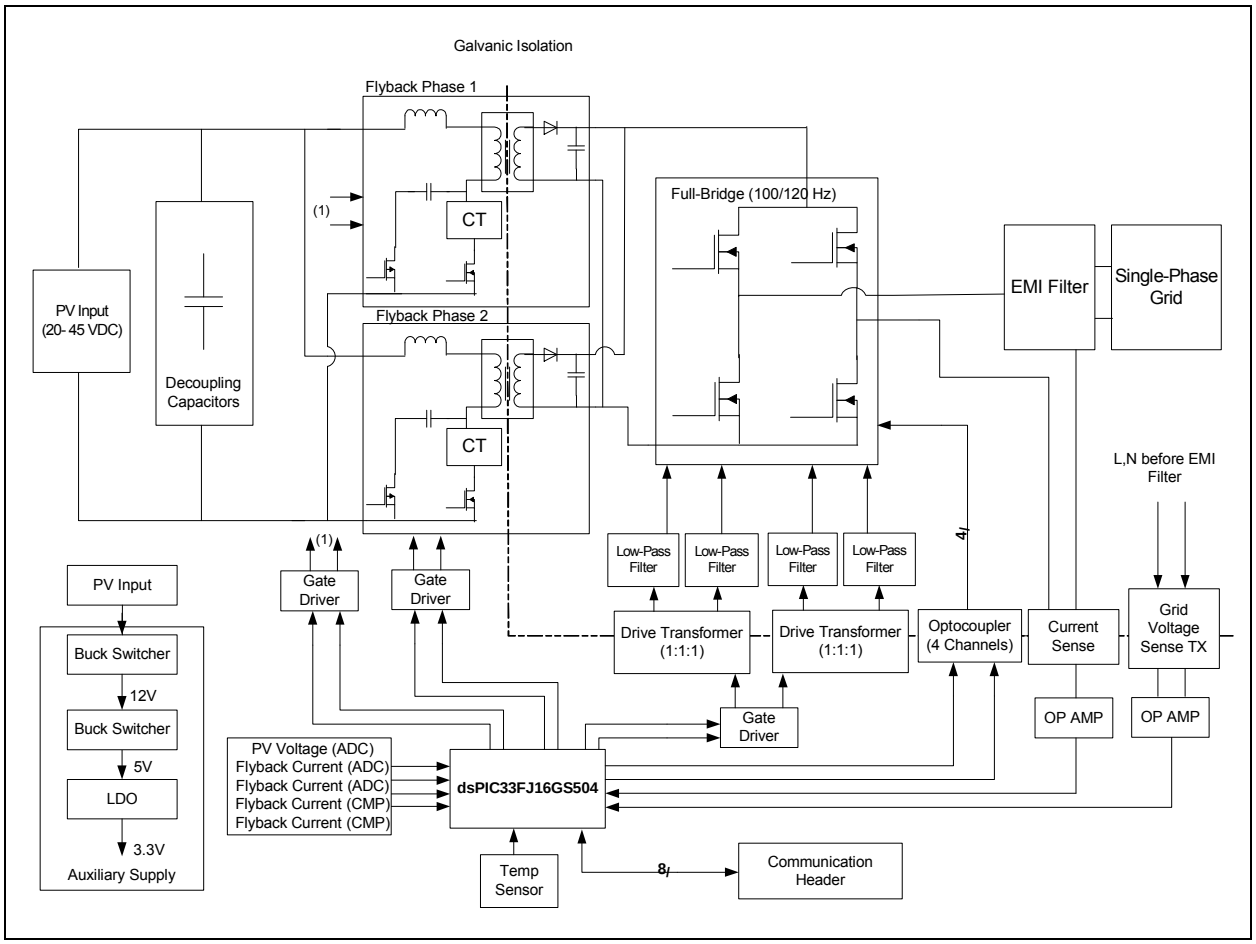
The Solar Microinverter Reference Design is a single stage, grid-connected, solar PV microinverter. This means that the DC power from the solar panel is converted directly to a rectified AC signal. This conversion is done by an interleaved flyback converter. A Full-Bridge (unfolding) converter, switched at 2x line frequency, controls the direction of power flow to the grid. This microinverter has been designed to connect to any PV module having a power rating of approximately 250 watts, with an input voltage range of 25 VDC to 45 VDC, and a maximum open circuit voltage of ~55V.

Features of the reference design include:

- Peak Efficiency: 94.8%
- Maximum Power Point Tracking: 99.5%
- Maximum Output Power: 215W
- Grid Voltage Range (230 VAC): 210 VAC-264 VAC
- Grid Voltage Range (120 VAC): 90 VAC-140 VAC
- Input Voltage Range: 25 VDC-45 VDC
- Input Voltage Extended Range: 20 VDC-25 VDC @ reduced output power
- Galvanic Isolation
- Support for Power Line/Wireless Communication (add-on)

A block diagram of the grid-connected Solar Microinverter Reference Design is shown in Figure 5.

FIGURE 5: HIGH-LEVEL SOLAR MICROINVERTER BLOCK DIAGRAM



Decoupling Capacitors

There are five decoupling capacitors at the input of the solar microinverter that serve as an energy storage element between the input and output. These capacitors balance the different instantaneous powers in the system. As the input power from the PV panel is to remain constant to maximize the energy harvested from the panel, there will be an instantaneous power mismatch between the input power and output power.

The solar microinverter generates a sinusoidal current that is in phase with the grid voltage. There is little phase shift ($\phi \sim 0$) between the grid voltage and current (PF near unity). Equation 1 shows the time varying output power.

EQUATION 1: TIME VARYING OUTPUT POWER

$$P_{out}(t) = V_{out}\,COS\,(\omega t) \bullet I_{out}\,COS\,(\omega t - \phi)$$

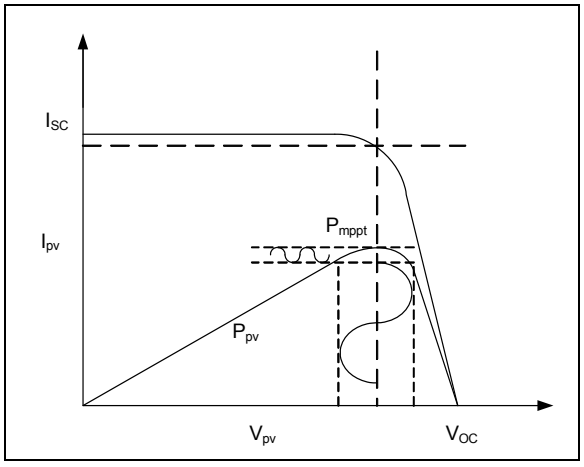
Equation 1 can be expressed as two components; average constant power and time varying power with 2x the line frequency, as shown in Equation 2.

EQUATION 2: TIME VARYING OUTPUT POWER

$$P_{out}(t) = \frac{1}{2}V_{out}I_{out} + \frac{1}{2}V_{out}I_{out}cos(2\omega t)$$

The decoupling capacitors are also required to reduce the ripple voltage from the PV panel in order to achieve a utilization factor greater than 99% (maximum power utilization). As shown in Figure 6, large PV panel ripple voltage means that the system operates further away from MPP.

FIGURE 6: VOLTAGE RIPPLE EFECT ON PV



Leveraging the work by S. B. Kjaer in *"Design and Control of an Inverter for Photovoltaic Applications"*, the ripple voltage can be determined by Equation 3, where α and β are coefficients of a second-order Taylor polynomial and Kpv is the utilization factor.

EQUATION 3: RIPPLE VOLTAGE

$$V_{ripple} = \sqrt{\frac{(k_{pv} - 1) \cdot 2 \cdot P_{MPP}}{3 \cdot \alpha \cdot V_{MPP} + \beta}}$$

With a known ripple voltage, the required capacitance can be determined to meet the ripple specifications as shown in Equation 4.

EQUATION 4: REQUIRED CAPACITANCE

$$C_{bulk} = \frac{P_{MPP}}{2\pi \cdot f_{ripple} \cdot V_{mpp} \cdot V_{ripple}}$$

The ripple frequency is twice the line frequency as the output of the flyback is a rectified sine wave and V_{MPP} and P_{MPP} have been taken as worst case. Different PV modules need to be considered to determine the required bulk capacitance. Additionally, the wide tolerance of electrolytic capacitors, which can be up to 20 percent, must be taken into account.

ELECTROLYTIC CAPACITOR LIFE MODEL

Manufacturers of solar panels offer warranties of 30 years, or more, on their solar panels. This impacts the design of any solar microinverter system because it should be just as reliable as the PV panel. The biggest limiting factor, and an area that needs to be addressed in more detail, is the life expectancy of the electrolytic bulk capacitors. For example, over time it is possible for the Equivalent Series Resistance (ESR) of electrolytic capacitors to increase significantly, causing the capacitor to overheat and possibly short out.

Several factors affect the life expectancy of electrolytic capacitors. These include DC operating voltage, ripple current and ambient temperature. Equation 5 determines the operating hours of electrolytic capacitors, where Lb is the base life given by the manufacture, ΔT is the difference between maximum rated temperature and working temperature, and Mv is the voltage multiplier.

EQUATION 5: OPERATING HOURS OF ELECTROLYTIC CAPACITORS

$$L_{hrs} = L_b \cdot M_v \cdot 2^{\frac{\Delta T}{10}}$$

For this reference design, five 2200 µF aluminum electrolytic capacitors from Nichicon were selected (UPW1J222MHD) for the input bulk capacitance. These capacitors have a rated voltage of 63 VDC and have a base life of 8000 hours at 105°C. The rated ripple current at 100 kHz is 3.2A. As the ripple current is at a frequency of 100/120 Hz, the rated ripple current is multiplied by a frequency coefficient of 0.85. The ripple current at 120 Hz is 2.72A. From Equation 5, the expected life calculates to ~30 years. This is actually on the low end as many factors were not considered, such as operating temperature which is assumed constant. Microinverters only operate during daylight hours and the equation doesn't account for reduced ripple current. Therefore, from calculations and usage considerations, it is possible for the electrolytic bulk capacitors to be just as reliable as the PV panels.

Interleaved Active Clamp Flyback Design

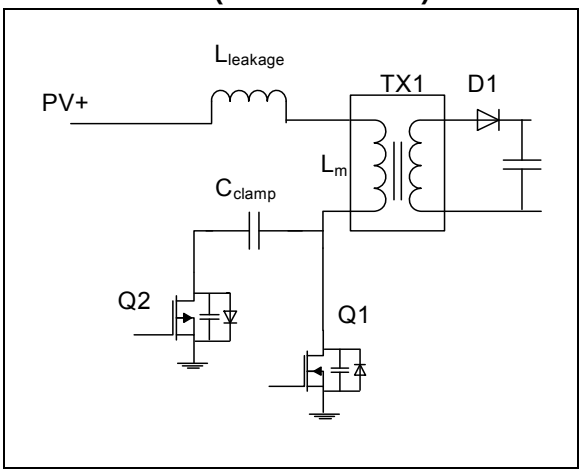
The flyback converter was selected as a single stage topology that can boost the low PV panel voltages (20-45 VDC) to a rectified AC output, as well as provide galvanic isolation from the PV panel and the grid. Flyback converters are generally used in low power, step-down applications, typically less than a couple hundred watts and that have a low output current. A forward converter can also step up the PV panel voltage and provide galvanic isolation. When comparing the two topologies, the flyback converter requires fewer components as there is no freewheeling diode on the output or the need for an output inductor; this is why the flyback topology was selected.

One of the biggest concerns about the flyback topology is how to handle the leakage energy. When the flyback MOSFET turns off, there is a large amount of energy still in the core that isn't transferred (linked) to the secondary side. This energy causes a large voltage spike on the flyback MOSFET, which can be very destructive for the MOSFET. Traditional Resistor, Capacitor, Diode (RCD) snubbers can be added across the transformer primary to dissipate this energy through heat. The RCD snubber will protect the flyback MOSFET, but will have a negative impact on system efficiency.

The solar microinverter incorporates an active clamp circuit that is essentially a lossless snubber. The leakage spike is clamped by the clamping capacitors (C_{clamp}), and then the leftover energy is stored in the clamping capacitors. This energy is then transferred to the secondary, recycling the energy. If correctly implemented, the active clamp circuit also provides Zero Voltage Switching (ZVS) on the flyback MOSFET, which reduces the switching losses and improves overall efficiency.

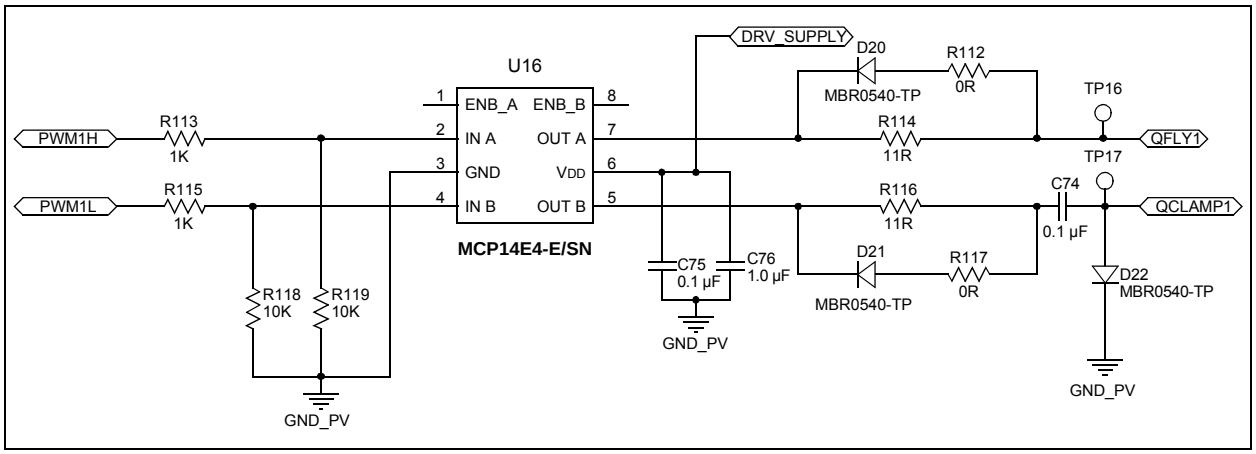
Figure 7 shows the simplified circuit of the single-phase active clamp flyback converter.

FIGURE 7: ACTIVE CLAMP FLYBACK CONVERTER (SINGLE PHASE)



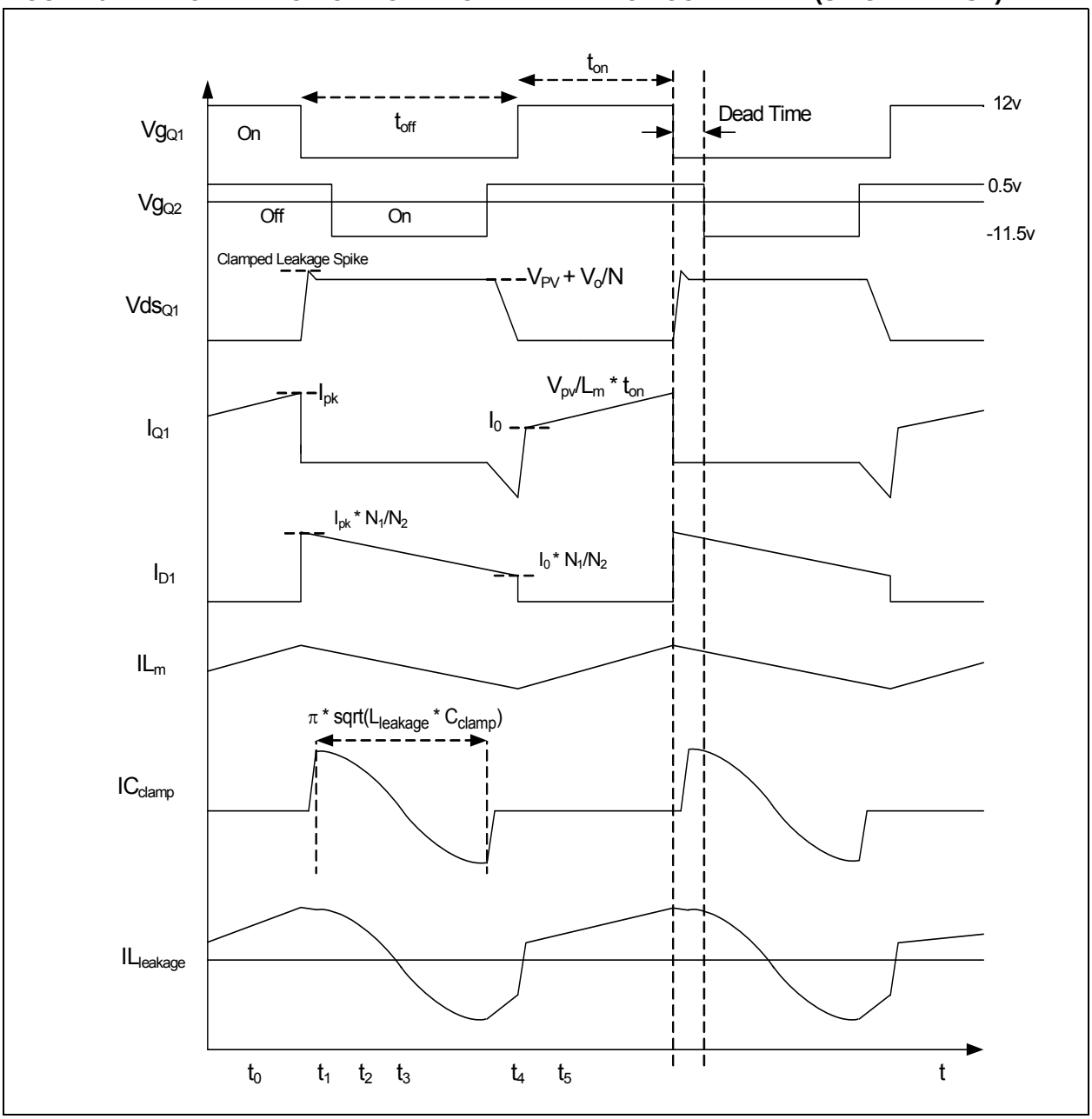
Here the leakage inductance is shown as a separate component, but this can be incorporated into the main transformer. A P-Channel MOSFET is selected to eliminate the need for a high-side gate drive circuit if the clamp MOSFET was across the transformer windings.

FIGURE 8: FLYBACK DRIVE CIRCUIT



One key item is the circuit for driving the P-Channel MOSFET. To drive the P-Channel MOSFET, a negative voltage between the gate and source is required. The output of the gate drive IC (MCP14E4) is a square wave with a given duty cycle (d) and an amplitude of 12V. A small ceramic capacitor is placed in series to remove the DC offset. At a duty cycle of 50%, the amplitude of the square wave would be +6V to -6V. A diode is added after the capacitor, with the anode connected to the capacitor, and the cathode connected to ground. This diode will clamp the positive voltage to ~0.7V and force the amplitude all negative. Figure 9 shows the gate drive waveforms for both MOSFETs.

FIGURE 9: OPERATION OF ACTIVE CLAMP FLYBACK CONVERTER (SINGLE PHASE)



The Solar Microinverter Reference Design implements an interleaved active clamp flyback converter. An interleaved topology shares the input/output current which results in lower copper and core losses. Also, the output diode conduction losses are reduced to help improve overall efficiency. There are also two other reasons to implement an interleaved design: reduction in the output current ripple which helps lower Total Harmonic Distortion (THD), and improve input bulk capacitor life span as the input current ripple is reduced.

When designing the flyback transformer, a design decision must be made as to whether the flyback converter operates in Discontinuous Mode (DCM) or Continuous Conduction Mode (CCM). The interleaved flyback converter operates in both DCM as well as CCM. At light loads, the flyback will operate in DCM, but at higher loads, the system will operate in CCM. In CCM, the primary/secondary peak currents will be two to three time less than DCM. Additional benefits to operating in CCM include:

- Smaller output filter capacitors with lower ripple ratings
- Reduced losses in the output diode
- Smaller transient output voltage spikes
- EMI performance will be better
- With silicon carbide diodes, the reverse recovery losses are minimized

Figure 9 demonstrates the operating waveforms of the active clamp flyback converter operating in Continuous Conduction mode. The following section breaks down the waveform into six different time intervals and discusses in detail how the system operates.

INTERVAL t_0

During interval, t_0, the flyback MOSFET (Q1) is conducting and the P-Channel clamping MOSFET is open. Diode, D1, is reversed biased as the voltage across the output of Transformer (TX1) is negative. During this time, the output capacitor delivers the required energy to the load. The inductor ripple current can be defined by Equation 6.

EQUATION 6: INDUCTOR RIPPLE CURRENT

$$I_L = \frac{V_{PV} \cdot \left(\frac{d}{f_{sw}}\right)}{L_M}$$

INTERVAL t_1 (DEAD TIME)

Interval, t_1, is defined as the instant from when MOSFET Q1 turns off, to when MOSFET Q2 starts conducting. This is referred to as dead time. This interval can be broken into two parts. The first part is the instant directly after MOSFET Q1 turns off to the clamping of the drain to the source voltage of MOSFET Q1.

When MOSFET Q1 transitions off, the current flowing in the circuit from the leakage inductance continues to flow in the same direction, which charges the Output Capacitance (Coss) of MOSFET Q1. This current will charge Coss to the PV module input voltage, plus the reflected rectified output voltage ($PVinput + Vout/N$, where N is the transformer turns ratio). During this time, the output diode (D1) becomes forward biased as the voltage across the transformer secondary becomes positive. The energy stored in the core is transferred to the secondary, which charges the output capacitor and provides energy to the load.

The second interval takes place after Coss has been charged and continues until the instant before turning on the P-Channel MOSFET (Q2). After Coss has been charged, the remaining energy in the leakage inductance will begin to flow through the clamping capacitors forward biasing the body diode of the P-Channel MOSFET. The clamping capacitors begin to store the leftover energy from the leakage inductor.

INTERVAL t_2

During this interval, the P-Channel MOSFET transitions on with ZVS, as the body diode was forward biased during interval, t1. The output diode is forward biased, providing energy to the output capacitor and load.

The leakage inductor and clamping capacitor begin to resonate with the energy transferring from the inductor to the clamping capacitor. Equation 7 determines the resonant frequency of the clamping network. The interval ends when the energy from the inductor depletes.

EQUATION 7: RESONANT FREQUENCY OF THE CLAMPING NETWORK

$$f_r = \frac{1}{2\pi \cdot \sqrt{L_{leakage} \cdot C_{clamp}}}$$

INTERVAL T_3

During this interval, the P-Channel MOSFET must be on so that the tank current can continue to resonate, but now the energy stored in the clamp capacitors is transferred back to the leakage inductor. During this interval, the output diode is still forward biased and the energy that is stored in the capacitor will be transferred to the secondary side, recycling the leakage energy.

INTERVAL t_4 (DEAD TIME)

Interval, t_4, is another dead-time state as MOSFET Q2 has transitioned off. MOSFET Q2 should transition off near the peak of the resonant period, forcing the maximum tank current to flow through the body diode of MOSFET Q1, quickly discharging the drain-to-source voltage. During this time, the output diode remains forward biased.

INTERVAL t_5

At instant, t_5, the flyback MOSFET Q1 transitions with Zero Voltage Switching. The output diode is reversed biased and the output capacitor supplies the load current.

For Zero Voltage Switching (ZVS) to occur, it is important that the energy in the inductor when the flyback MOSFET turns off (interval t_1) to be greater than the energy required to charge C_{oss} of MOSFET Q1, and that the body diode of MOSFET Q1 can be forward biased. The energy stored in the inductor and the energy required to charge C_{oss} can be calculated by Equation 8 and where I_{pk} can be calculated by Equation 9.

EQUATION 8: ENERGY REQUIRED TO CHARGE COSS

$$E_{inductor} = \frac{1}{2} I_{pk}2 \cdot L_{leakage}$$

$$E_{capacitor} = \frac{1}{2} V_{coss}2 \cdot C_{oss}$$

EQUATION 9: IPK

$$I_{pk} = \frac{\frac{P_{out}}{2\eta} \cdot \sqrt{2}}{V_{mpp} \cdot d} + \frac{I_{L\_ripple}}{2}$$

Transformer Design

The flyback transformer has been designed to meet the following specifications:

- Minimum Input Voltage: 19 VDC
- Maximum Output Voltage (230 VAC): 375V
- Maximum Output Power (V_{pv} > 25V): 215W
- Maximum Output Power (20 VDC > V_{pv} < 25 VDC): 185W
- Secondary Current (230 VAC) – 1.05 Arms
- Maximum Duty Cycle: 0.75
- Switching Frequency: 57 kHz
- Magnetizing Inductance: 55 µH
- Leakage Inductance: 1.3 µH
- Maximum Energy Stored in Core: 5.5 mJ
- Isolation: 3 kVA

With the specification provided, the required turns ratio of the transformer can be determined by Equation 10.

EQUATION 10: TRANSFORMER TURNS RATIO

$$N = \frac{V_{out}}{V_{pv}} \cdot \left(\frac{1 - D}{D}\right)$$

To leave some margin, a turns ratio of seven was selected for the 230 VAC systems. The duty cycle can be pushed relatively high because the active clamp circuit will remove the energy from the core during the OFF time. There is, however, a limit as to how high the duty cycle can be since there must be sufficient time for the resonance to occur between the active clamp capacitors and the leakage inductance.

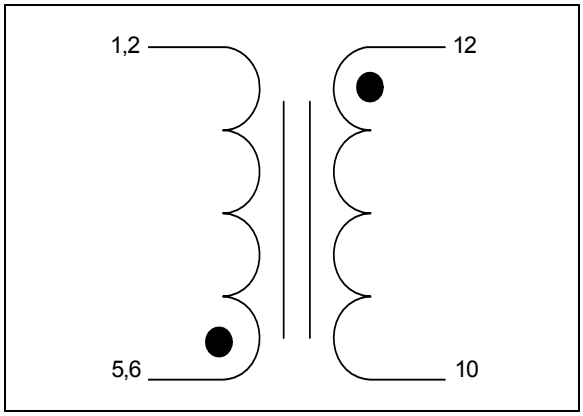
The selected bobbin and core for the flyback transformer are in-lined, 12-pin RM14 bobbin, and standard size 3C90 core material. The RM core has a better surface area to cross-sectional area, which reduces the required primary number of turns while still supporting the large magnetizing inductance. The core material is a popular choice for this switching frequency.

The following describes the transformer construction:

- Primary Number of Turns: 6
- Turn Ratio: 7
- Core Gap Size: 1.27mm
- Primary/Secondary Construction: Litz Wire
- Primary Winding Structure: 4 parallel bundles of 40 gauge, 41 strands
- Secondary Winding Structure: 2 parallel bundles of 40 gauge, 41 strands
- Effective Window Utilization: 80%
- Vacuum Varnished in Dolph's BC-346

Figure 10 shows the pinout of the transformer.

FIGURE 10: FLYBACK TRANSFORMER DIAGRAM



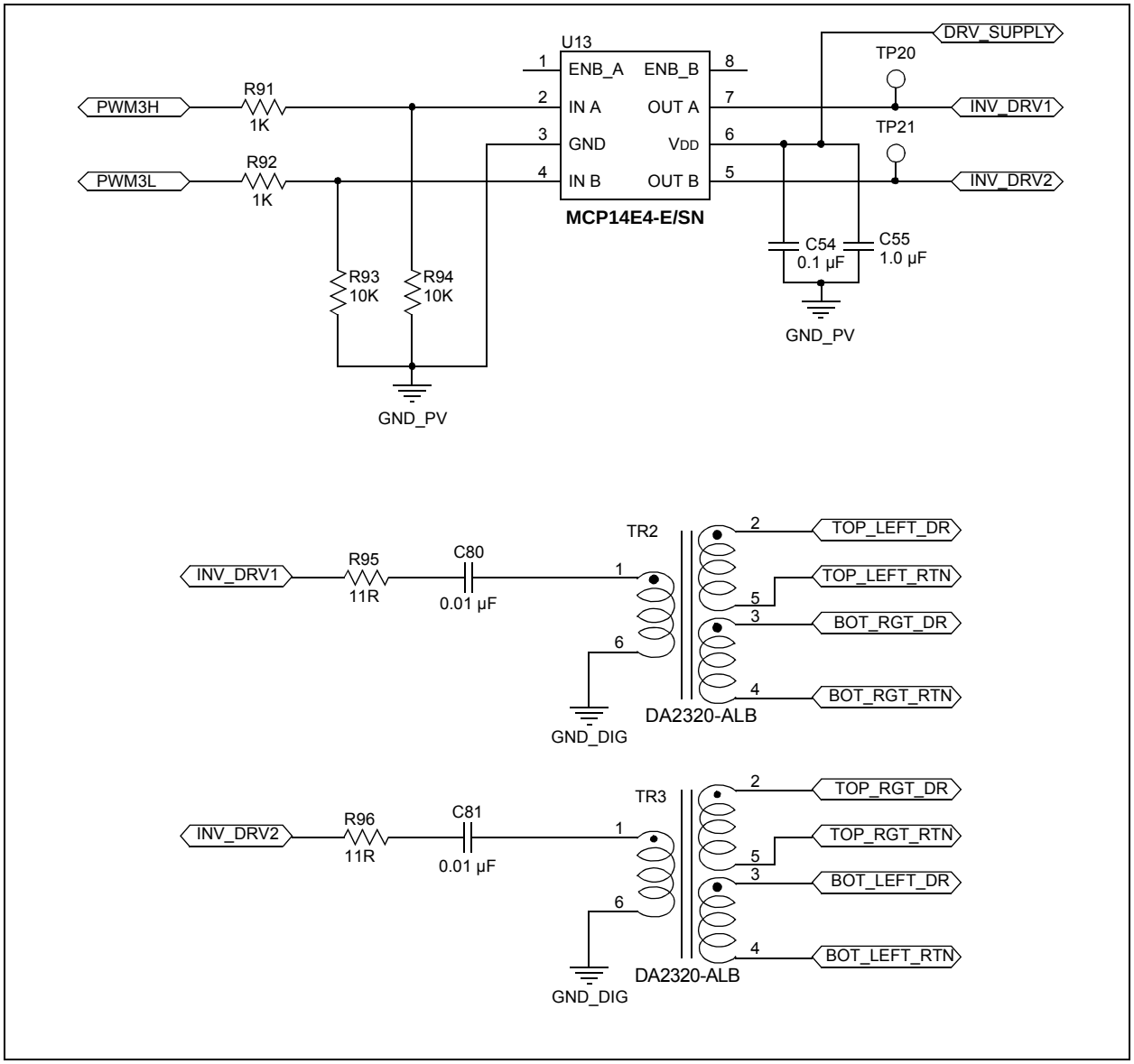
Unfolding Bridge Circuit Design

A full-bridge type circuit is connected to the output of the flyback converter. The full-bridge circuit is an unfolding circuit for the rectified output voltage of the flyback that controls the direction of power flow to the grid.

Figure 11 shows the isolated drive circuit for the unfolding bridge MOSFETs.

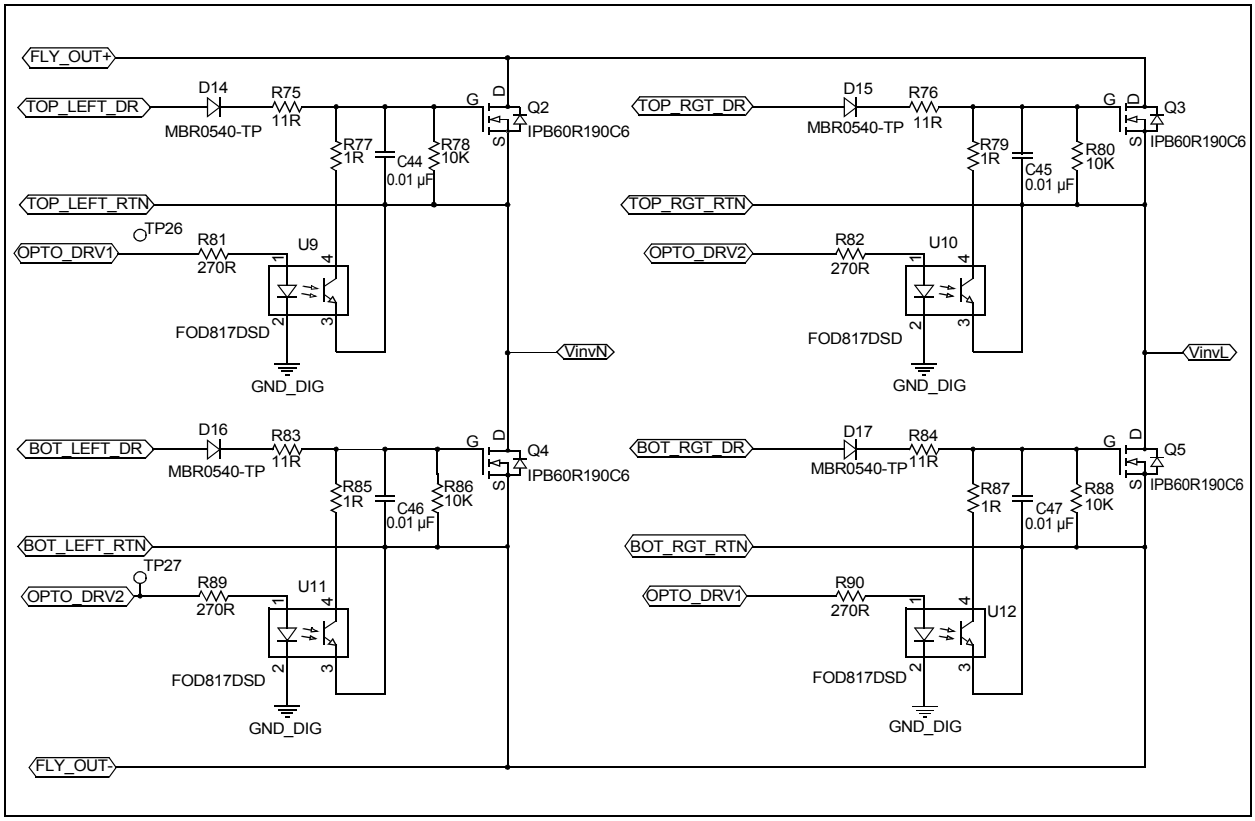
To maintain galvanic isolation, small gate drive transformers are used to drive both high-side and low-side MOSFETs. A high-frequency (228 kHz), fixed duty cycle (50%), PWM drive signal drives the gate drive transformers. To prevent saturation of the gate drive transformers, ceramic capacitors are added in series between the output of the driver IC and the gate drive transformer. These capacitors remove the DC offset which will drive the MOSFETs with a 6-volt drive signal.

FIGURE 11: FULL-BRIDGE DRIVE CIRCUIT



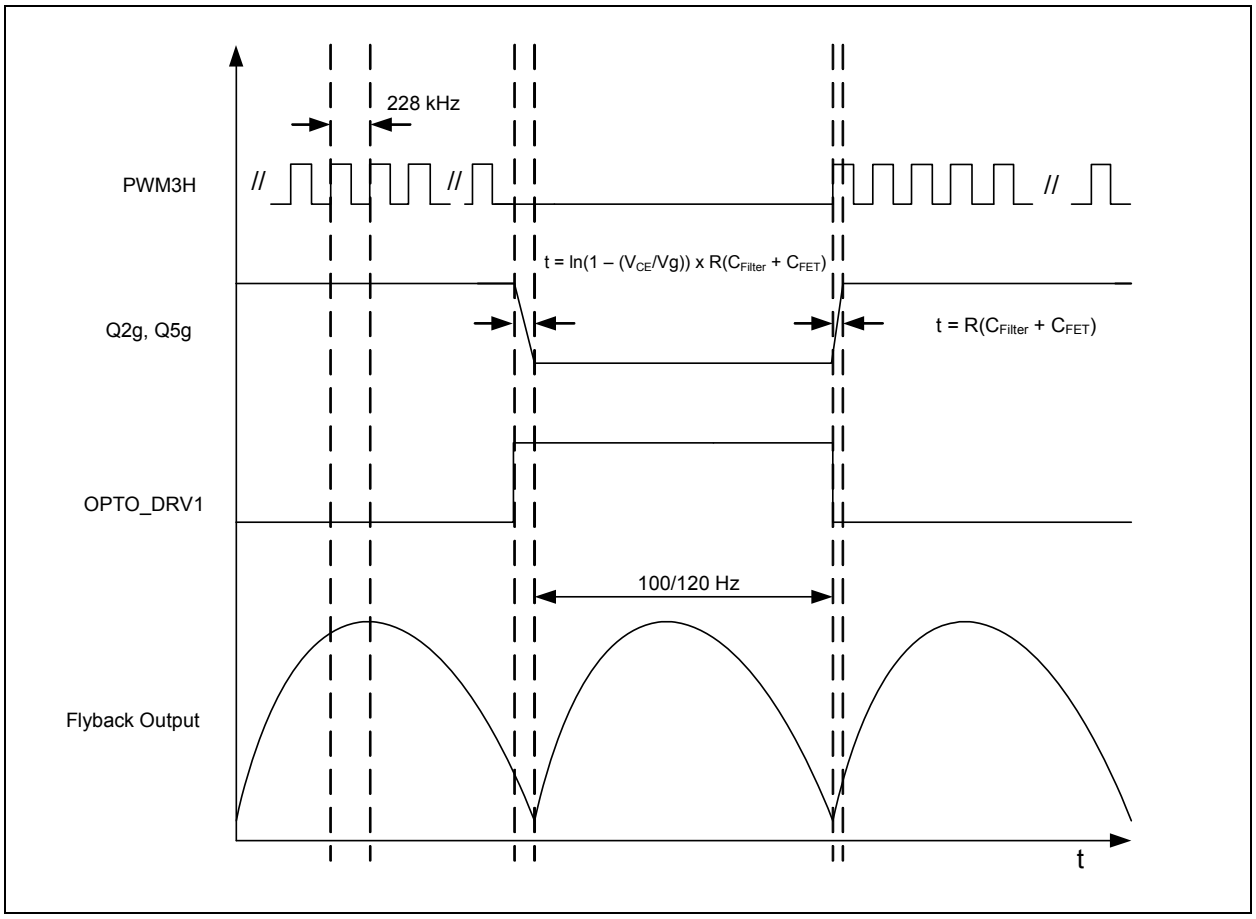
On the output of the drive transformers are low-pass filters that generate a pure DC voltage for driving the full-bridge MOSFETs at 2x the line frequency (100 Hz/ 120 Hz). This reduces switching losses as the MOSFETs are switched on and off near the zero cross (voltage/current near zero). Optocouplers are added across the gate-to-source of the full-bridge MOSFETs to create a fast discharge path when the MOSFETs are switched off. Without the optocoupler discharge path, the only element to discharge the gate voltage is the gate-to-source pull-down resistor. The full-bridge unfolding circuit is shown in Figure 12.

FIGURE 12: FULL-BRIDGE UNFOLDING CIRCUIT



The operating waveforms of the unfolding bridge circuit are shown in Figure 13. During one AC half cycle, PWM3H switches and drives one leg of the unfolding circuit (Q2, Q5). When the AC voltage approaches the zero cross, PWM3H is disabled and the optocoupler is enabled (OPTO_DRV1). During the other half cycle, PWM3L drives MOSFET Q3 and MOSFET Q4.

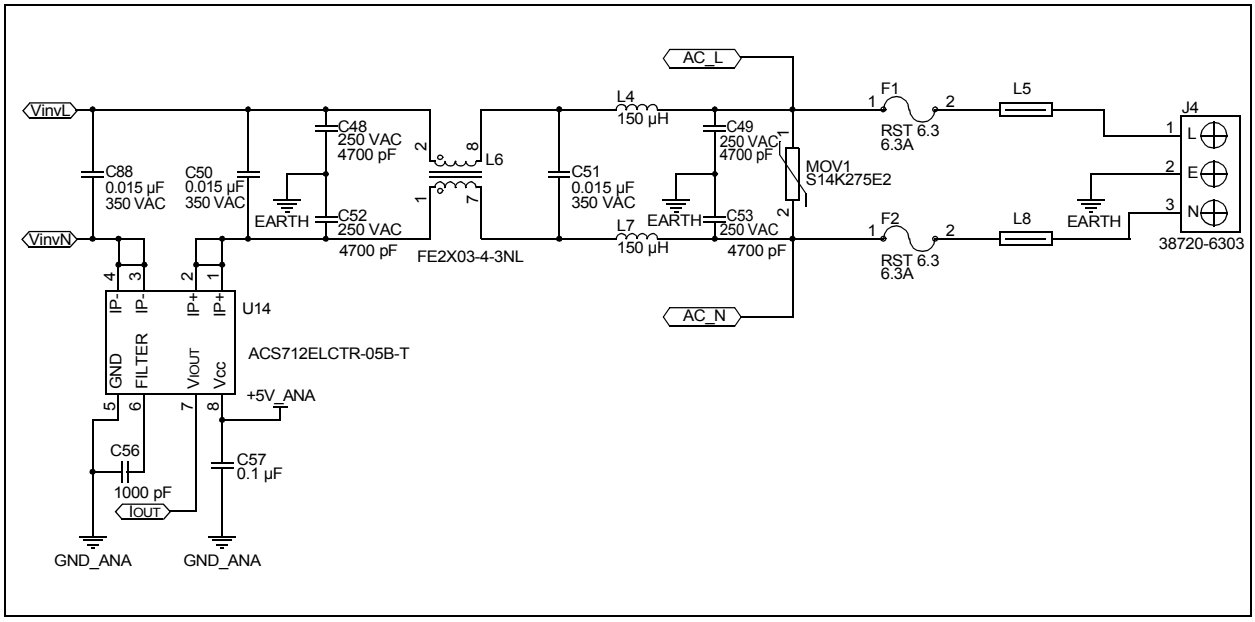
FIGURE 13: FULL-BRIDGE OPERATIONAL WAVEFORMS



EMI Filter

An Electromagnetic Interference (EMI) filter is connected to the output of the full-bridge unfolding circuit. The EMI filter consists of a common-mode choke (L6) and a Differential mode filter (C51 and L4/L7). This filter has been designed with off-the-shelf components that are rated appropriately. At the output of the EMI filter is a 430V varistor across the Line/Neutral terminals, which will add additional protection against transient voltage spikes. After the varistor are two fuses, one in the AC line path and one in the neutral path. The last component in series with the fuse before the output connector is a ferrite bead. The ferrite bead helps at the high end of the frequency spectrum. The schematic of the EMI filter is shown in Figure 14.

FIGURE 14: EMI CIRCUIT



Feedback Networks

The solar microinverter measures/monitors the following feedback networks:

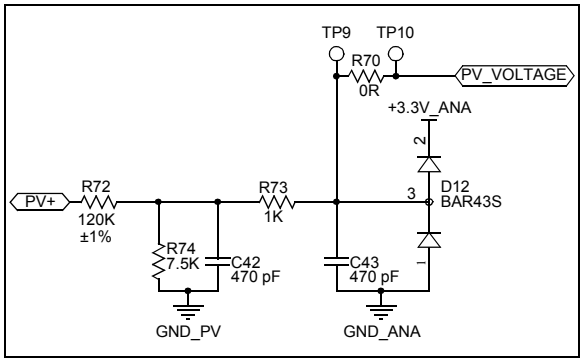
- PV Panel Voltage
- AC Voltage Sense
- AC Current Sense
- Flyback Currents
- Flyback Output Voltage
- AC Zero Cross Detect
- 2.5V Reference Voltage
- 12V Drive Supply

As the Analog-to-Digital Converter (ADC) on the dsPIC® DSC has a range of 0V to 3.3V, additional circuitry is required to accurately measure/monitor most feedback signals above. This section provides circuit schematics of several feedback networks, gain calculations and theory of operation.

PV PANEL VOLTAGE SENSE

The PV panel voltage is scaled using the voltage divisor circuit shown in Figure 15.

FIGURE 15: PV PANEL VOLTAGE SENSE CIRCUITRY



The resistor divider scales down the PV panel voltage to the ADC input voltage level (0-3.3V). Equation 11 computes the gain for the voltage divisor.

EQUATION 11: VOLTAGE DIVISOR GAIN

$$V_{ADC} = V_p \cdot \frac{R74}{R74 + R72}$$

The base voltage, that is the voltage that would give 3.3V on the ADC pin, is approximately 56V. The base voltage is helpful to quickly calculate the voltage at the ADC pin or the Q15 fixed-point number format equivalent. For example, 36V on the PV panel voltage would equal 2.11V on the ADC pin (36/56 * 3.3) or 21,027d in Q15 format (36/56 * 32767).

Resistor, R73, and capacitors, C42/C43, are used for additional signal filtering. Diode, D12, provides protection if the voltage on the analog pin of the dsPIC DSC exceeds 3.3V.

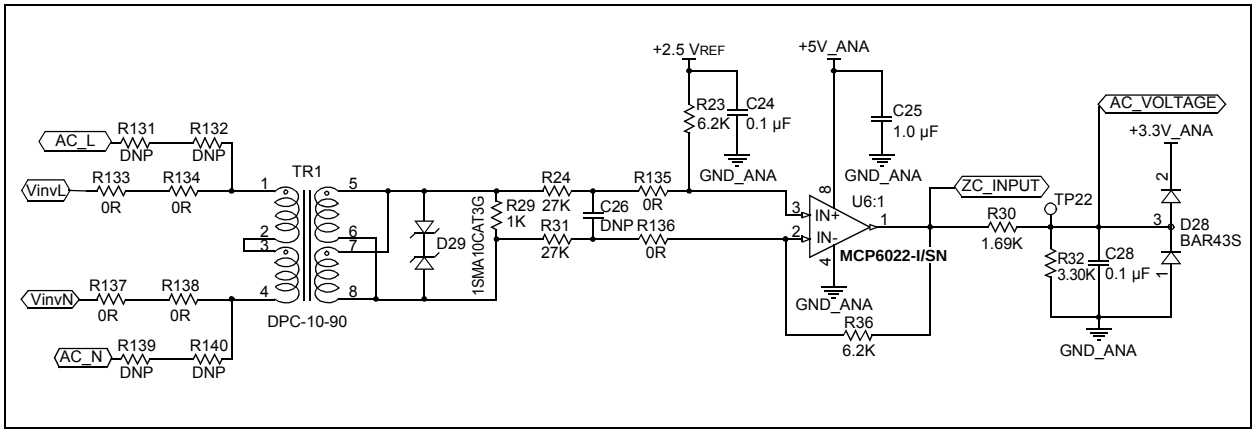
The sensed PV panel voltage is used for Maximum Power Point tracking, voltage feed forward compensation and for protection.

AC VOLTAGE SENSE

To maintain galvanic isolation, a low-power 50/60 Hz transformer is added to the microinverter output to measure the grid voltage. The Line/Neutral sense points for the AC sense transformer are taken before the output EMI filter to avoid impacting EMI performance. A Transient Voltage Suppression (TVS) diode has been added to the output of the transformer to protect the op amp and dsPIC DSC from high-voltage transients (spikes).

Figure 16 shows the AC voltage sense schematic.

FIGURE 16: AC VOLTAGE SENSE CIRCUITRY



The base voltage for the AC voltage sense is approximately 445V. Equation 12 computes the gain for the voltage sense circuit.

EQUATION 12: VOLTAGE SENSE CIRCUIT GAIN

$$V_{ADC} = \left[\left(\frac{V_{grid\_pk}}{N_{TR1}} \cdot \frac{R36}{R31}\right) + 2.5V\right] \cdot \frac{R32}{R30 + R32}$$

As seen in Figure 16, a 2.5V offset is added into the circuit to force the AC voltage positive.

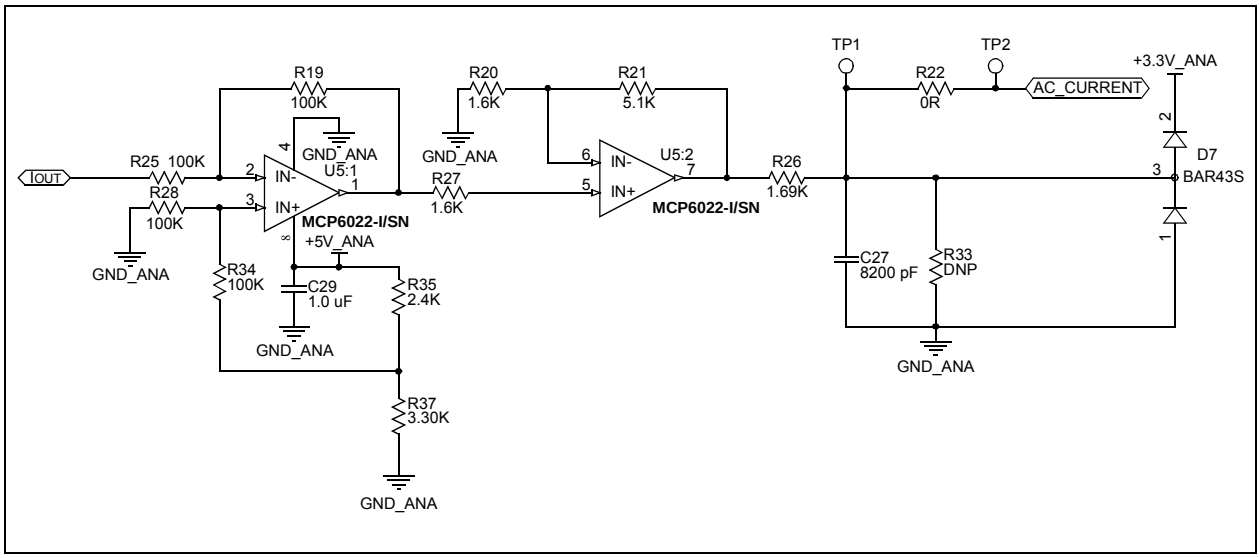
A resistor divider network is added to the output which scales the offset to 1.65V on the dsPIC DSC. Capacitor, C26, and resistors, R135/R136, can be used for a low-pass filter if necessary.

AC CURRENT SENSE

A Hall effect-based linear current sensor is connected between the inverter output and the grid. This current sense IC measures the inverter output current flowing into the grid. The selected Hall effect current sensor can measure current with 80 kHz bandwidth. It provides 2.1 kV of isolation between the high AC voltage and the low output voltage. The output sensitivity of the selected current sensor is fairly low at 180 mV/A with an offset of 2.5V.

The output of the current sensor IC is fed to the inverting pin of op amp, U5, and an offset voltage is fed to the non-inverting pin. The output of the op amp is amplified by a non-inverting amplifier and is fed to the analog channel of the ADC. The effective current signal at the ADC pin of the dsPIC DSC will have an offset of 1.65V. Figure 17 shows the AC current sense schematic.

FIGURE 17: AC CURRENT SENSE CIRCUITRY



The base current for the AC current sense is approximately 2.14A. Equation 13 computes the gain for the current sense circuit.

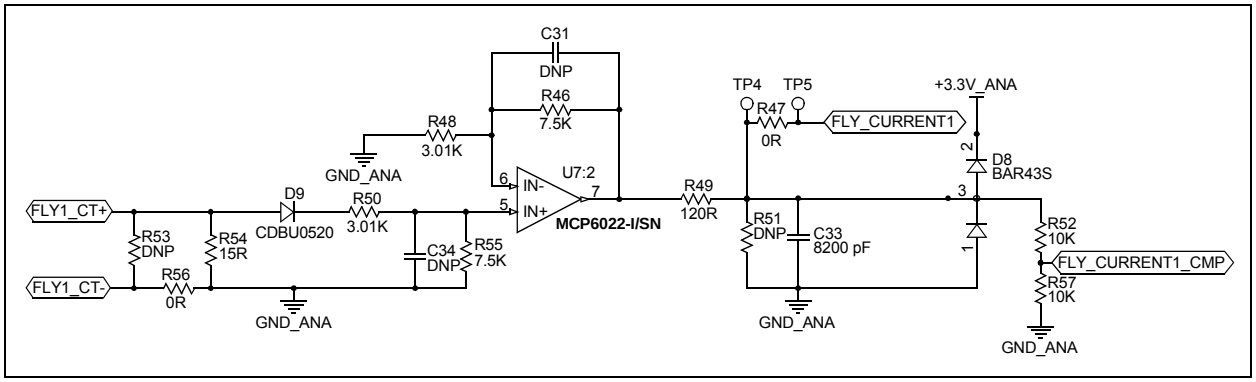
EQUATION 13: CURRENT SENSE CIRCUIT GAIN

$$V_{ADC} = 2 \cdot \left[5 \cdot \left(\frac{R37}{R37 + R35}\right) \cdot \left(\frac{R28}{R28 + R34}\right)\right] - V_{U14} \cdot \left(1 + \frac{R21}{R20}\right)$$

FLYBACK CURRENT SENSE

Current Sense Transformers (CT) are used to measure the flyback currents. The CTs have been placed between the flyback transformer and the flyback MOSFET. This method offers galvanic isolation, if necessary, but also reduces losses as compared to traditional shunt circuits. Figure 18 shows the flyback current sense schematic.

FIGURE 18: FLYBACK CURRENT SENSE CIRCUITRY



The selection of the CT depends on the current handling capabilities, the number of turns (n) on the secondary of the transformer and the external current sense resistor, known as the burden resistor. The current transformer turns ratio and the burden resistor are chosen to minimize the losses seen across the burden resistor. The peak power dissipated across the burden resistor can be calculated by Equation 14.

EQUATION 14: PEAK POWER DISSIPATION

$$P_{loss\_pk} = \left(\frac{I_{LM\_pk}}{N_{TR5}}\right) \cdot R54$$

A non-inverting op amp, with a gain of ~3.5, amplifies the voltage across the burden resistor into the ADC voltage range.

A resistor divider network is added to the output of the flyback current sense for overcurrent protection using the on-board analog comparators. This allows maximum range on the ADC and will provide quick shutdown of the PWM module in the event of an overcurrent condition. The exact gain of the flyback current sense network is provided in Equation 15. The base current for a single phase is approximately 13.5A.

EQUATION 15: GAIN OF FLYBACK CURRENT

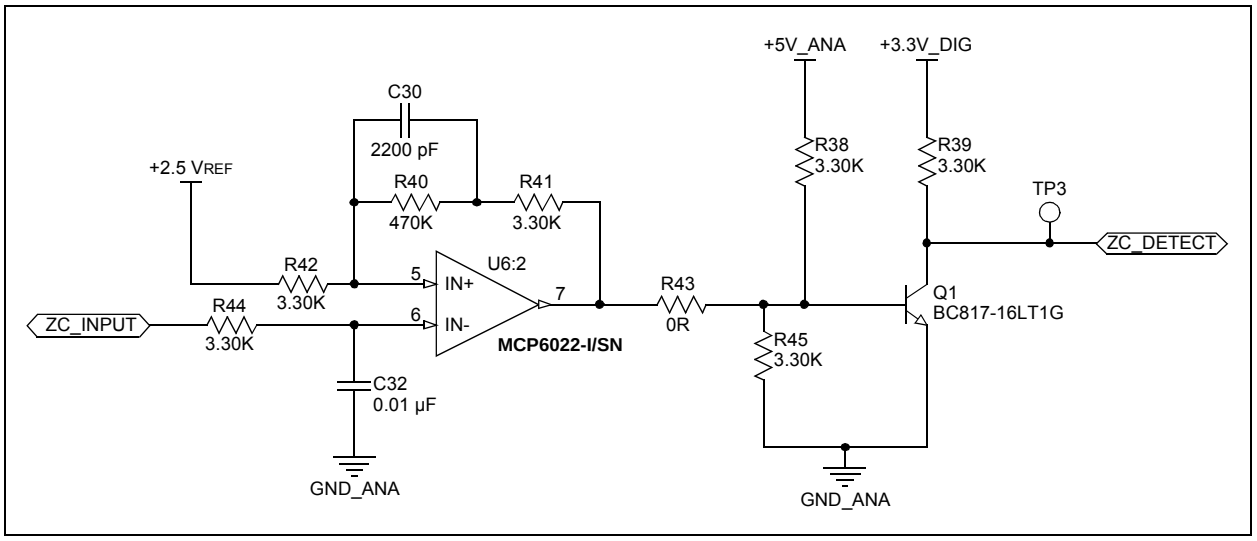
$$V_{ADC} = \left[\left[\left(\frac{I_{LM\_pk}}{N_{TR5}}\right) \cdot R54\right] - V_{D9}\right] \cdot \left(\frac{R55}{R55 + R50}\right) \cdot \left(1 + \frac{R46}{R48}\right)$$

HARDWARE ZERO CROSSING

A zero cross detect circuit has been added to detect the change in grid voltage state (i.e., +ve to -ve) and to change the state of an I/O port (PORT RB15) on the dsPIC DSC accordingly. As the grid voltage state changes from negative to positive, it changes the state of PORT RB15 from low-to-high and vice-versa.

The output of the AC voltage differential amplifier, U6:1, is compared with the 2.5V reference by comparator, U6.2. The comparator output drives transistor, Q1, as shown in Figure 19. To avoid false triggering of the comparator, a hysteresis band of ~10 mV is added using R40, R41 and C30.

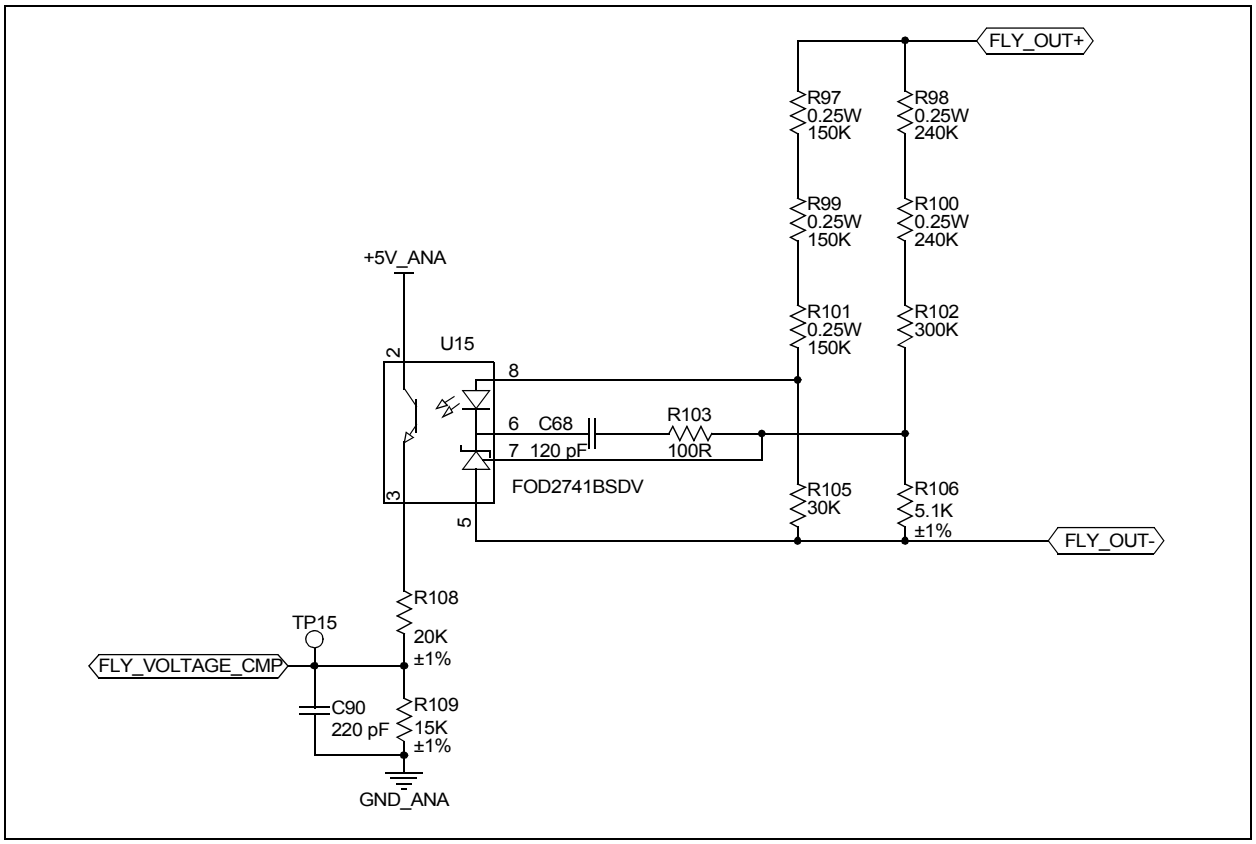
FIGURE 19: ZERO CROSS DETECT CIRCUIT



FLYBACK OVERVOLTAGE PROTECTION

An optically isolated error amplifier, consisting of a reference voltage, an error amplifier and an optocoupler, is connected to the flyback output to protect the microinverter in the event that the flyback secondary becomes open circuit (i.e., high-side, full-bridge MOSFET fails to turn on). If the flyback secondary becomes open, it is possible for the output voltage on the flyback to rise to catastrophic limits. The flyback overvoltage protection circuit is shown in Figure 20.

FIGURE 20: FLYBACK OVERVOLTAGE PROTECTION CIRCUIT



This circuit will remain non-operational until the voltage rises beyond the set flyback maximum voltage limit. In order for the optocoupled signal to be enabled, the voltage at the reference pin must be 2.5V. Equation 16 calculates the required flyback output voltage to generate 2.5V on the reference pin.

EQUATION 16: REQUIRED FLYBACK OUTPUT VOLTAGE

$$V_{flyback\_output} \cdot \frac{R106}{R106 + R102 + R100 + R98} > 2.5V$$

At this time, the LED would become forward biased and the current flowing through the circuit is limited by the resistor network, R97, R99 and R101.

The maximum forward current that the LED will carry is expressed in Equation 17.

EQUATION 17: MAXIMUM LED FORWARD CURRENT VOLTAGE

$$I_{LED} = \frac{V_{flyback\_output}}{R101 + R99 + R97} \cong 866uA$$

With 866 µA of current on the primary and a minimum Current Transfer Ratio (CTR) of 100%, the current seen on the low voltage or isolated side is also 866 µA. As the operating temperature of the system can be 65º Celsius, a CTR of 60% has been taken to ensure reliability. The phototransistor collector current will now be calculated at 520 µA. This current will impact the resistor values for the voltage divider on the isolated side. When the voltage at Test Point 15 is high (~1.6V), the analog comparator interrupt is generated and the PWM outputs are disabled.

AUXILIARY POWER DESIGN

The auxiliary power supply provides power to all on-board electronics, such as the dsPIC DSCs, gate drive ICs and operational amplifiers. For a solar microinverter, there are a few different options for deriving the auxiliary power. One option is to use a small bridge rectifier and a flyback converter connected to AC mains. Another option is to use a flyback converter connected to the PV module input. If connected to AC mains, it should be noted that there are nighttime power consumption limitations that must be met. In both instances, the flyback converter can provide isolated auxiliary power that may be required for some drive circuitry.

For this reference design, a constant on-time buck switching regulator (LM5008A) is connected to the PV module to generate a regulated 12V output. As this reference design supports several different PV modules with a wide input voltage range, a proper buck switching regulator should be selected. The regulated 12V output is used for driving the flyback MOSFETs, full-bridge MOSFETs and the remaining auxiliary power sections. The nominal efficiency of the buck regulator is 90%. At approximately 100 mA of load current, the typical losses in the buck regulator are 125 mW. Figure 21 shows the circuit for the 12V drive supply. A second high-efficiency, step-down voltage regulator (MCP16301) steps down the 12V drive supply to 5V, as shown in Figure 22.

FIGURE 21: 12V DRIVE SUPPLY CIRCUIT

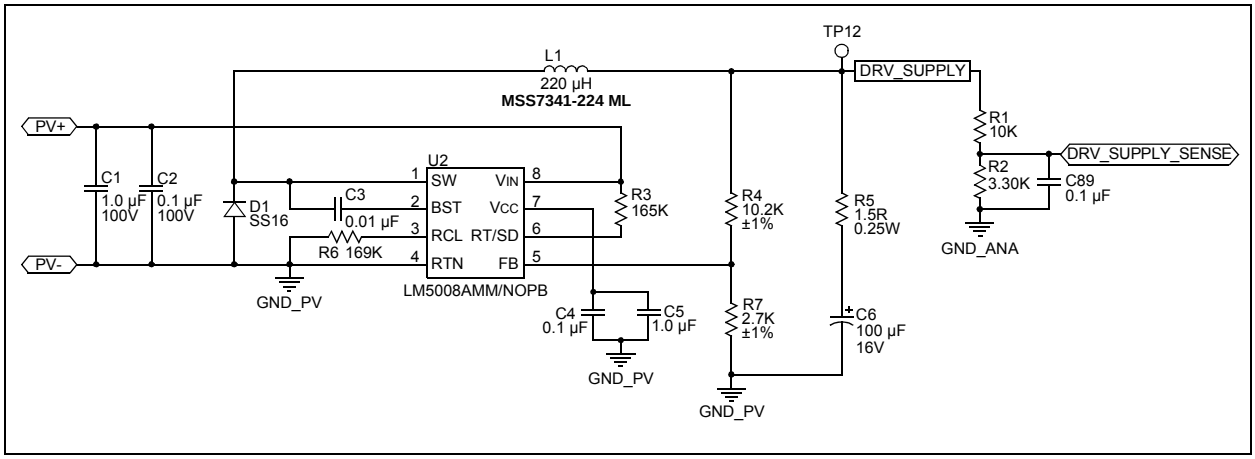
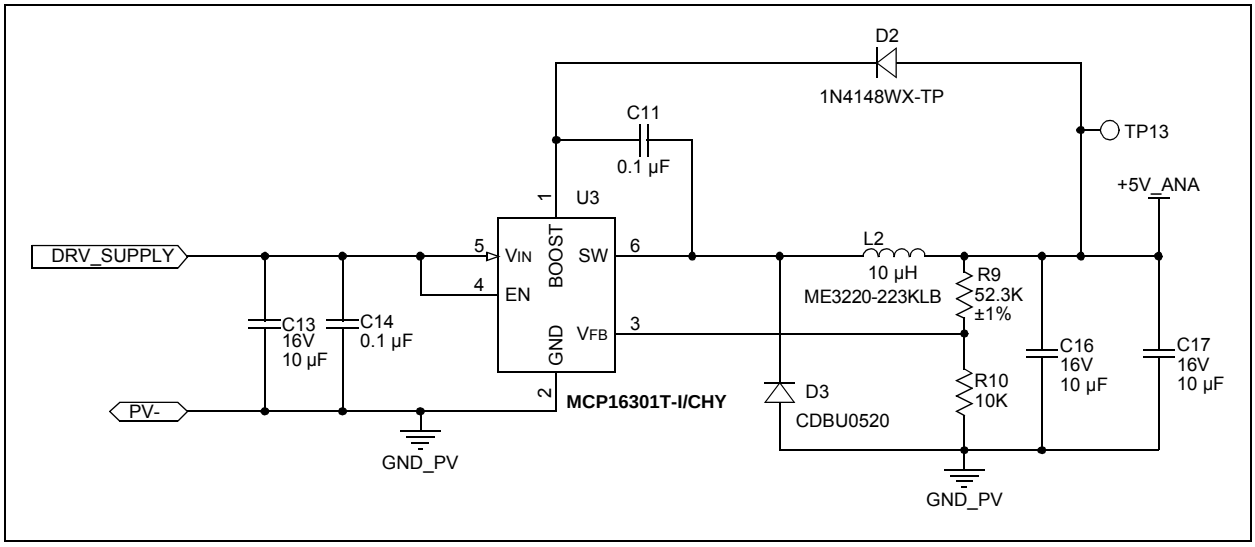


FIGURE 22: 5V DRIVE SUPPLY CIRCUIT



This auxiliary power supply rail is used for the Hall effect-based linear current sensor IC, an optically isolated error amplifier and several rail-to-rail operational amplifiers. Nominal efficiency of the step-down buck regulator is 90%, and at a load current of 135 mA, the total losses in the regulator are approximately 75 mW.

A low quiescent current LDO (Low Dropout) voltage regulator is used to generate the 3.3V drive supply for the dsPIC devices and on-board temperature sensor. At a typical load current of 120 mA, the approximated losses seen in the LDO are 12 mW.

The total losses in the auxiliary power section are approximately 1.2W. This would change slightly with the changing of the PV input voltage.

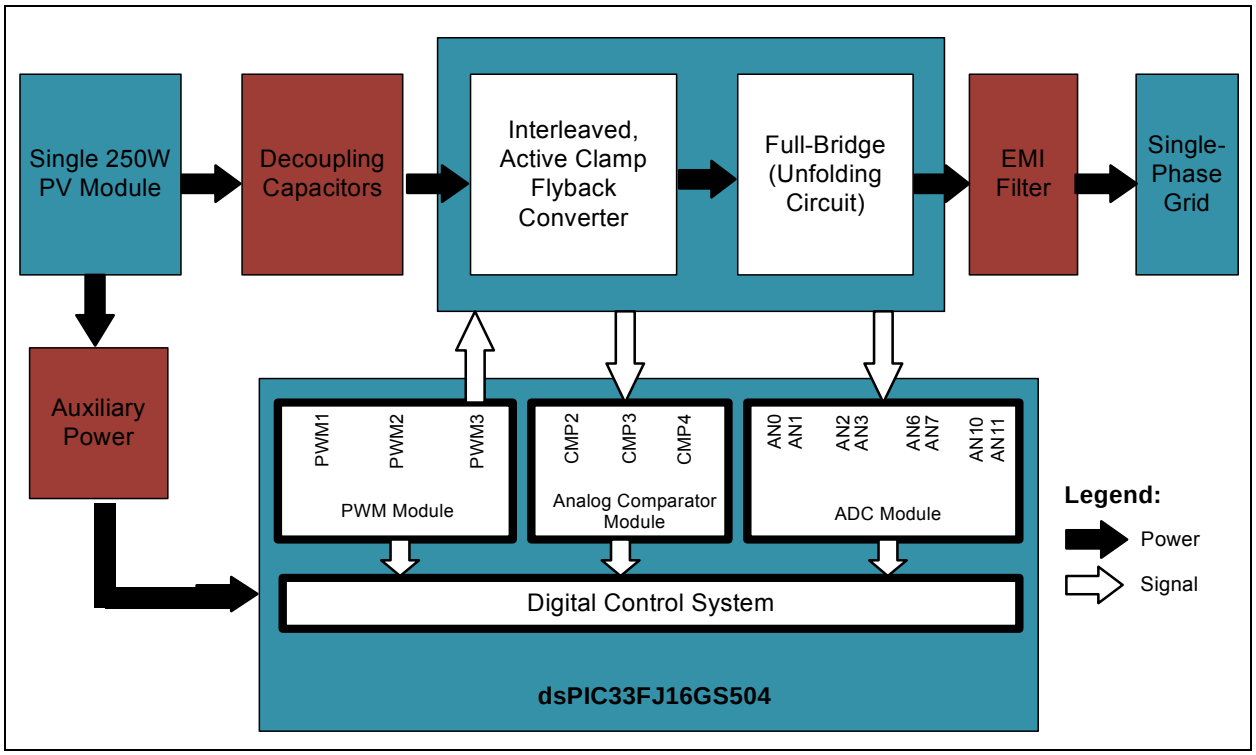
SOFTWARE DESIGN

The Solar Microinverter Reference Design is controlled by a single dsPIC DSC device, as shown in the system block diagram in Figure 23. The dsPIC DSC device is the heart of the Solar Microinverter Reference Design and controls all critical operations of the system as well as the housekeeping operations.

The functions of the dsPIC DSC can be broadly classified into the following categories:

- Digital Power Conversion Algorithms
- State Machine for Different Modes of Operation
- Maximum Power Point Tracking (MPPT)
- Digital Phase Lock Loop (PLL)
- System Islanding and Fault Handling
- Communication via Power Line or Wireless (not implemented)

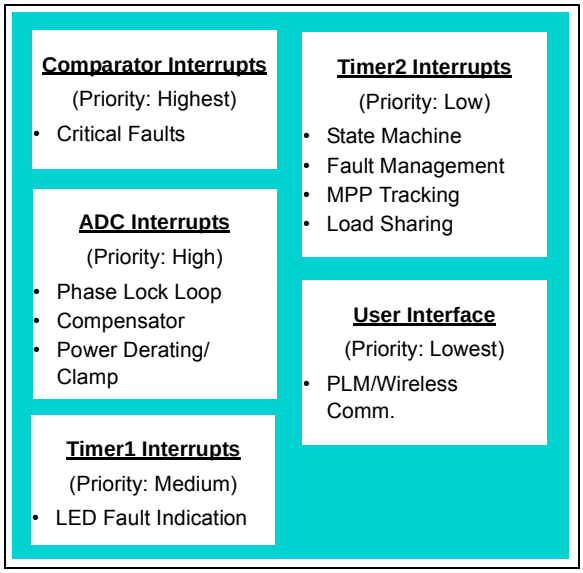
FIGURE 23: SYSTEM BLOCK DIAGRAM



A high-level block diagram of the solar microinverter software structure is shown in Figure 24. As shown in this figure, the software is partitioned into five parts:

- User Interface
- Timer2 Interrupt Service Routine (10 kHz)
  - MPP Tracking (AC Frequency/3)
  - Load Sharing (5 kHz)
- Timer1 Interrupt Service Routine (3.3 Hz)
- ADC Interrupt Service Routine (56 kHz)
- Analog Comparator Interrupts

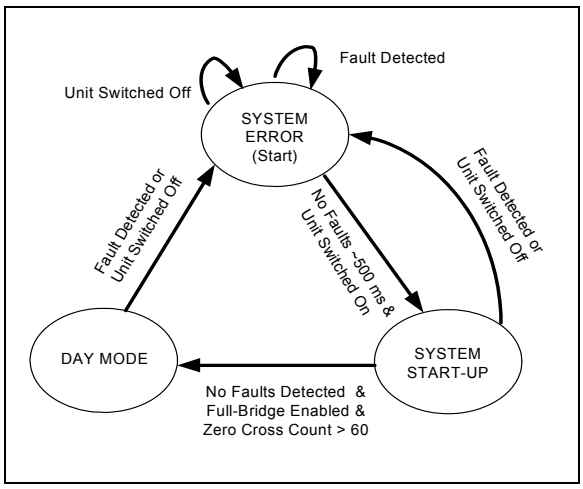
FIGURE 24: HIGH-LEVEL SOFTWARE BLOCK DIAGRAM



STATE MACHINE

The solar microinverter software implements a state machine to determine the mode of operation for the system. The state machine is executed, once every 100 µs, inside a timer Interrupt Service Routine (ISR). As shown in Figure 25, there are three system states: System Error, System Start-up and Day mode.

FIGURE 25: STATE TRANSITION DIAGRAM



System Error

At power-up, the system state is initialized to system error. If the system does not detect a Fault for 500 ms, and the on/off switch is in the ON position, the state machine switches to system start-up.

The system state switches to System Error mode if the on/off switch is switched OFF or if any of the following Faults occur:

- Grid under/overvoltage
- Grid under/over frequency
- Flyback MOSFET overcurrent
- Flyback output overvoltage
- Inverter output overcurrent
- PV under/overvoltage
- Overtemperature
- Drive supply under/overvoltage
- Hardware zero cross
- AC current sense offset
- 2.5V reference under/overvoltage

As soon as the system switches to system error, the PWM drive signals are disabled and placed into a “safe” state, several global variables/flags are re-initialized and a timer is initialized to blink an LED for Fault indication.

System Start-up

During system start-up, the AC current offset is measured and averaged, all Faults are continuously monitored and the full-bridge unfolding circuit is enabled after several successive zero cross events. After the full-bridge circuit has been enabled, the system waits for several more zero cross events to occur before switching the system state to Day mode. During this time, if a Fault occurs or if the on/off switch is switched to the OFF position, the system state will switch back to system error.

Day Mode

Normal operation of the solar microinverter occurs during Day mode. In this mode, the solar microinverter is fully operational and is delivering the maximum available energy from the PV panel to the single-phase grid. The Maximum Power Point and load sharing functions are called in Day mode.

During this time, if a Fault occurs or if the on/off switch is switched to the OFF position, the system state will switch to a system error.

DEVICE PERIPHERAL CONFIGURATION

The dsPIC DSC device offers high-speed, intelligent power peripherals, specifically designed for power conversion applications. These intelligent power peripherals include the High-Speed PWM, High-Speed 10-Bit ADC and High-Speed Analog Comparator modules. These peripheral modules include features that ease the control of any Switch Mode Power Supply with a high-resolution (1.04 ns) PWM, flexible ADC triggering and comparator Fault handling. In addition to the intelligent power peripherals, the dsPIC DSC also provides built-in peripherals for digital communications, including I^2C™, SPI and UART modules, that can be used for power management and housekeeping functions. This section will discuss how the PWM, ADC and analog comparators have been setup/configured in software.

PWM Configuration

A total of three PWM generators (PWMxH/PWMxL) are used in the system. Two PWM generators (one with a 180 degree phase shift) drive the interleaved active clamp flyback and one PWM generator drives the full-bridge unfolding circuit. The active clamped flyback PWM generators are configured for Complementary mode with a fixed dead time. Dead time is configured for 50 ns and the alternate dead time has been configured for 250 ns. To drive the P-Channel MOSFET, PWMxL has been inverted (active-low) with respect to PWMxH. Figure 9 shows the PWM gate drive waveforms of the single stage, active clamp flyback converter.

For both flyback converters, the PWM Latched Fault mode has been enabled for overcurrent protection. In the event there is an overcurrent condition, the analog comparators will trigger the PWM module to shut down in a latched manner. To prevent sporadic shutdowns due to noise at MOSFET switching instants, Leading Edge Blanking (LEB) has been enabled at MOSFET turn-on, as well as MOSFET turn-off. The LEB counter has been configured for 240 ns.

The Full-Bridge unfolding drive circuit is shown in Figure 11. The PWM generator has been configured for independent time base switching at a frequency that is four times that of the flyback converter (~228 kHz). A single PWM channel switches for one half cycle and then is placed in an override state while the other PWM channel switches. The duty cycle of the PWM channels is fixed at 50% and dead time is disabled.

Analog-to-Digital Converter (ADC) Configuration

PWM1 and PWM2 trigger the ADC to start sampling/converting 4 ADC pairs at precise instances in time. PWM1 triggers ADC Pair 0 and PWM2 triggers the other three ADC pairs (Pair 1, Pair 3 and Pair 5). The ADC module has an internal priority of ANx channels, with ADC Pair 0 having the highest priority. A single ADC interrupt (ADCP3) is used to read the ADC result buffers. When this interrupt is generated (after conversion of Pair 3 is complete), ADC Pairs 0, 1 and 3 are available, and ADC Pair 5 will still be in the process of sampling and converting. Toward the end of the ADC interrupt routine, the result buffers for AN10 and AN11 can be read. At the end of the interrupt, the PWM triggers are updated based on the new PWM duty cycle.

Analog Comparator Configuration

The solar microinverter uses three analog comparator modules for system protection. Two of the comparator modules are used for flyback overcurrent protection and the third module is used for flyback output overvoltage protection. Each module has interrupts enabled. If the Interrupt Service Routine is entered, the system indicates that a critical Fault has occurred. For the overvoltage protection ISR, all PWM channels are placed in an override state and then the critical Fault flag is set. The comparator module will automatically shut down the PWM if the flyback overcurrent limit is exceeded. The reference voltage for the flyback overcurrent protection is variable, based on the operating voltage. This is updated in the system state machine when the system is operating in Day mode.

START-UP ROUTINE

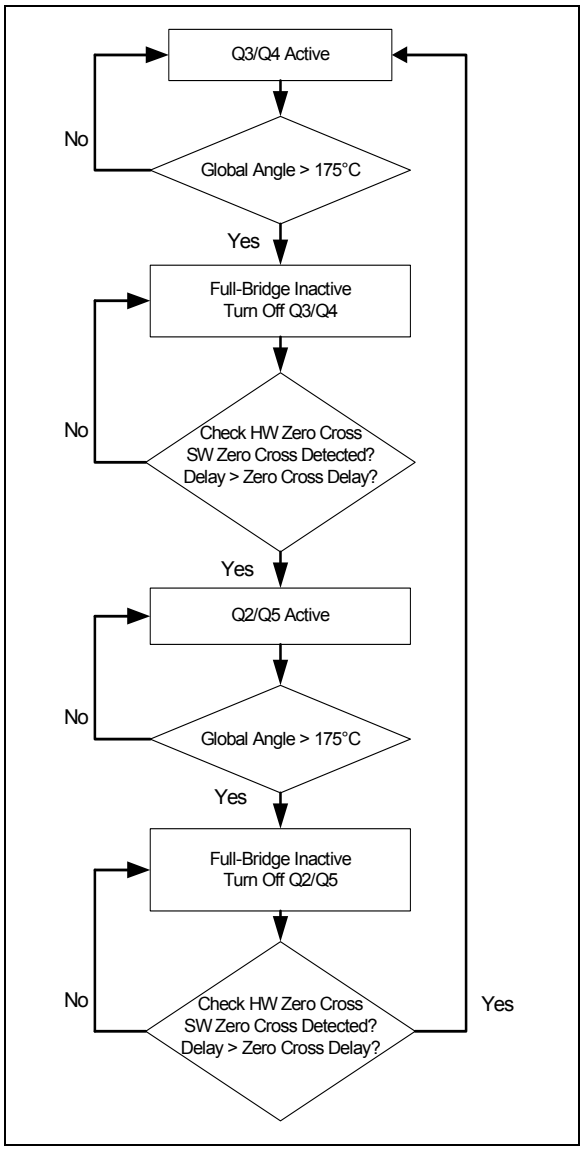
The following section describes the start-up procedure for the solar microinverter. The system powers up in system error, but with no Faults detected. Once the on/off switch is switched to the ON position, and no Faults are present, a restart counter of 500 ms starts. If no Faults have been detected for 500 ms, the system will switch to Start-up mode. If, at any time a Fault occurs during the restart event, the restart counter is reset to zero and the system waits for the Fault to be removed before entering the restart counter routine.

When the system enters Start-up mode, approximately 30 zero cross events are counted before enabling the full-bridge unfolding circuit. The unfolding circuit is enabled at the peak of the AC voltage to eliminate a large inrush current if enabled at the zero crossing. Approximately 30 zero crossings are counted after enabling the full-bridge, unfolding circuit before enabling the flyback converter. If, at any time, a Fault is detected, the system will switch back to system error. To enable the flyback converter, the system state machine switches to Day mode.

FULL-BRIDGE (UNFOLDING CIRCUIT)

Figure 26 shows the flowchart for the state machine that has been implemented to control/determine the proper state for driving the full-bridge unfolding circuit.

FIGURE 26: FULL-BRIDGE FLOWCHART



There are four different states for the full-bridge state machine. Two of the states define an inactive region, and the other two states drive the full-bridge unfolding circuit. All PWM drive signals are in an override state when the state machine is operating in the inactive states.

At each zero cross, the last known hardware zero cross state is compared against the new state to ensure that the hardware zero cross is functional. Before the state machine can switch to an active state, both the hardware zero cross and software zero cross events need to occur. The flyback output voltage never reaches zero volts. When the full-bridge MOSFETs are disabled near the zero cross, there will be some small voltage that remains (~15V) on the flyback output. Because of this, a small delay has been added to give time for the AC voltage to reach the approximated flyback output voltage. This will reduce/eliminate small glitches caused by the difference in voltages. The delay is different for 50 Hz/60 Hz operation.

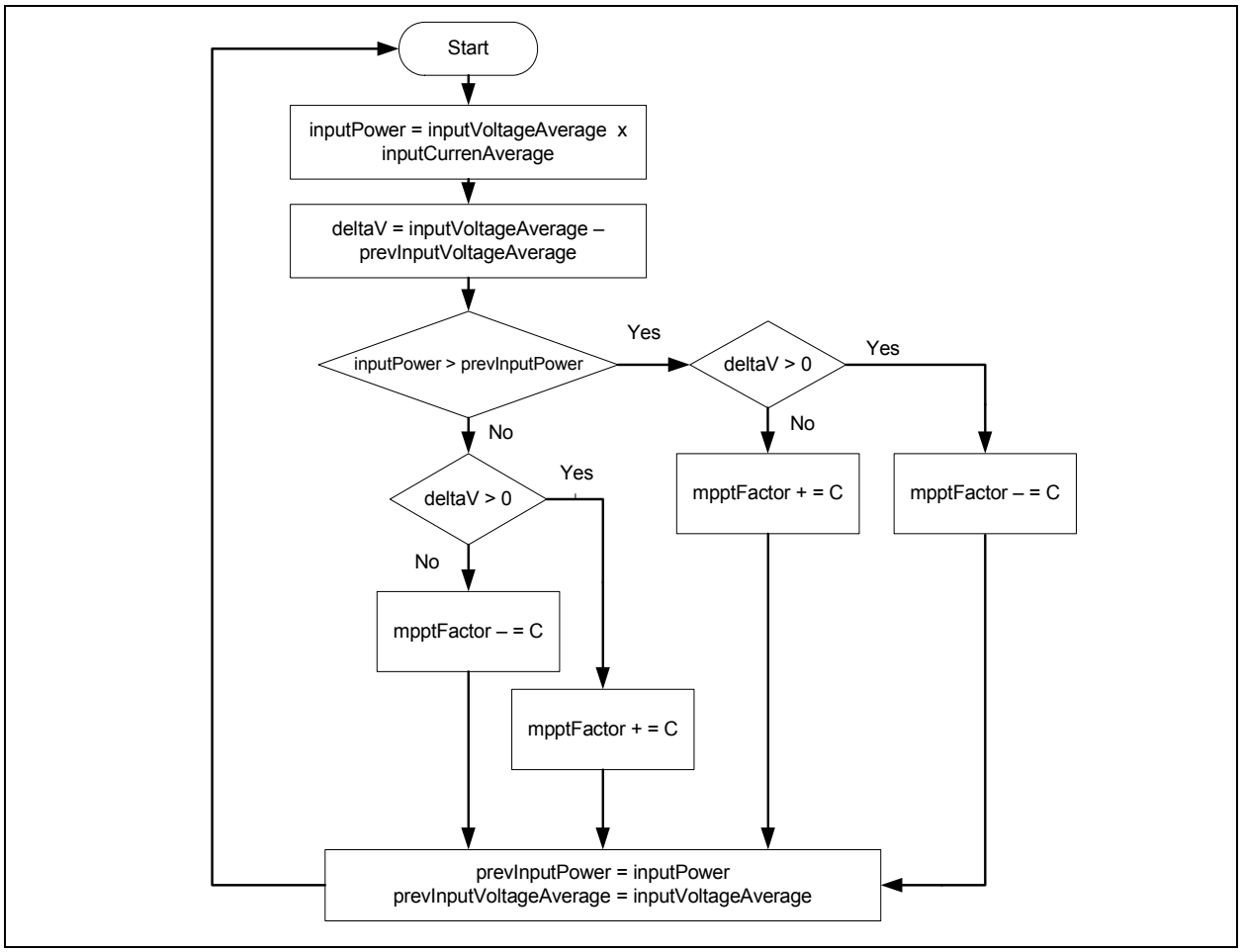
When in an active state, the PWM drive signal remains active until the system global angle is greater than 175 degrees. This event occurs very close to the zero cross event. If, for some reason, the software zero cross is detected before the global angle is greater than 175 degrees, the state of the full-bridge drive is automatically changed to the proper inactive state (depending on the direction of the zero cross event).

MPPT ALGORITHM

There are two algorithms commonly used to track the Maximum Power Point (MPP): the Perturb and Observe (P&O) method, and the Incremental Conductance method. This reference design uses the P&O method for MPPT. The P&O method operates by periodically incrementing or decrementing the current reference based on the measured input power. If a given perturbation leads to an increase (decrease) in the output power of the PV module, the subsequent perturbation is generated in the same (opposite) direction.

The MPPT routine is executed every three AC cycles. The average input voltage and average input current are parameters passed to the MPPT routine. The average input power is calculated here, as well as the change in input voltage. The decision to increment or decrement the `mpptFactor` (current reference) is based on the change in input power and the change in input voltage. Figure 27 provides a software flowchart for the P&O method for Maximum Power Point tracking.

FIGURE 27: SOFTWARE FLOWCHART FOR MPPT



An additional step that can improve the tracking response is to have a second set of increment/decrement factors that are based on the delta voltage. For example, if the system is operating on the right-hand side of the power curve and a given perturbation leads to an increase in power, but the change in voltage is small, the next perturbation could be even larger as the system is operating further away from MPP. Once a larger change in the input voltage is observed, the system is moving closer to the MPP and a smaller perturbation can be made. The same holds true when operating on the left-hand side of the power curve, but when there is a large delta in the input voltage, a large perturbation can be made.

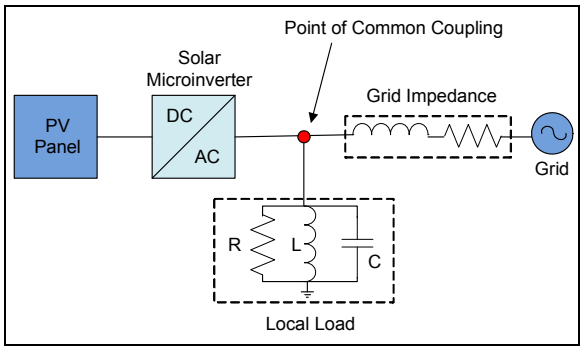
ANTI-ISLANDING

Islanding is the continued operation of the inverter when the grid has been removed intentionally, by accident or by damage. In other words, if the grid has been removed from the microinverter, then the microinverter should stop supplying power to the grid.

All anti-islanding methods can be categorized as being passive or active. In passive methods, usually the grid voltage and grid frequency are monitored, and if either deviate outside of their defined operating range, the microinverter will switch off. Active methods, on the other hand, will inject a small disturbance signal and then monitor the response to determine if islanding has occurred.

Figure 28 shows the power flow of the grid and solar microinverter when the grid is connected. The local load is represented by a parallel connected Resistor, Inductor and Capacitor (RLC) circuit.

FIGURE 28: SYSTEM LEVEL POWER FLOW



When the grid is removed, the microinverter will see the local load. In the event that the local load resonates near the operating frequency before the grid was removed, the microinverter will see a small change in active and reactive power, and will not be able to detect that the grid has shut down. This is known as an island condition and is a Non-Detection Zone (NDZ) for the microinverter. All passive methods have a large NDZ, while active methods have a relatively small NDZ.

There are several different active methods that can be used to reduce the NDZ. A few of the common active methods are:

- Frequency Jump
- Slip Mode Frequency Shift
- Impedance Measurement
- Active Frequency Drift
- Sandia Frequency Shift
- Sandia Voltage Shift

Almost all active methods will impact (degrade) the output power quality of the solar microinverter.

The Sandia Frequency Shift (SFS) uses positive feedback to push the microinverter output current frequency out of the defined operating range, causing the microinverter to shut down. This is done by introducing a small misalignment in phase angle by truncating/extending the output current and then monitoring the next cycle to see how the grid frequency was impacted. If the grid is present, the grid frequency will not change when the disturbance is injected. However, as soon as the grid is removed, the resonating frequency of the local load will change when the disturbance is injected.

The Sandia Frequency Shift can be implemented using Equation 18. Where $fm - fline$ is the difference between measured frequency and the line frequency, K is an accelerated gain and cf_0 is the chopping fraction when there is no error in frequency. As seen by Equation 18 below, the chopping fraction is accelerated as the frequency moves further away from the operational frequency of the line.

EQUATION 18: SFS IMPLEMENTATION

$$cf = cf_o + K(fm - fline)$$

In addition to the SFS, the Sandia Voltage Shift (SVS) method can also be used to reduce the Non-Detection Zone. SVS also uses positive feedback and adjusts the amplitude of the microinverter output current, based on changes in the grid RMS voltage. When the grid is connected, there will be little to no change in the grid RMS voltage, but if the grid was removed and the output current increased/decreased, the voltage at the point of common coupling will change. It is possible to increase or decrease the output current, but it is recommended to decrease the current to prevent or reduce the chance of damaging the microinverter.

The initial release of the solar microinverter software only implements the passive method for islanding detection by monitoring both the grid voltage and grid frequency. A future software release is planned that will incorporate an active method along with the existing passive method.

PHASE LOCK LOOP

In systems connected to the grid, a critical component of the inverter's control system is the ability to synchronize the inverter's output current with the grid voltage. This is done by use of a Phase Lock Loop (PLL). The PLL generates the grid voltage frequency and phase angle. The estimated frequency, ωe, and phase angle, θe, of the grid voltage can be used not only for control and signal generation, but also for protection against island situations. Refer to **"Anti-Islanding"** for more details.

If the inverter's PLL is unable to synchronize to the grid voltage accurately, the output power factor, harmonics and efficiency may be impacted. In software, the grid voltage is sampled every ADC interrupt (rate of 17.8 µs). In every sample, the grid voltage polarity is checked. If there is a change in the grid voltage polarity, the software sets a zero cross detect flag. The number of ADC interrupts between each zero cross determines the period value.

The period value is then used to determine the phase angle increment for the sine table reference. The sine table consists of 512 elements which generates a 0 to 90 degree sine reference, with 32767 equaling 90 degrees. As 90-180 degrees of the sine reference is a mirror image of that of 0 to 90 degrees, the sine reference only needs to consist of 0 to 90 degrees. Equation 19 determines the phase angle for the sine table reference based on the inverter period (calculated each AC half cycle).

EQUATION 19: PHASE ANGLE

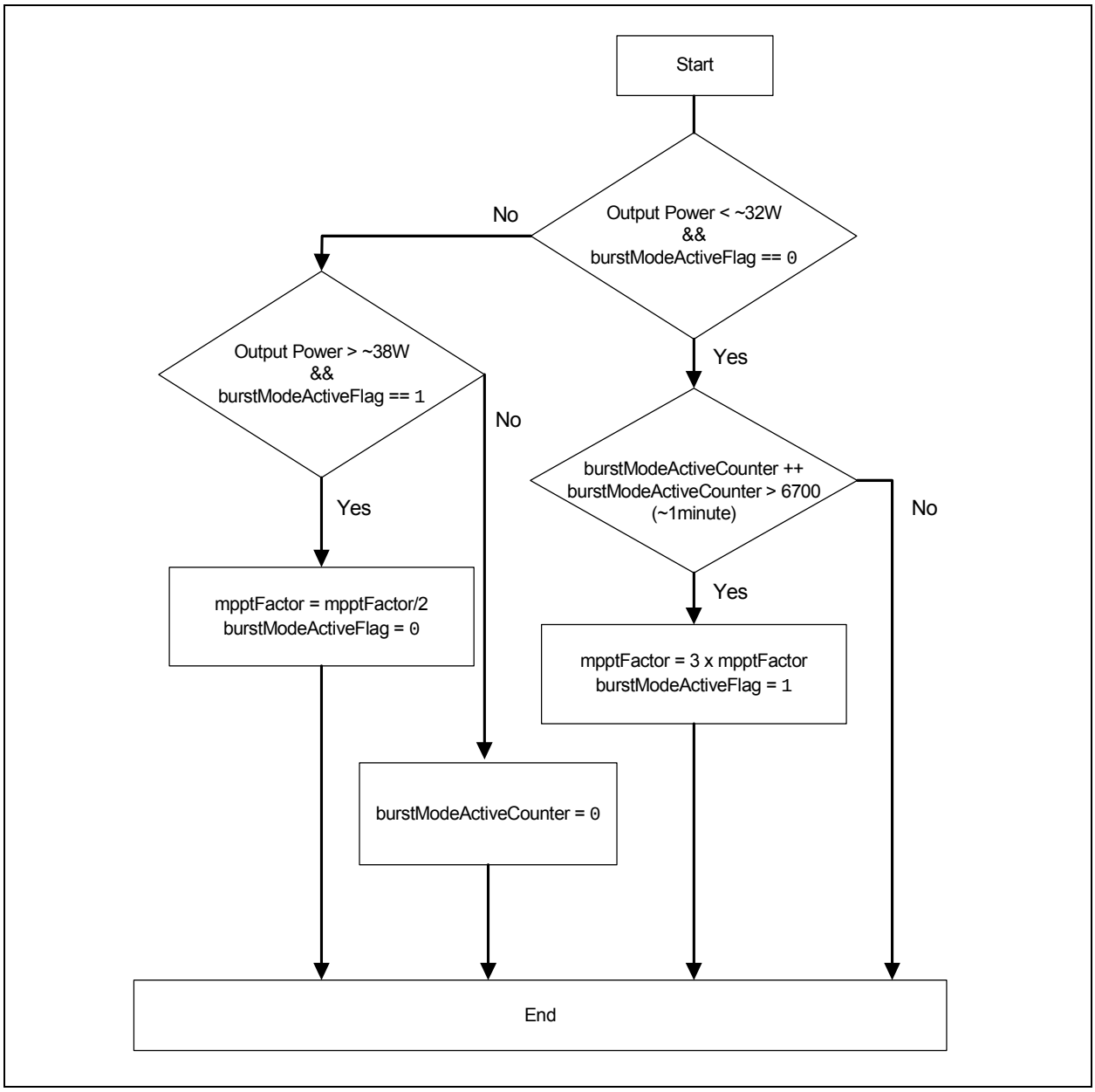
```
deltaAngle = _builtin_divsd((long))32767,inverterPeriod);
```

BURST MODE

To improve efficiency at light loads, a Burst mode feature has been implemented in the software. When the system is operating below 15% of the rated output power for more than a minute, Burst mode is enabled. When in Burst mode, the system will deliver three times the maximum power in one full AC cycle and then shuts down for two full AC cycles. During the off cycles, the bulk capacitors are recharged and will be able to provide enough energy to the load for the next burst cycle. During this time, the Maximum Power Point tracker is still harvesting the maximum power from the PV panel, but instead of being delivered over three AC cycles, the power is delivered over one AC cycle. With this implementation, efficiency at light loads can be increased by up to 15%.

Equation 29 shows the software flowchart for Burst mode implementation. Hysteresis has been added for entering/exiting from Burst mode.

FIGURE 29: BURST MODE DIAGRAM

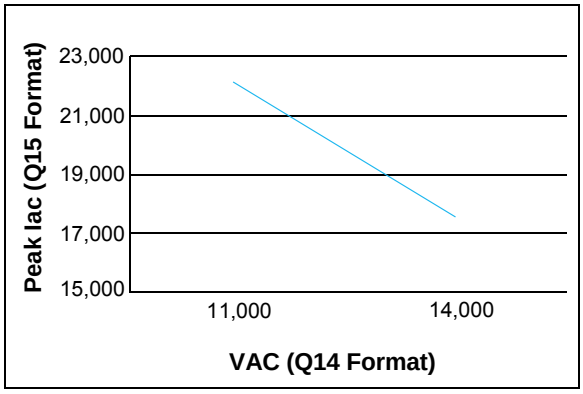


POWER DERATING AND OUTPUT POWER CLAMP

The solar microinverter is designed to support 215W output power at nominal input voltages (25 VDC-45 VDC). To ensure that the microinverter does not operate at an output power greater than 215W, a software clamp on the maximum allowable output current has been designed, based on the measured peak AC voltage.

If the peak inverter output current (`mpptFactorMaximum`) at minimum/maximum operating voltages (210 VAC and 264 VAC) for a 230V system is calculated, then the maximum peak inverter current can be determined at any operating voltage using the curve in Figure 30.

FIGURE 30: POWER CLAMP CURVE



The peak inverter output current can be determined by Equation 20. We can rearrange Equation 20, convert 1.567 into Q14 format and use the built-in multiply instruction to determine the maximum inverter output current at any given inverter output voltage.

EQUATION 20: PEAK INVERTER OUTPUT CURRENT

$$y = -1.567x + 39530$$

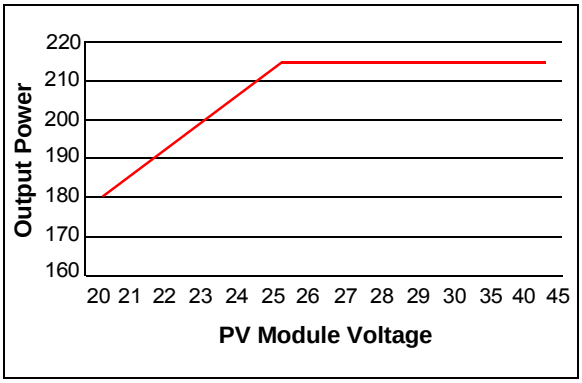
Equation 21 is the software implementation to calculate the peak inverter output current. This is calculated at every AC zero cross.

EQUATION 21: SOFTWARE IMPLEMENTATION

```
y = 39530 – (_builtin_mulss(x, 25673)) >> 14);
```

To prevent saturation of the flyback transformers when the PV module voltage is in the extended operating range (below 25 VDC), a power derating feature has been implemented to clamp the microinverter's output current. This routine derates the output current at a rate of seven watts for every one volt drop on the PV module. Figure 31 shows the output power derating as a function of the input voltage.

FIGURE 31: OUTPUT POWER DERATING



The peak current (in Q15 format), at nominal grid voltage for a power of seven watts, is calculated as shown in Equation 22.

EQUATION 22: PEAK CURRENT

$$I_{pk\_Q15} = \frac{7W * \sqrt{2}}{230\ V_{ac} \cdot 2.14A} \cdot 32767 \approx 650\ counts,\ where\ 2.14A\ is\ the\ base\ current$$

A one volt drop on the PV module (in Q15 format) is calculated as shown in Equation 23.

EQUATION 23: VOLTAGE FEEDBACK AT ONE VOLT

$$V_{pv\_Q15} = \frac{1V}{56.1V} \cdot 32767 = 584\ counts,\ where\ 56.1V\ is\ the\ base\ voltage$$

The derating constant can be calculated as, $I_{pk\_Q15} / V_{pv\_Q15} = 1.113$, which in Q14 format equals 18235. The derating factor can be determined by multiplying the voltage difference (25V – input voltage) by the derating constant, as shown in Equation 24.

EQUATION 24: DERATING FACTOR SOFTWARE IMPLEMENTATION

$$Derating\ Factor = ((\_builtin\_mulss(V_{diff}, 18235)) >> 14);$$

The maximum current reference (`mpptFactorMaximum`) is then subtracted by the derating factor to clamp the output power.

FAULT MANAGEMENT

The dsPIC DSC monitors all major system parameters, such as inverter output voltage/current, PV panel power, reference voltages, ambient temperature and frequency, to name a few. Each parameter is closely monitored, and if any of the measured signals are out of specification, the system will enter into system error. The Fault will be displayed using an LED on the PCB (LED D27). The LED will blink a certain number of times to indicate which Fault has occurred. When the Fault is removed, the system will restart but the LED will continue to blink for approximately one minute. This allows a visual indication of the last known Fault. Table 1 lists all Faults and the corresponding LED counts.

TABLE 1: DEVICE FAULTS

Fault	LED Count	Critical Fault
PV Panel Under/Overvoltage	1	
Inverter Frequency (Over/Under)	2	
VAC Under/Overvoltage	3	
Iac Overcurrent	4	Yes
Flyback Overcurrent (ADC/CMP)	5	Yes
Over Temperature	6	
Drive Supply (Over/Under) Voltage	7	
Flyback Output Voltage (CMP)	8	Yes
2.5V Reference (Over/Under) Voltage	9	
AC Current Offset	10	
Hardware Zero Cross Failure	11	

The software is written in such a way that the first recorded Fault is stored and displayed via the LED. Once that Fault is removed, the system will enter the restart period. In the restart period, if another Fault is detected, the system will enter back into system error.

There are three system Faults that are treated as a critical Fault: flyback overcurrent, inverter overcurrent and flyback overvoltage. If any of these critical Faults occur, the system will try a single restart. If the Fault is still present during the restart process, the system will shut down and a power-down cycle will be required to restart the system. If the system starts up without detecting a critical Fault, the system resumes as normal.

Flyback overcurrent protection and overvoltage protection utilize the on-chip analog comparators. In the event the flyback overcurrent Fault occurs, the PWM will be latched (disables PWM) in approximately 20 ns. This should protect the flyback converter and prevent any hardware failures. The comparator interrupt will also be generated to indicate the Fault occurred and to set the critical Fault flag. If the flyback overvoltage Fault occurs, the analog comparator interrupt is generated, the PWM outputs will be disabled using the PWM override feature and the critical Fault flag will be set. The comparator interrupts have the highest priority in software to ensure that the PWMs are disabled in a timely manner.

DEVICE RESOURCES

Table 2 summarizes the device resources. Table 2 indicates that the dsPIC33FJ16GS504 is very well utilized, from the program memory, to the device peripherals, to the MIPS usage. There are 8 device pins consisting of general purpose I/O, output compare and ADC that are currently not used, but have been routed to a 12-pin header for supporting PLM or wireless communication.

MIPS usage is approximated and is mostly restricted by the ADC Interrupt Service Routine. This routine is called every 17.8 µs with a nominal interrupt time of ~12 µs or 65% MIPS usage. The state machine interrupt is the second most called function, at a rate of 100 µs. These two routines make up a majority of the 30 MIPS used as all other routines are called at a much slower rate (i.e., every zero cross or every third AC cycle).

TABLE 2: DEVICE RESOURCES

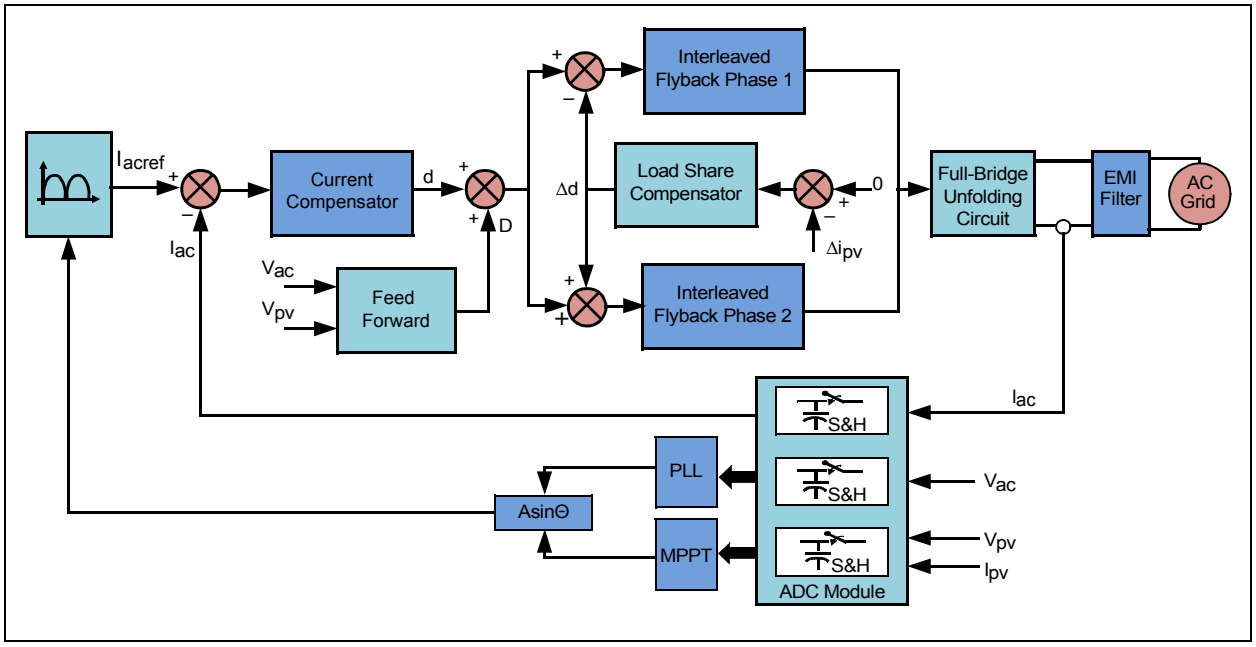
Description	Device Resource
Program Memory (w/o compiler optimizations)	9117 bytes (56%)
Data Memory	242 bytes (11%)
MIPS Usage	30 MIPS (75%)
PWM Module (3 – Pairs)	PWM1H/L – Active Clamp Flyback Phase 1 PWM2H/L – Active Clamp Flyback Phase 2 PWM3H/L – Full-Bridge Unfolding Circuit
ADC Module (8 – Channels)	ADCBUF0 – PV Panel Voltage ADCBUF1 – Flyback Phase 1 Current ADCBUF2 – Flyback Phase 2 Current ADCBUF3 – AC Current ADCBUF6 – 2.5V Reference ADCBUF7 – AC Voltage ADCBUF10 – Temperature ADCBUF11 – Drive Supply
Comparator Module (3 – Channels)	CMP2C – Flyback Current Phase 1 CMP3B – Flyback Current Phase 2 CMP4C – Flyback Overvoltage
GPIO	RC0, RC13 – Drive Signals for Optocouplers RC3, RC8, RC12 – LED Drive Signals RC11 – ON/OFF Switch RB15 – Zero Cross Detect
Communication (PLM/Wireless)	8 – GPIO/OC/ADC
Programming/Debugging	PGEC2/PGED2

COMPENSATOR DESIGN

The control structure of the solar microinverter system is shown in Figure 32. This system has a multi-loop control structure. The MPPT serves as the outer power loop, which decides the maximum power that can be extracted from the PV panel at a given solar irradiance and temperature. The MPPT loop, along with the PLL, provide a sinusoidal current reference to the inner current loop. The inner current loop controller regulates the AC current delivered to the grid at near unity power factor. The current loop is fast acting and with a much wider bandwidth than the outer MPPT power loop.

Therefore, for the MPPT loop, the current control loop appears as a unity gain system with zero or minimal phase error. The current loop modulates the converter current into a rectified sine wave output. The MOSFET full-bridge unfolds this rectified current into an alternating current to be delivered to the grid. The current loop bandwidth can be improved through the use of a feed-forward compensator. The steady-state duty cycle can be dynamically computed using the measured PV panel voltage and grid voltage. While the feed-forward compensator supplies the steady-state modulation, the current control loop takes into account the dynamic variations and modulates the controlled current accordingly. The following sections discuss the mathematical modeling of the solar microinverter system to obtain the transfer functions of output to control input and output to disturbance inputs of the system.

FIGURE 32: COMPENSATOR BLOCK DIAGRAM

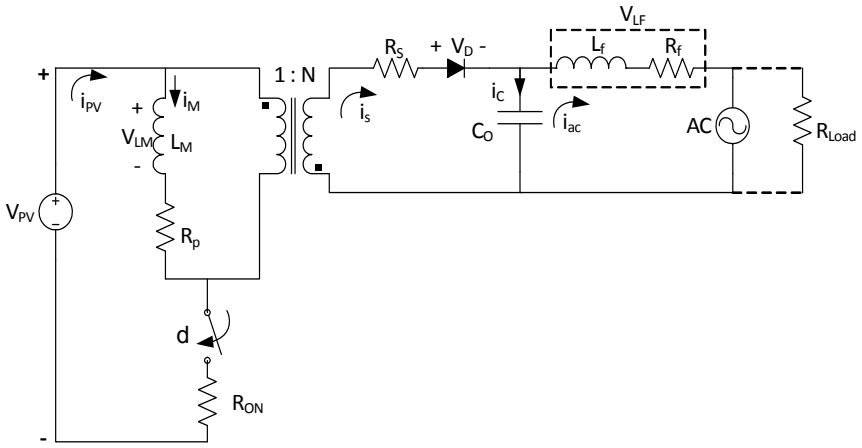


CURRENT LOOP COMPENSATOR DESIGN

The flyback converter is basically an isolated, non-inverting buck-boost converter. The flyback converter, like other power electronic converters, is a highly nonlinear system.

A single non-ideal flyback converter connected to an equivalent grid is shown in Figure 33.

FIGURE 33: NON-IDEAL FLYBACK CONVERTER



The grid voltage is assumed to be a half-wave, rectified voltage with the same RMS value as the AC grid. This assumption is made for simplifying the analysis of the flyback converter.

The flyback converter has the following three states, corresponding to three energy storage elements, that need to be analyzed:

- $I_m(s)$ – Flyback inductor current
- $V_{ac}(s)$ – Flyback output capacitor voltage
- $I_{ac}(s)$ – Output filter inductor current which is fed to the grid

The averaged Kirchhoff's Voltage Law and Current Law (KVL and KCL) equations of the converter over one-switching cycle are shown in Equation 25; where (d) is the duty cycle or modulation signal and (d') is the off-time (1- d).

EQUATION 25: KVL/KCL SYSTEM

$$V_{LM} = L_M \frac{d(i_m)}{dt} = d^* v_{pv} - d^* i_m (R_{on} + R_p) - d' \left(\frac{v_{ac} + i_m R_s}{N} \right)$$

$$i_s = \frac{i_m}{N} d'$$

$$V_{Lf} = V_{ac} - i_{ac} R_f - v_{grid}$$

$$i_c = C_o \frac{d(v_{ac})}{dt} = i_s - i_{ac}$$

$$v_{grid} = R_{load} i_{ac}$$

$$i_{pv} = d^* i_m$$

All the quantities (states and inputs) in Equation 25 are averaged over one switching cycle. The equations included in Equation 25 are large signal and exact (nonlinear) representation of the system. In order to obtain the transfer functions between the system output and the control and disturbance inputs, the system equations are linearized over a chosen operating point. The solar microinverter system has a wide operating voltage and current range, as the output swings from zero to peak, over every quarter-sine wave. Since the converter operates at unity power factor, the Rload is a representation of the grid load and is given by: $Vgridrms/Iacrms$. The operating point is chosen corresponding to the RMS values of the nominal grid voltage and output current at nominal panel peak power voltage. Perturbing all the quantities in Equation 25, the following input, state and output vectors are obtained.

The system state vector is provided in Equation 26 and the system input vector is provided in Equation 27, where d is the control input and $Vgrid$ and Vpv are the disturbance inputs.

EQUATION 26: SYSTEM STATE VECTOR

$$x = [i_m \; i_{ac} \; v_{ac}]^T$$

EQUATION 27: SYSTEM INPUT VECTOR

$$u = [d \; v_{grid} \; v_{pv}]^T$$

As the controlled variable is the output filter current, the output of system is provided by Equation 28:

EQUATION 28: SYSTEM OUTPUT VECTOR

$$y = [i_{ac}]$$

Perturbing and linearizing the state, input and the output vectors, isolating the steady state and the perturbed quantities, we obtain the following equations shown in Equation 29:

EQUATION 29: SYSTEM VECTORS

$$x = X + \tilde{x} = [I_m\ I_{ac}\ v_{ac}] + [\tilde{i_m}\ \tilde{i_{ac}}\ \tilde{v_{ac}}]$$

$$u = U + \tilde{u} = [D\ v_{grid}\ v_{pv}] + [\tilde{d}\ \ \tilde{v_{grid}}\ \tilde{v_{pv}}]$$

$$y = Y + \tilde{y} = I_{ac} + \tilde{i_{ac}}$$

The vectors, X, U and Y represent the quiescent operating point of the system and the vectors, $\tilde{x}$, $\tilde{u}$ and $\tilde{y}$ are the perturbations over the operating point.

Substituting Equation 29 into Equation 25, separating the AC quantities and disregarding the smaller AC terms, the linearized system equations are obtained, as shown in Equation 30.

From Equation 30, the small signal equivalent AC circuit is obtained as shown in Figure 34.

EQUATION 30: LINEARIZED SYSTEM EQUATIONS

$$\tilde{v}_{LM} = L_M\frac{d(\tilde{i}_m)}{dt} = D\tilde{v}_{pv} + \tilde{d}\left(v_{pv} - I_m(R_{on}+R_p) + \frac{I_m}{N}R_s + \frac{v_{ac}}{N}\right) - \left(D(R_{on}+R_p) + D'\frac{R_s}{N}\right)\tilde{i}_m + \frac{D'\tilde{v}_{ac}}{N}$$

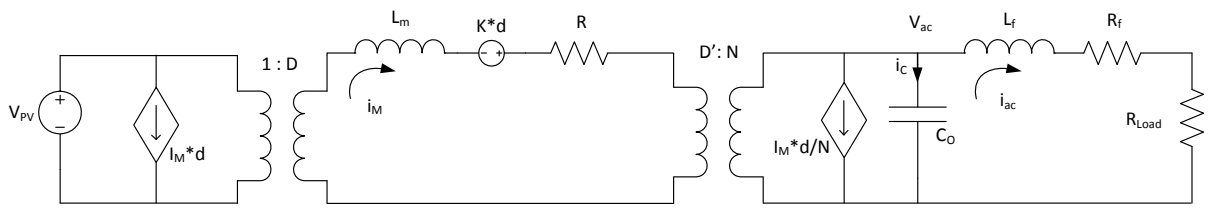
$$\tilde{i}_S = \frac{D'\tilde{i}_m}{N} - \frac{\tilde{d}I_m}{N}$$

$$\tilde{v}_{Lf} = L_f\frac{d(\tilde{i}_{ac})}{dt} = \tilde{v}_{ac} - \tilde{i}_{ac}R_f - \tilde{v}_{grid}$$

$$\tilde{i}_c = C_o\frac{d(\tilde{v}_{ac})}{dt} = \frac{D'}{N}\tilde{i}_m - \frac{I_m}{N}\tilde{d} - \tilde{i}_{ac}$$

$$\tilde{i}_{pv} = D\tilde{i}_m + \tilde{d}I_m$$

FIGURE 34: SMALL SIGNAL AC CIRCUIT



Rewriting Equation 30, the linearized state equations are provided as in Equation 31;

EQUATION 31: SYSTEM STATE EQUATIONS

$$\frac{d(\hat{i}_m)}{dt} = -\frac{R}{L_m}\hat{i}_m + 0\cdot\hat{i}_{ac} - \frac{D'}{L_m N}\hat{v}_{ac} + \frac{k}{L_m}\hat{d} + 0\cdot\hat{v}_{grid} + \frac{D}{L_m}\hat{v}_{pv}$$

$$\frac{d(\hat{i}_{ac})}{dt} = 0\cdot\hat{i}_m - \frac{R_f}{L_f}\hat{i}_{ac} + \frac{1}{Lf}\hat{v}_{ac} + 0\hat{d} - \frac{1}{Lf}\cdot\hat{v}_{grid} + 0\hat{v}_{pv}$$

$$\frac{d(\hat{v}_{ac})}{dt} = \frac{D'}{NC_o}i_m - \frac{1}{C_o}\hat{i}_{ac} + 0\cdot\hat{v}_{ac} - \frac{I_m}{NC_o}\hat{d} + 0\cdot\hat{v}_{grid} + 0\cdot\hat{v}_{pv}$$

$$\text{Where, } k = \left(\hat{v}_{pv} - I_m(R_{on}+R_p) + \frac{I_m}{N}R_s + \frac{\hat{v}_{ac}}{N}\right)$$

$$R = D(R_{on}+R_p) + D'\frac{R_s}{N}$$

and the output equation is provided in Equation 32;

EQUATION 32: OUTPUT STATE EQUATION

$$y = \hat{i_{ac}}$$

writing Equation 31 and Equation 32 in state matrix form.

$$\begin{bmatrix}\dot{\hat{i}}_m\\ \dot{\hat{i}}_{ac}\\ \dot{\hat{v}}_{ac}\end{bmatrix} = \begin{bmatrix}-\frac{R}{L_m} & 0 & -\frac{D'}{L_m N}\\ 0 & -\frac{R_f}{L_f} & \frac{1}{L_f}\\ \frac{D'}{NC_o} & -\frac{1}{C_o} & 0\end{bmatrix}\begin{bmatrix}\hat{i}_m\\ \hat{i}_{ac}\\ \hat{v}_{ac}\end{bmatrix} + \begin{bmatrix}\frac{k}{L_m}\\ 0\\ -\frac{I_m}{NC_o}\end{bmatrix}\hat{d} + \begin{bmatrix}\frac{D}{L_m}\\ 0\\ 0\end{bmatrix}\hat{v}_{pv} + \begin{bmatrix}0\\ -\frac{1}{L_f}\\ 0\end{bmatrix}\hat{v}_{grid}$$

$$\dot{X} = [A]X + [B_1]U_1 + [B_2]U_2 + [B_3]U_3$$

$$\hat{i}_{ac} = \begin{bmatrix}0 & 1 & 0\end{bmatrix}\begin{bmatrix}\hat{i}_m\\ \hat{i}_{ac}\\ \hat{v}_{ac}\end{bmatrix}$$

$$Y = [C]X$$

The relationship between the output and the control input (forcing all the other disturbances to zero) is provided in Equation 33.

EQUATION 33: RELATIONSHIP BETWEEN OUTPUT AND CONTROL INPUT

$$\frac{Y(s)}{U1(s)} = C(sI-A)^{-1}B1 \quad \text{where, } U2(s) = U3(s) = 0$$

Using Equation 33, the transfer function is obtained between the output AC current and modulation input, as shown in Equation 34

EQUATION 34: TRANSFER FUNCTION (Iac vs. MODULATION INPUT)

$$G_{id}(s) = \frac{\left(\frac{kD' - I_m R}{L_m N L_f C_o} - \frac{I_m s}{L_m c_o N}\right)}{S^3 + \left(\frac{R}{L_m} + \frac{R_f}{L_f}\right)S^2 + \left(\frac{RR_f}{L_m Lf} + \frac{1}{L_f C_o} + \frac{D'^2}{N^2 L_m Co}\right)s + \left(\frac{R}{L_m L_f C_o} + \frac{R_f \cdot D'^2}{N^2 L_m C_o}\right)}$$

From Equation 34, the output to control transfer function has a right half zero transfer function, which is typical of boost and buck-boost topologies. The open-loop bode plot of the system is shown in Figure 35.

In order to obtain the bode plot, the grid voltage has been replaced by an equivalent resistive load with the chosen operating point. The load resistance has been included in the term, *Rf*, as the filter inductor DCR is in series with the load resistance in the AC-equivalent circuit. From the open-loop bode plot, it can be observed that both gain margin and phase margin of the system are low, thus, the system inherently has a poor relative stability. Additionally, it is also observed that the switching frequency ripple attenuation needs improvement and that the system gain at the required operating frequency (100/120 Hz) is very low.

Therefore, the control objectives are defined as follows:

- Gain Margin ≥ 10 dB
- Phase Margin ≥ 45 deg.
- Gain at Operating Frequency ~15 dB
- Bandwidth ~1/10th Sampling Frequency
- Switching Frequency Attenuation ≤ -40 dB

The sampling frequency and the control loop execution rate of the system are equal to the switching frequency, which is 57 kHz. A PI compensator was chosen to obtain the required stability margins, gain and bandwidth. Figure 36 shows the bode plot of the system, which is provided in Equation 35.

EQUATION 35: SYSTEM TRANSFER FUNCTION

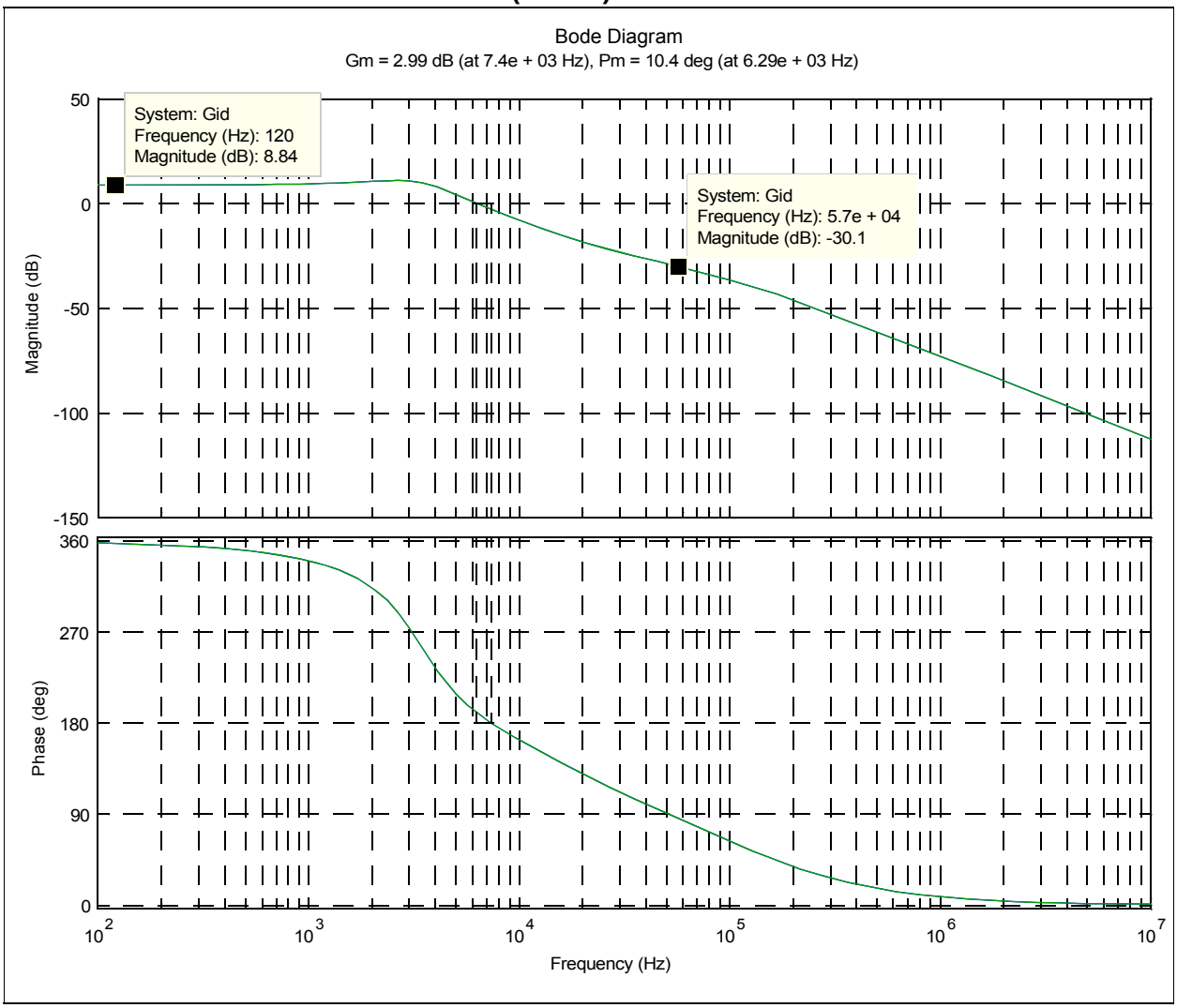
$$OLTF = Gid(s) \times Gc(s) \times H(s)$$

Where *Gid(s)* is given by Equation 34, *H(s)* is the transfer function of the hardware current sensor filter and *Gc(s)* is the PI compensator transfer function, provided in Equation 36.

EQUATION 36: PI COMPENSATOR TRANSFER FUNCTION

$$Gc(s) = Gco * (1 + \omega c/s)$$

FIGURE 35: OPEN-LOOP BODE PLOT (PLANT)



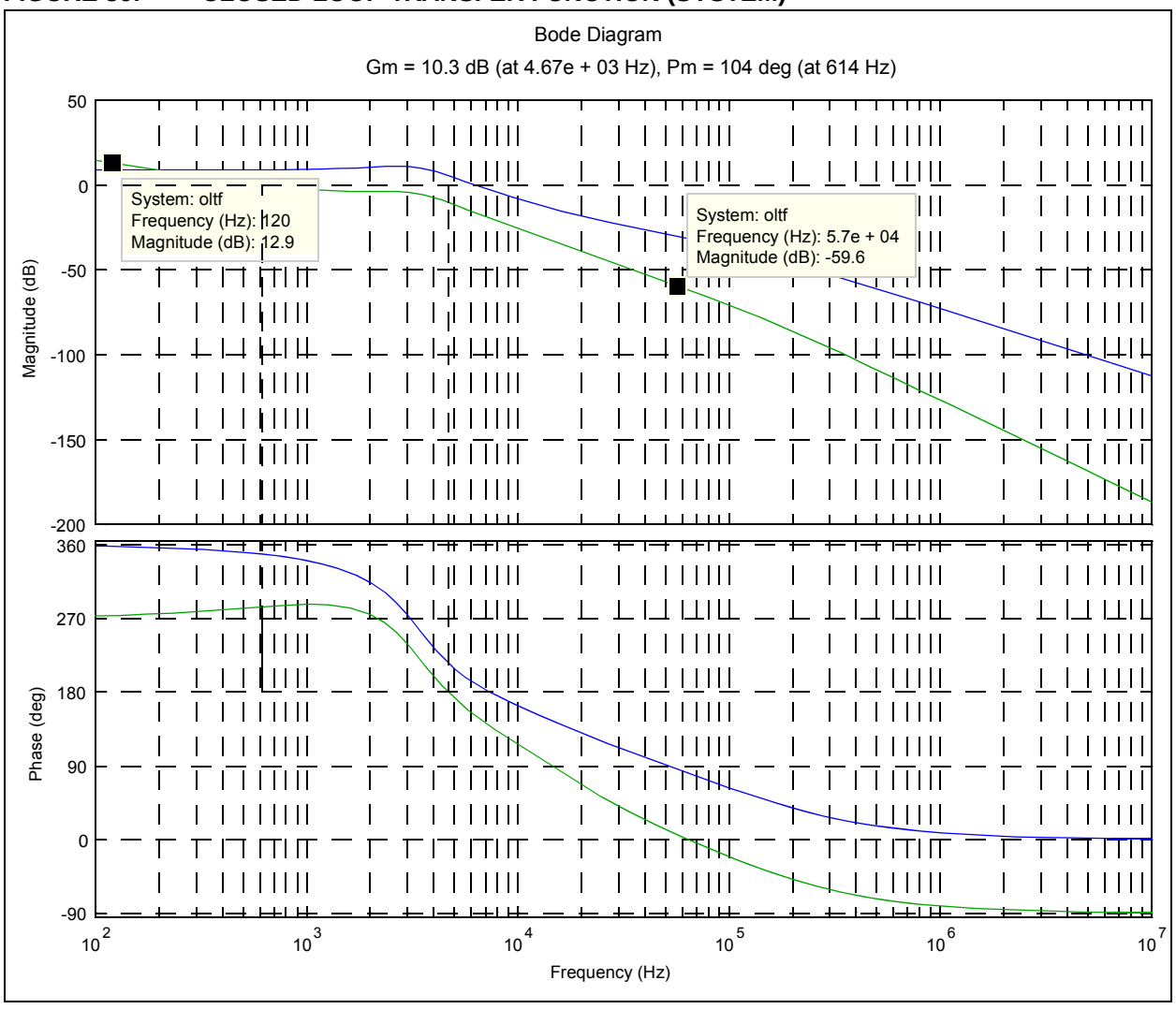
Where Gco is the steady-state gain of the PI compensator and ωc is the corner frequency of the PI compensator, Equation 36 can be resolved to the proportional and integral components, as shown in Equation 37.

EQUATION 37: PI COMPENSATOR

$$Gc(s) = Kp + Ki/s$$

Figure 36 shows that the compensator has achieved sufficient stability margins, along with steady-state gain and switching frequency attenuation.

FIGURE 36: CLOSED LOOP TRANSFER FUNCTION (SYSTEM)



FEED-FORWARD COMPENSATOR DESIGN

A combined feed-forward and feedback system can improve the performance of the control system to a large extent, whenever there is a major measurable disturbance. In an ideal situation, the feed-forward compensator will completely reject the measured disturbance signal better than the compensator acting alone. The role of the feed-forward compensator in the solar microinverter system is to provide the steady-state duty ratio, "$D(t)$", to the system, thereby allowing the compensator to provide only the "$\Delta d(t)$" for tracking the dynamic current reference. The feed-forward network will help the compensator to reject the disturbances caused by fluctuations in both the input voltage (PV panel voltage), and the output voltage (AC grid voltage). The relationship between the input voltage and the output voltage for a flyback converter is provided in Equation 38.

EQUATION 38: VOLTAGE CONVERSION RATIO

$$V_o = \frac{N \cdot D}{1 - D} V_{in}$$

By rewriting Equation 38, we obtain the following expression for the steady-state duty cycle (D) in Equation 39.

EQUATION 39: STEADY-STATE DUTY CYCLE

$$D = \frac{V_o}{V_o + V_{in} N}$$

The feed-forward compensator is nothing but the software implementation of Equation 39, that represents the steady-state input/output voltage relationship, and this will be added to the output of the compensator. The compensator will be a correction factor to this, D, for achieving the dynamic current reference, as shown in Figure 32. The final duty ratio, without considering the load sharing compensator, is provided in Equation 40.

EQUATION 40: FINAL DUTY CYCLE

$$d(t) = D(t) + \Delta d(t)$$

Where, $D(t)$, is the contribution from the feed-forward compensator and $\Delta d(t)$ is contribution from the AC current control compensator.

LOAD SHARING COMPENSATOR DESIGN

As explained in the earlier sections, the solar microinverter system is comprised of two interleaved flyback converters connected in Input Parallel Output Parallel (IPOP) configuration, thereby, sharing the load current. Any two practical converters, although the same by design, are bound to have parameter variations. Parameter variations could be observed in the parasitic elements, like primary and secondary resistances, diode voltage drops, Rdson, core losses, etc. Such parameter variations could cause one of the converters to be overloaded, thus leading to lower efficiency and degradation of reliability. In the worst-case, imbalances could also lead to situations of thermal runaway of the overloaded converter. Therefore, it becomes very important to incorporate a load sharing compensator, which would ensure equal sharing of the injected current.

The load sharing control loop constantly monitors the error between the input currents of the converters and will minimize this error. It does so by dynamically adjusting the duty ratio of each of the converters by the addition/subtraction of a small common correction factor depending on the sign of the error.

The transfer function between the current error ($\Delta I(s)$) and the correction modulation factor $\Delta d(s)$ is obtained as follows in Equation 41.

EQUATION 41: LOAD SHARING TRANSFER FUNCTION

$$Ipv1(s) = Gd, ipv1(s)Xd(s)$$

$$Ipv2(s) = Gd, ipv2(s)\ X\ d(s)$$

Let the error between the currents be equal to ΔI. Therefore, the currents can be seen as follows in Equation 42.

EQUATION 42: LOAD SHARING CURRENT ERROR

$$Ipv1(s) = Ipv2(s) = \Delta I = (Gd, ipv1(s) - Gd, ipv2(s))\ X\ d(s)$$

The goal is to make both the currents the same (i.e., make $Ipv1$ as $Ipv1(s) - \Delta I/2$ and $Ipv2$ as $Ipv2(s) + \Delta I/2$) by including correction factors of $\pm\Delta d$.

Rewriting Equation 41 with the correction factors provides the following in Equation 43.

EQUATION 43: LOAD SHARING CORRECTION FACTOR

$$Ipv1(s) - \Delta I/2 = Gd,ipv1(s)\ X\ (d(s) - \Delta d(s))$$

$$Ipv2(s) + \Delta I/2 = Gd,ipv2(s)\ X\ (d(s) + \Delta d(s))$$

Subtracting the second equation from the first equation, in Equation 43, provides the following result in Equation 44.

EQUATION 44: LOAD SHARING CURRENT

$$\Delta I = (Gd,ipv2\text{-}Gd,ipv1)d(s) + (Gd,\ ipv2 + Gd,\ ipv1)\Delta d(s))$$

Assuming $Gdipv2 \approx Gdipv1 \approx Gdipv$

$$\Delta I(s) = 2Gdipv(s)\ \Delta d(s)$$

The transfer function between i_{pv} and d can be obtained by modifying the system output in Equation 32 to y = i_{pv}, where i_{pv} is given in Equation 30, and applying Equation 33.

Simulink Model

A simulation of the mathematical model of the interleaved flyback microinverter system, using Simulink® MATLAB®, is available in both digital and the equivalent analog implementations. This section describes the digital implementation of the system simulation in Simulink. Figure 37 shows the overall block diagram of the simulation.

The model implements the exact nonlinear differential equations, considering the actual measured non idealities of the plant, thereby accurately representing the actual system. All the functionalities of the system, including interleaved operation, load sharing controller, feed-forward compensator, sensor transfer functions and software normalization operations, have been incorporated in the model.

FIGURE 37: SIMULINK® BLOCK DIAGRAM

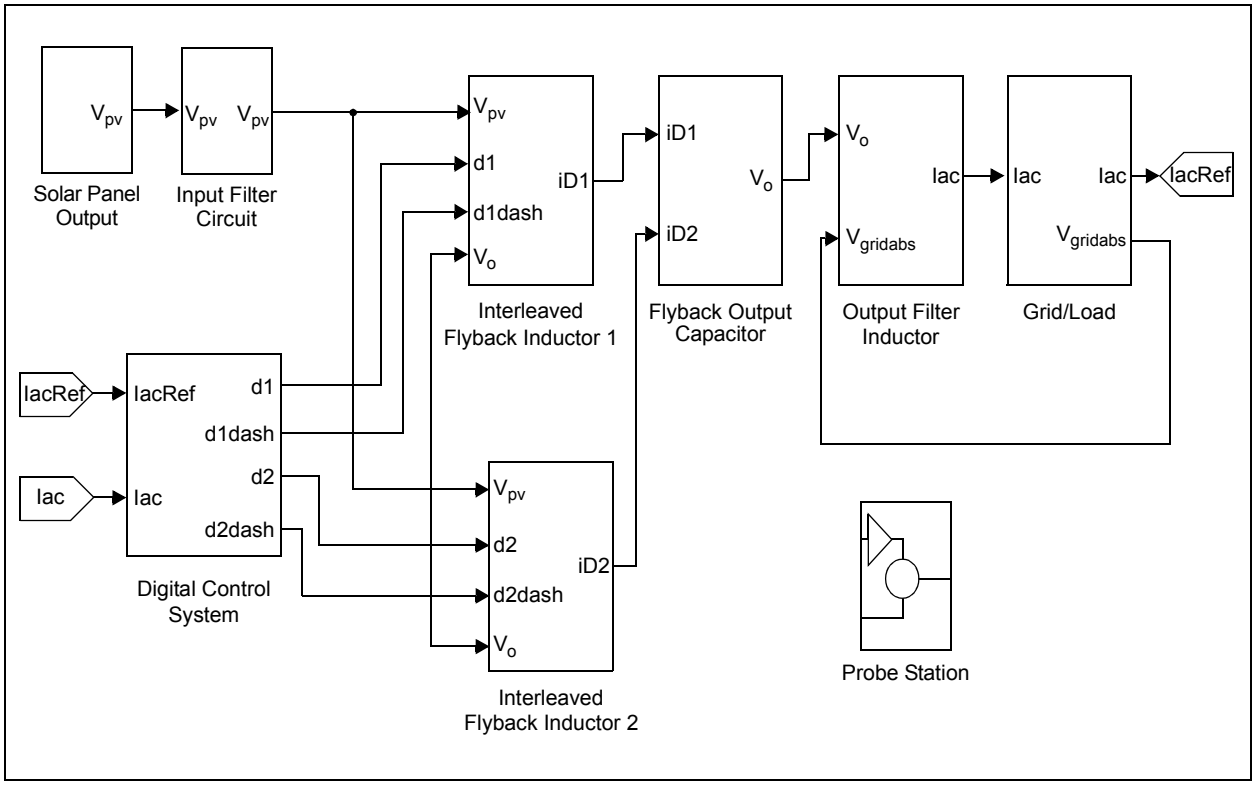


Figure 38, Figure 39, Figure 40 and Figure 41 show the Simulink implementations of a digital PI controller (with feed-forward compensator and load sharing compensator), flyback inductor model, output capacitor model and the output filter inductor model, respectively.

FIGURE 38: DIGITAL PI CONTROLLER

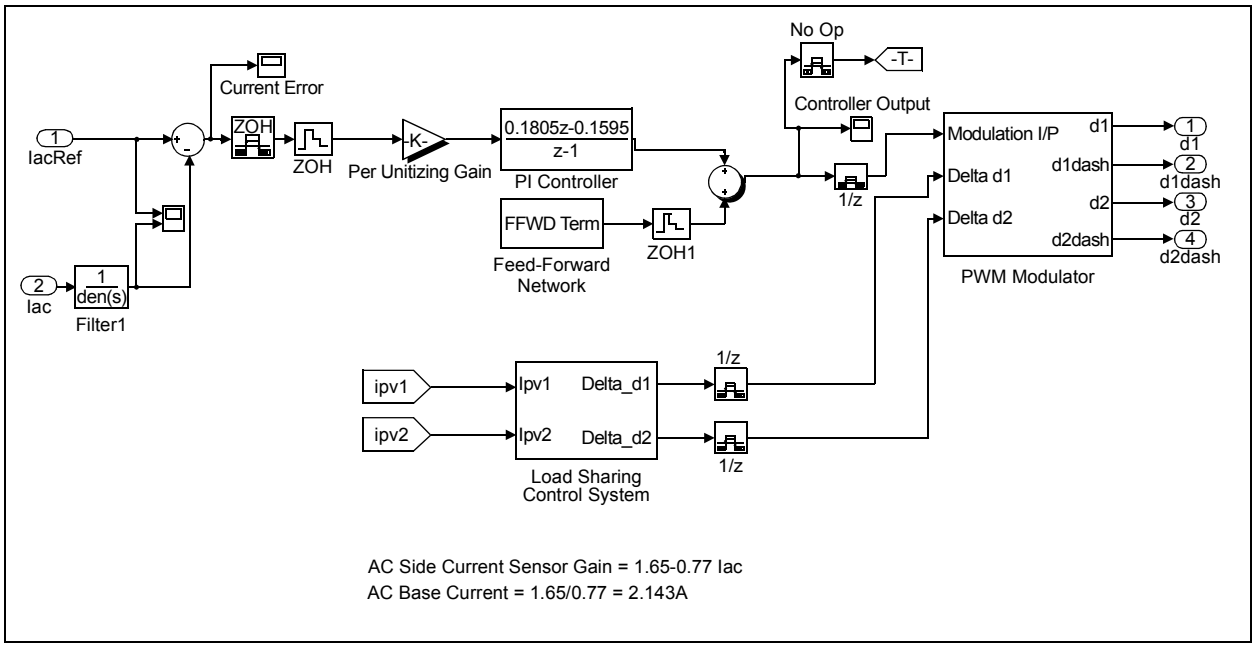


FIGURE 39: FLYBACK INDUCTOR MODEL

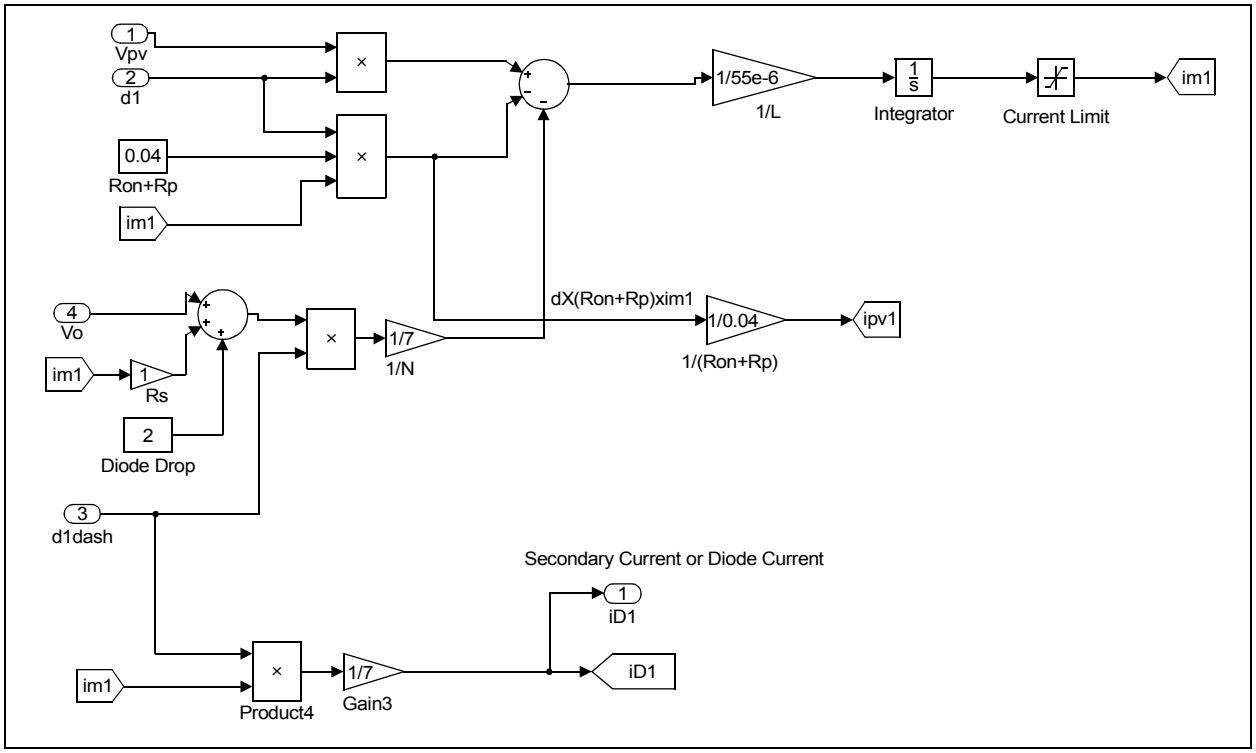


FIGURE 40: FLYBACK OUTPUT CAPACITOR MODEL

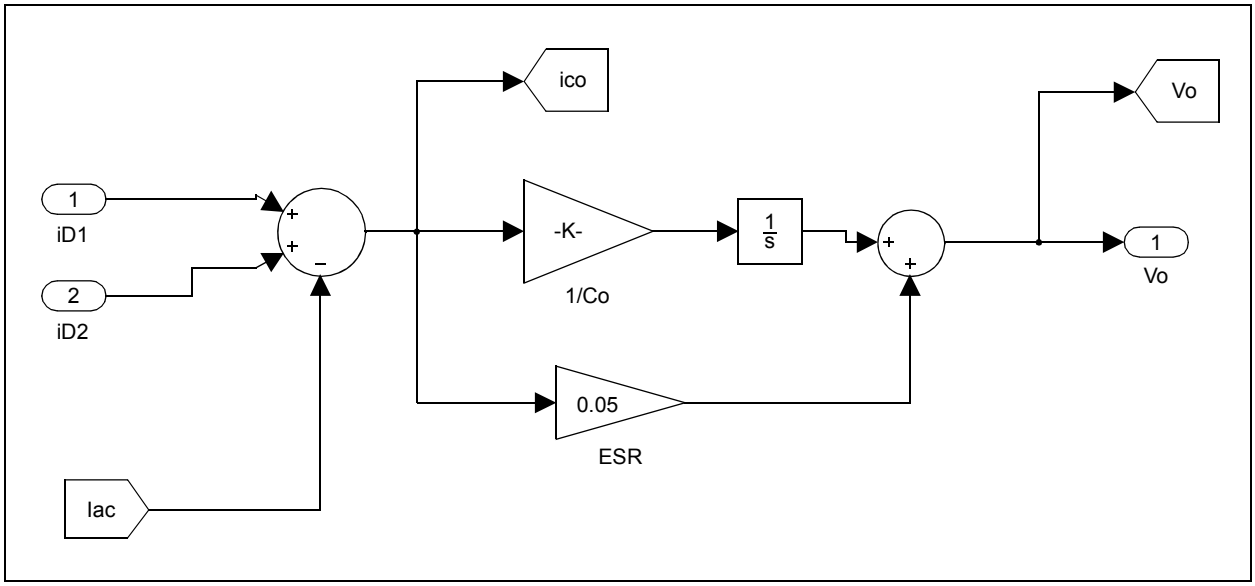
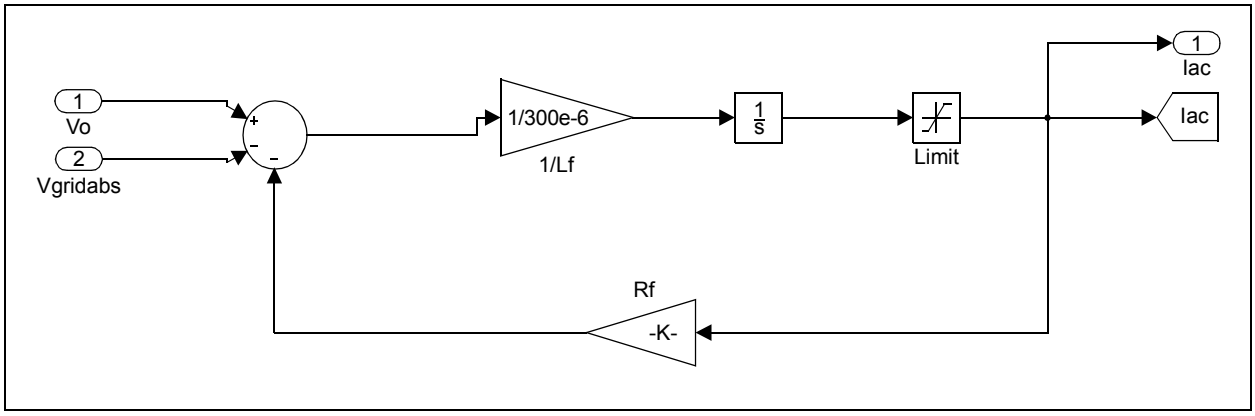


FIGURE 41: OUTPUT CURRENT FILTER MODEL



REFERENCES

Design and Control of an Inverter for Photovoltaic Applications
http://vbn.aau.dk/files/36989298/soeren_baekhoej_kjaer.pdf

Reliability Study of Electrolytic Capacitors in a Micro-Inverter
http://enphase.com/downloads/ElectolyticCapacitorLife092908.pdf

Reliability of CDE Aluminum Electrolytic Capacitors
http://www.cde.com/tech/reliability.pdf

S. B. Kjaer, J.K. Pedersen, F. Blaabjerg *"A Review of Single-Phase Grid-Connected Inverters for Photovoltaic Modules*", IEEE Trans. Ind. Appl., vol. 41, no 5, pp. 1292-1306, Oct. 2005.

Bower W, Ropp M. *"Evaluation of Islanding Detection Methods for Photovoltaic Utility-Interactive Power Systems",* IEA Report IEA Photovoltaic Power Systems Program T5-09: 2002, 2002.

APPENDIX A: DESIGN PACKAGE

A complete design package for this reference design is available as an executable installer. This design package can be downloaded from the Microchip corporate web site at: www.microchip.com

Design Package Contents

The design package contains the following items:

- Reference Design Schematics
- Bill of Materials
- Hardware Design Gerber Files
- Source Code
- Hardware Design Layout Files
- Demonstration Instructions
- MATLAB® Models

APPENDIX B: ELECTRICAL SPECIFICATION AND OPERATIONAL WAVEFORMS

This appendix provides information on the test results for the 215W Solar Microinverter Reference Design, as well as a few operating waveforms.

B.1 Electrical Specifications

Table B-1 lists the electrical specifications for the Solar Microinverter Reference Design. Figure B-1 and Figure B-2 show the 230 VAC system performance for efficiency, and total demand distortion across output power.

TABLE B-1: SOLAR MICROINVERTER ELECTRICAL SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units	Comments
VPV	PV Panel Input Voltage	20	36	53	VDC	
VMPP	Maximum Power Point Voltage	25	—	45	VDC	215W output power
	Maximum Power Point Voltage	20	—	25	VDC	Reduced output power
VOUT	Output Voltage (230 VAC)	210	230	264	VAC	
	Output Voltage (120 VAC)	90	120	140	VAC	
FOUT	Output Frequency (60 Hz)	59.3	60	60.7	Hz	
	Output Frequency (50 Hz)	47	50	53	Hz	
POUT	Maximum Output Power	180	—	215	W	Depends on V_{pv}
PMPP	PV Panel Power	—	—	250	W	
TDD	Total Demand Distortion	—	—	4	%	
PF	Output Power Factor	0.98	—	0.998	—	System not in Burst mode
η	System Efficiency	—	94	94.8	%	230 VAC System
MPPT	Maximum Power Point Tracking	—	99.5	—	%	

FIGURE B-1: EFFICIENCY

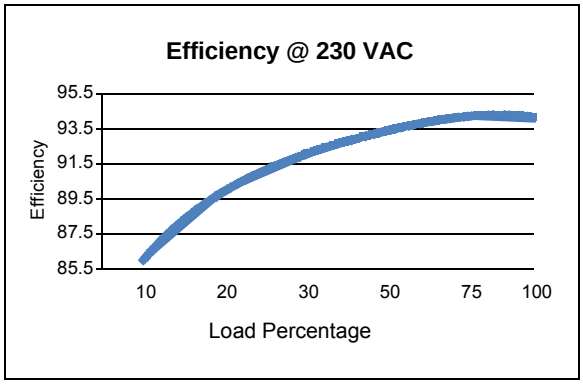
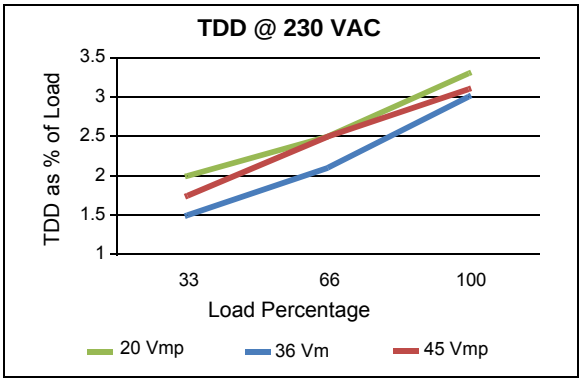


FIGURE B-2: TOTAL DEMAND DISTORTION



B.2 Operational Waveforms

Figure B-3 and Figure B-4 show the output current (yellow) and grid voltage (blue) of a 230 VAC system when operating at maximum output power and at 30 percent output power.

FIGURE B-3: OUTPUT VOLTAGE AND OUTPUT CURRENT – MAXIMUM POWER

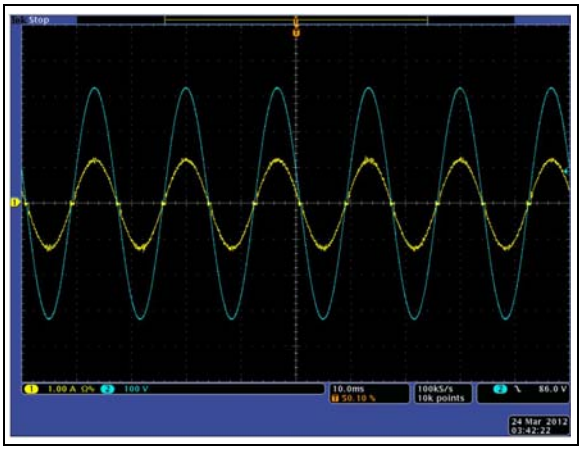


FIGURE B-4: OUTPUT VOLTAGE AND OUTPUT CURRENT – ~30% POWER

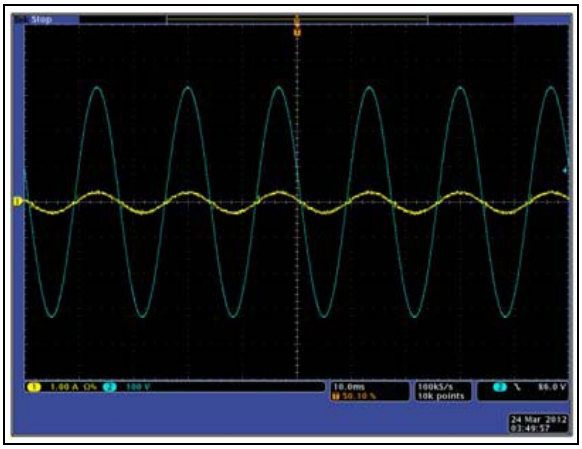
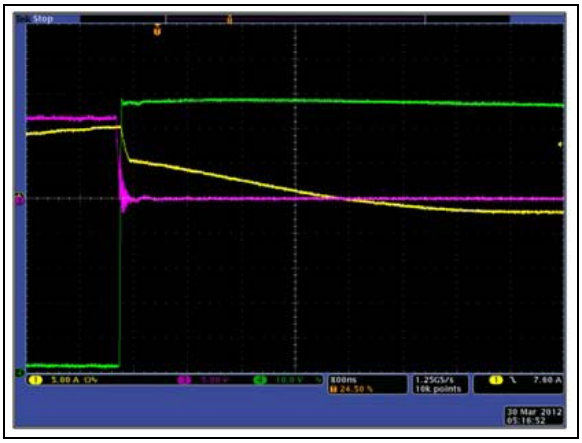


Figure B-5 shows the active clamp waveform for a single flyback phase.

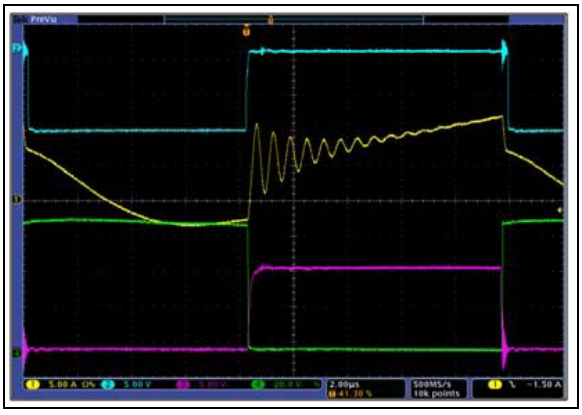
FIGURE B-5: ACTIVE CLAMP WAVEFORM



When the gate drive (violet) of the flyback MOSFET is disabled, the inductor current (yellow) charges the MOSFET output capacitor. This causes the drain-to-source voltage (green) to rise ($VPV + Vout/n$). When the drain-to-source voltage is greater than the voltage across the clamping capacitor, the voltage rise is clamped by the clamp capacitors. The leakage current now forward biases the body diode of the clamp MOSFET and will begin to resonate with the clamp capacitors.

Figure B-6 shows the resonant current waveform and ZVS for a single flyback phase.

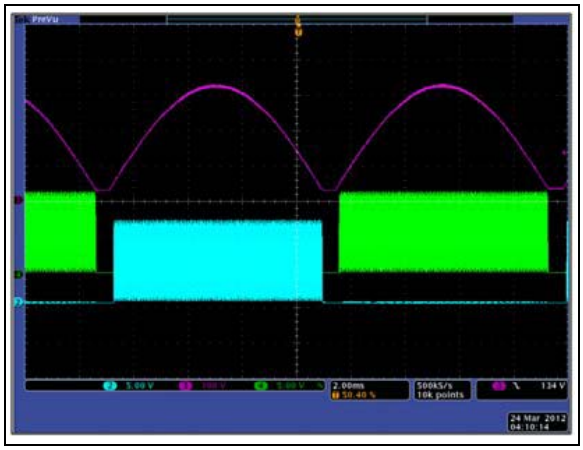
FIGURE B-6: ZVS WAVEFORM



When the gate drive of the active clamp MOSFET is disabled (blue), the inductor current (yellow) is negative and begins to flow through the flyback MOSFET body diode. The drain-to-source voltage of the flyback MOSFET begins to discharge (green). After the drain voltage is zero, the flyback MOSFET is enabled (violet).

Figure B-7 shows the gate drive waveforms for the full-bridge unfolding circuit.

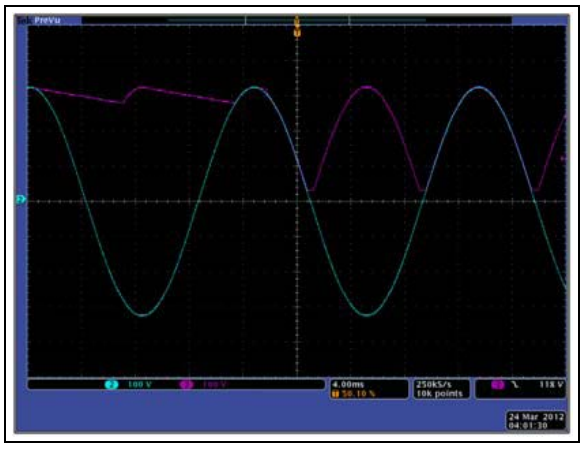
FIGURE B-7: UNFOLDING GATE DRIVE WAVEFORM



The MOSFET drive signals (blue, green) are driven every other AC half cycle. The flyback output voltage (violet) is seen as a 100/120 Hz rectified signal.

Figure B-8 shows the point at which the full-bridge unfolding circuit is enabled.

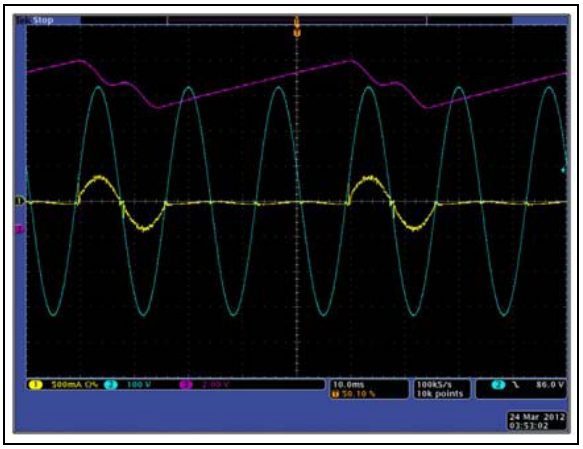
FIGURE B-8: FULL-BRIDGE START-UP WAVEFORM



When AC voltage is applied, and before enabling the full-bridge unfolding circuit, the output voltage of the flyback (violet) will be DC due to the body diodes of the MOSFETs. To eliminate large spikes, the full-bridge circuit is enabled at the peak of the AC voltage (blue).

Figure B-9 shows the waveform of the output current (yellow) and PV panel voltage (violet) when the system enters Burst mode.

FIGURE B-9: BURST MODE WAVEFORM



When operating in Burst mode three times, the energy is pushed during one AC cycle and the other two AC cycles are used to recharge the bulk capacitors.

APPENDIX C: 120 VAC HARDWARE CHANGES

This appendix highlights all hardware changes made between the 230 VAC system and a 120 VAC system. There are four major areas that have changed:

- Flyback Transformer
- Inverter AC Current Sense
- Inverter AC Voltage Sense
- Flyback Overvoltage Protection

C.1 Flyback Transformer Design

The 120 VAC flyback transformer design has similar design specifications as the 230 VAC transformer, except for a couple of changes:

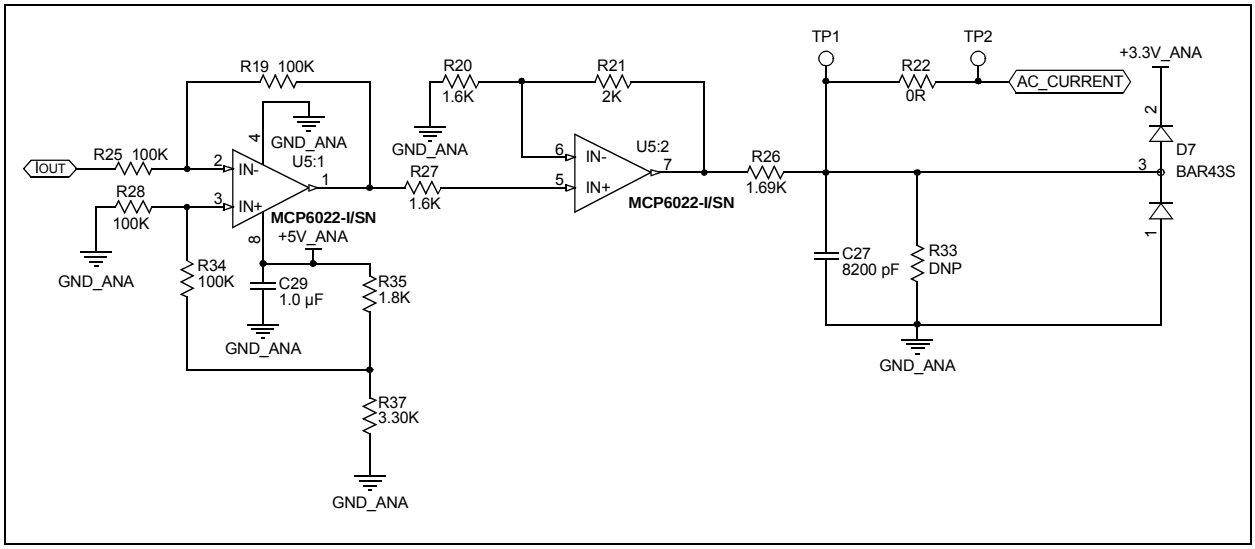
- Maximum Output Voltage: 200V
- Secondary Current: 2.4 Arms

The primary winding structure of the flyback transformer and core gap remains unchanged. As the rectified output voltage has reduced, the transformer turns ratio has reduced to four; this will keep the operating duty cycle range in that of a 230 VAC system. For the same output power and a lower operating voltage, the output current has now increased, so two more bundles of Litz wire has been added in parallel to the secondary winding.

C.2 Inverter Output Current Sense Circuit

Figure C-1 shows the AC current sense schematic for the 120 VAC systems. The base current for the AC current sense can be calculated by Equation C-1 and is approximately 3.9A.

FIGURE C-1: INVERTER AC CURRENT SENSE



EQUATION C-1: CURRENT SENSE CIRCUIT GAIN

$$V_{ADC} = \left[2 \cdot \left[5 \cdot \left(\frac{R37}{R37 + R35}\right) \cdot \left(\frac{R28}{R28 + R34}\right)\right] - V_{U14}\right] \cdot \left(1 + \frac{R21}{R20}\right)$$

C.3 Flyback Output Overvoltage Protection Circuit

The flyback overvoltage protection circuit for the 120 VAC systems is shown in Figure C-2. Resistors, R99, R101 and R105, were changed to keep the LED drive current the same as the 230 VAC system. Resistor, R106, was changed to give 2.5V at the reference pin when the peak inverter voltage is 210V.

C.4 Inverter Output Voltage Sense Circuit

Figure C-3, shows the AC voltage sense schematic for the 120 VAC systems. The base voltage for the AC current sense can be calculated by Equation C-4 and is approximately 247V.

FIGURE C-2: FLYBACK OVERVOLTAGE PROTECTION

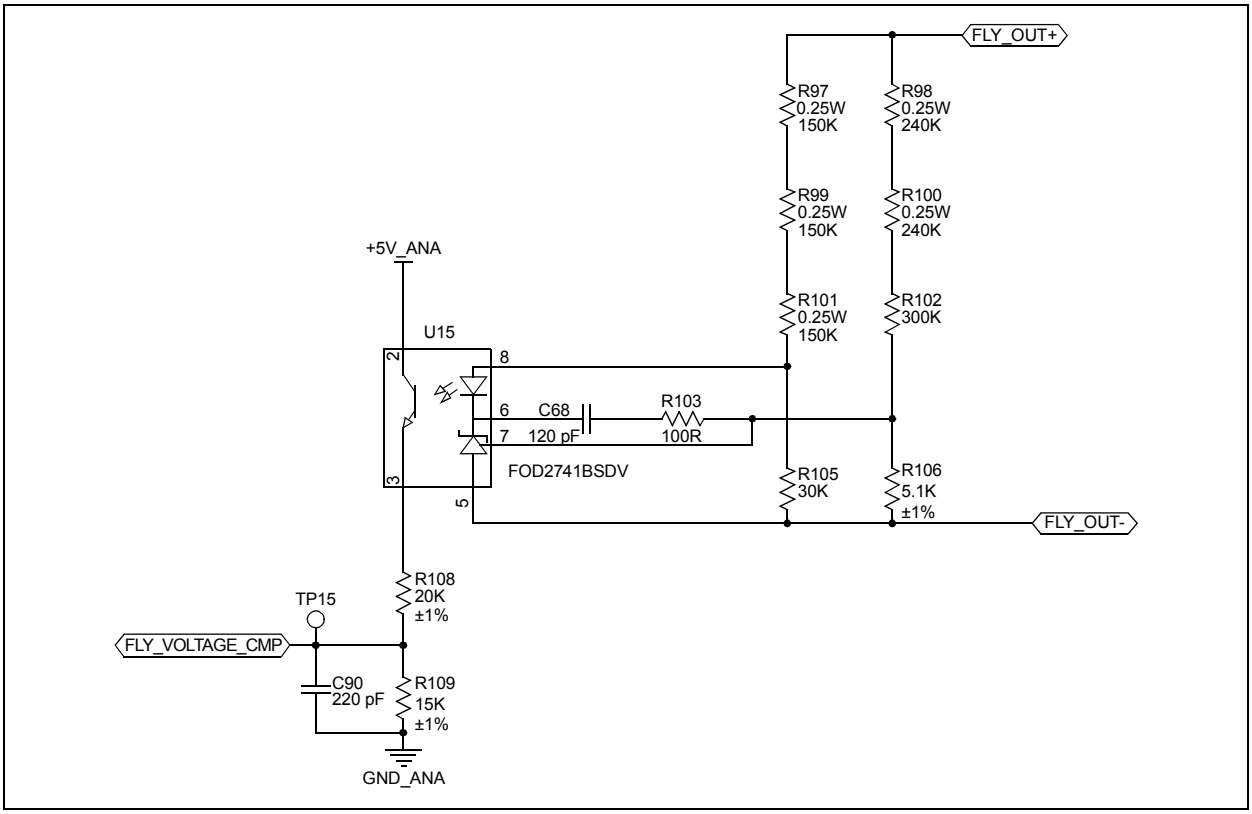
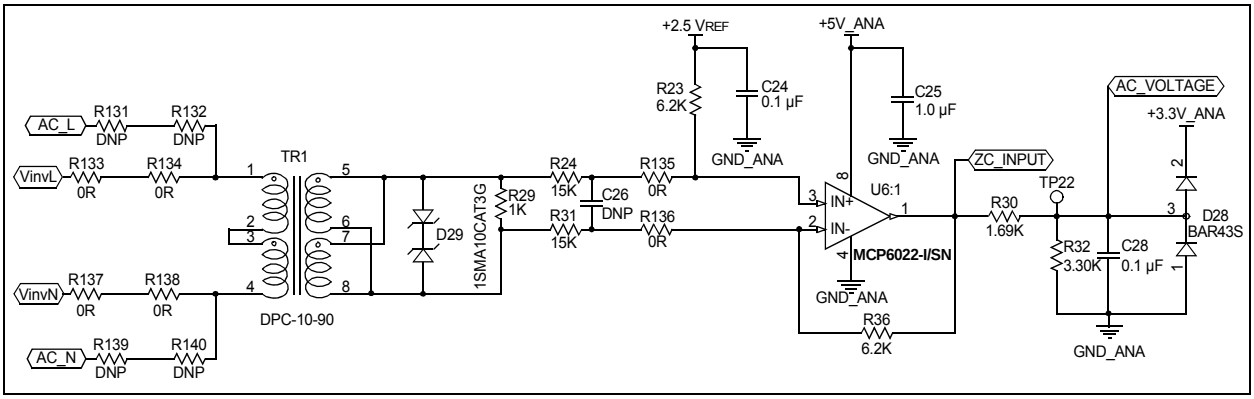


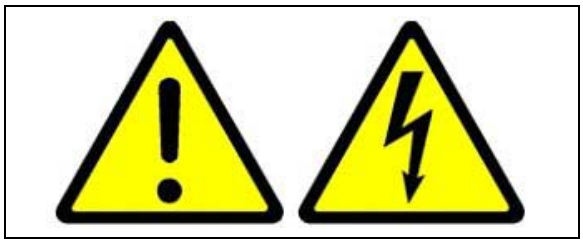
FIGURE C-3: INVERTER AC VOLTAGE SENSE



EQUATION C-4: VOLTAGE SENSE CIRCUIT GAIN

$$V_{ADC} = \left[\left(\frac{V_{grid\_pk}}{N_{TR1}}\right) \cdot \frac{R36}{R31} + 2.5V\right] \cdot \frac{R32}{R30 + R32}$$

APPENDIX D: SAFETY NOTICES



The following safety notices and operating instructions should be observed to avoid a safety hazard. If in any doubt, consult your supplier.

WARNING – This reference design must be earthed (grounded) at all times.

WARNING – This reference design should not be installed, operated, serviced or modified except by qualified personnel who understand the danger of electric shock hazards and have read and understood the user instructions. Any service or modification performed by the user is done at the user's own risk and voids all warranties.

WARNING – It is possible for the output terminals to be connected to the incoming AC mains supply and may be up to 410V with respect to ground, regardless of the input mains supply voltage applied. These terminals are live during operation and for some time after disconnection from the supply. Do not attempt to access the terminals or remove the cover during this time.

General Notices

- The reference design is intended for evaluation and development purposes and should only be operated in a normal laboratory environment as defined by IEC 61010-1:2001
- Clean with a dry cloth only
- Operate flat on a bench and do not move the reference design during operation
- The reference design should not be operated without all of the supplied covers fully secured in place
- The reference design should not be connected or operated if there is any apparent damage to the unit

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

ISBN: 978-1-62076-383-4

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Osaka
Tel: 81-66-152-7160
Fax: 81-66-152-9310

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

11/29/11