AN1426

Design Tips for the MCP3911

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INTRODUCTION

The central goal of this application note is to supply support material for a new MCP3911 design. In many systems, multiple MCP3911 devices will exist to measure multiple powers, currents, or voltages. Proper cascading of the delta sigma master clock (MCLK) and serial communication to lessen I/O usage on the microcontroller will be discussed. For energy metering and power monitoring systems, grounding and layout are essential when the MCP3911 is connected to the primary side of a high voltage system, e.g. shunt-based current sensing systems. PCB layout techniques, through proper analog and digital grounding, will be described here, using a reference design available for the MCP3911.

The operation of the ADC across different operating conditions will also be discussed. There are various ways to optimize the accuracy of the analog-to-digital conversion. Decisions such as choosing the correct oversampling ratio, or selecting proper MCLK speeds, can affect the conversion performance from a few dB to much more, in some cases.

Here, pushing the limits of the analog-to-digital conversion will be the focus, showing the true performance limits of the device.

Addressable Devices on Single SPI Bus

The MCP3911 analog front ends are addressable in such a way that multiple devices can be placed on a single SPI bus using a single CS pin. When ordering the devices, they can be purchased with different part numbers containing address codes A0, A1, A2 or A3. These address options correspond to the following address bits in the control byte of the MCP3911, shown in Figure 1.

These devices should all share the same oversampling clock, i.e. the OSC1 pin of these devices should be tied together. This clock is typically driven from an output compare or Pulse-width Modulation (PWM) module of the microcontroller, which is discussed in more detail later in this application note. This allows for a reduced pin count microcontroller to be used in a system such as shown in Figure 1.

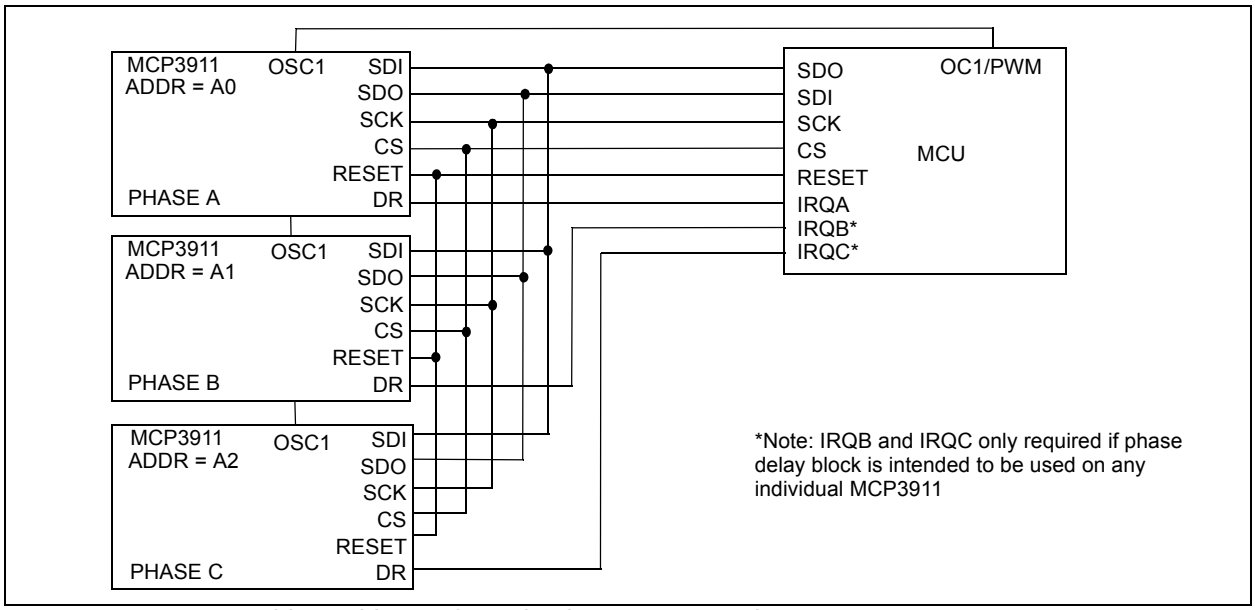

FIGURE 1: *Addressable SPI for Poly-phase Meter Designs.*

SINGLE VS. MULTIPLE IRQ

When the devices are clocked by a single MCLK, and the OSC1 pins are tied together, as long as the internal clock prescale and oversampling ratios are the same, the data ready pulse will be synchronized between the devices. This holds true only if there is no phase delay introduced into the PHASE register, or if the PHASE register values match. If it is intended for no phase delay to be introduced on any of the individual MCP3911 devices, then a single interrupt request pin (IRQ) can be used, and the devices are simply read in sequence prior to the next DR event.

Address Options:	A6	A5
A0	0	0
A1	0	1
A2	1	0
A3	1	1

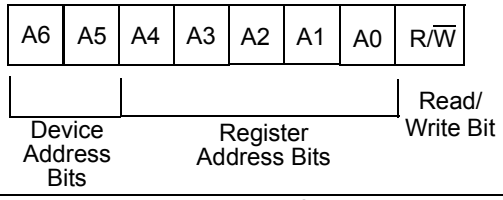

FIGURE 2: *Control Byte.*

One-command Configuration at System Startup

After V_{DD} has stabilized on the MCP3911, it is possible to configure the device for use in your application. For time-sensitive applications, a one-shot configuration word can be sent to write values across all configuration registers. The internal registers of the MCP3911 can be written to and clocked consecutively, without the need for raising CS between registers and transmitting multiple control bytes. There is no global address write command for multiple MCP3911 devices, so each MCP3911 device must be written to individually with separate address bytes. It is not necessary for the master clock (MCLK) of the MCP3911 to be active during this configuration loading on the SPI bus. It is also not necessary to reset the device before this configuration.

If you want to reset or configure all the devices simultaneously, simply stop the MCLK during the loading of the configuration registers. The SPI clock (SCK) will only load the serial interface register values. The internal function depends on the master digital clock MCLK, so starting this after the devices have been loaded would be equivalent to a global address write.

The PHASE:8, STATUSCOM:16, CONFIG:16, and optionally the offset and gain calibration registers OFFCAL_CH0:24,GAINCAL_CH0:24,OFFCAL_CH1:24, and GAINCAL_CH1:24 can all be written consecutively as shown in Figure 3.

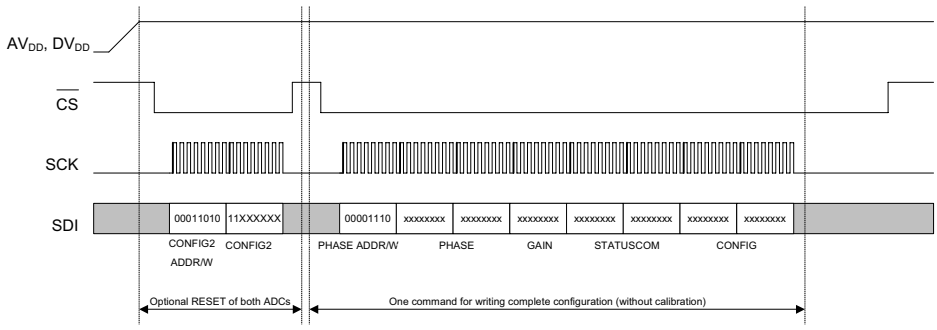

FIGURE 3: *Typical One Command Configuration.*

MCLK Generation

In a system such as the one shown in Figure 1, the MCLK generated by the microcontroller should always be present when measuring and calculating power quantities. In the system shown, the MCLK and MCU internal clock are synchronous, which is best when attempting to do a specific number of power calculations between an integer number of samples.

The MCP3911 contains an internal oscillator, which allows the device to be used with an external crystal. This draws slightly more current, the internal oscillator circuitry can be disabled by setting the CLKEXT bit to 0 if a crystal is not used, and the part receives an externally generated clock source, such as a pin on a microcontroller, as shown in Figure 1. For higher performance microcontrollers, the operating frequency of the MCU clock can be higher than the limit of the internal analog master clock (AMCLK) of the MCP3911.

For situations such as this, the internal prescaler of the MCP3911 should be used, as shown in Table 1, by changing the PRE bits in the configuration register.

TABLE 1: PRESCALER SETTINGS

Config PRE<1:0>		Analog Master Clock Prescale
0	0	AMCLK = MCLK/1 (default)
0	1	AMCLK = MCLK/2
1	0	AMCLK = MCLK/4
1	1	AMCLK = MCLK/8

Continuous Read Modes

The MCP3911 has various read modes that allow you to loop over certain regions of addresses. These modes are available by changing the READ bits in the CONFIGURATION register. This allows the user to avoid sending multiple control bytes.

There are a total of four read modes. Registers that are defined as groups can be read continuously with a single CS assertion. Registers that are defined as types can be read continuously with a single CS assertion. The entire register map can be read continuously with a single CS assertion, or a single register can be read repeatedly with a single CS assertion. A description of the register types and groups are defined in Table 2. Note this is a partial listing of the register set.

TABLE 2: REGISTER MAP GROUPING FOR ALL CONTINUOUS READ/ WRITE MODES

Function	Address	READ<1:0> = 11	READ<1:0> = 10	READ<1:0> = 01
CHANNEL 0	0x00	LOOP ENTIRE REGISTER MAP	TYPE	GROUP
	0x01			
	0x02			
CHANNEL 1	0x03			GROUP
	0x04			
	0x05			
MOD	0x06		TYPE	GROUP
PHASE	0x07			
	0x08			
GAIN	0x09			
STATUSCOM	0x0A			GROUP
	0x0B			
CONFIG	0x0C			
	0x0D			

Power Optimization

The MCP3911 has many low power options that should be used to lessen the power consumption of the device, given certain application environments. The various blocks of the device that can be shut down will be described here.

OSCILLATOR CIRCUIT

The MCP3911 contains an internal oscillator that allows the device to be connected to a low-cost crystal and generate its own internal clock source. In applications where a MCU is driving the clock (or some other clock source), the oscillator circuit of the device can be put into shutdown mode, saving current. This is done by setting the CLKEXT bit in the CONFIG register to logic high.

MCLK SPEED AND OSR SELECTION

AMCLK is the internal clock speed that is post prescaler and drives the sample rate of the device. If your application is power sensitive, the bandwidth of the system should be thoroughly investigated, as the internal clock speed and sampling rate is the overall factor in determining the current drawn through DV_{DD} pin, DI_{DD}.

Changing the Oversampling Ratio (OSR) will have no effect on AI_{DD}, i.e. increasing the oversampling to get higher accuracy data at a slower rate will *not* diminish the power consumed inside the MCP3911. However, from an overall system perspective, the use of higher OSRs on the MCP3911 will greatly reduce any post averaging and power consumption that might then be needed on the MCU. Therefore, it is always best to use the highest OSR as possible, to put the averaging on the MCP3911, and reduce the data rate and processing that occurs on the MCU. The bandwidth of the application will limit the highest OSR. For power measurement and energy metering applications, typically the 50^{th} or 60^{th} harmonic is enough for adequate bandwidth selection. So for a 60 Hz line frequency, this would require at minimum a 4-5 ksps rate from the ADC. The relationship between sample rate (DRCLK), OSR, and MCLK is shown in the following equation.

EQUATION 1:

$$DRCLK = \frac{DMCLK}{OSR} = \frac{AMCLK}{4 \times OSR} = \frac{MCLK}{4 \times OSR \times PRESCALE}$$

So for a target data rate of ~4 ksps, an OSR of 256 can be used from a MCLK of 4 MHz.

To directly change the digital current consumption, a slower MCLK can be used, if the bandwidth of the application allows it. Digital I_{DD} (DI_{DD}) is directly tied to the MCLK rate. If power consumption is more important than analog to digital conversion, then a slower MCLK with a lower OSR might yield ADC results that are sufficient for the application, while keeping the power consumption lower.

ANALOG CURRENT BOOST

The driving factor of the analog I_{DD}, (AI_{DD}), is the current boost setting in the CONFIG register. The current boost options determine how much current is given to the analog portion of the device, which drives the delta sigma modulator, PGA, and other blocks crucial to the A/D conversion. For slower sampling speeds, the current required by this circuit is lessened, and a lower boost setting should be used.

The following figure shows the trade-off in AI_{DD} for the different boost settings, and also the relationship between MCLK and DI_{DD}. Notice that AI_{DD} is not affected by increasing the MCLK, only by changing the BOOST setting.

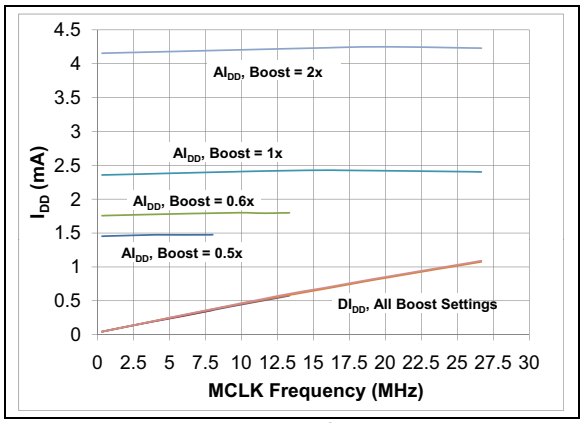

FIGURE 4: *Operating Current vs. MCLK and BOOST Settings, V_{DD} = 3.3V.*

So the obvious next question should be, how do I determine the correct BOOST setting for my application? Once you have determined the appropriate sample rate and MCLK frequency for your application, you can choose the correct boost setting. As you can see from the following figure, the performance of the device (shown here by measuring Signal-to-Noise and Distortion Ratio (SINAD)) is drastically impacted at certain sampling rates, if the proper current boost is not selected.

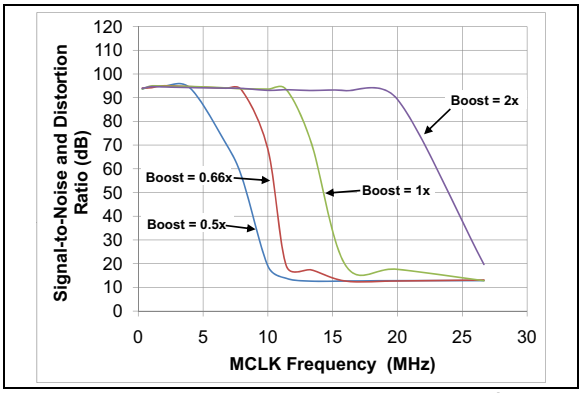

FIGURE 5: *SINAD vs. MCLK and BOOST Settings, V_{DD} = 3.3V.*

Here you can see, for the lowest boost setting that consumes the least power (Boost = 0.5x), performance falls off around 3-4 MHz. Whereas, the highest current boost setting that consumes the most power (Boost = 2x), AMCLK can be driven to almost 20 MHz with no degradation of performance. The above graph is for PGA GAIN = 1 and for V_{DD} = 3.3V. This graph does not tell the entire story, as maximum clock rates are also slightly effected by PGA gain and V_{DD}. Table 3 provides a more complete story, showing recommended maximum clock speeds as a function of BOOST, PGA, and V_{DD}. This table was generated by selecting the limit where SINAD was more than -5 dB from its maximum.

TABLE 3: MAXIMUM AMCLK LIMITS AS A FUNCTION OF BOOST AND PGA GAIN

Conditions		V_{DD} = 3.0V to 3.6V, T_A from -40°C to 125°C		V_{DD} = 2.7V to 3.6V, T_A from -40°C to 125°C	
Boost	Gain	Maximum AMCLK (MHz)	Maximum AMCLK (MHz)	Maximum AMCLK (MHz)	Maximum AMCLK (MHz)
0.5x	1	3	3	3	3
0.66x	1	4	4	4	4
1x	1	10	10	10	10
2x	1	16	16	16	16
0.5x	2	2.5	3	3	3
0.66x	2	4	4	4	4
1x	2	10	10	10	10
2x	2	14.5	16	13.3	14.5
0.5x	4	2.5	2.5	2.5	2.5
0.66x	4	4	4	4	4
1x	4	10	10	8	10
2x	4	13.3	16	10.7	11.4
0.5x	8	2.5	2.5	2.5	2.5
0.66x	8	4	4	4	4
1x	8	10	10	6.7	8
2x	8	10	14.5	8	8
0.5x	16	2	2	2	2
0.66x	16	4	4	4	4
1x	16	10.6	10.6	8	10
2x	16	12.3	16	8	10.7
0.5x	32	2	2	2	2
0.66x	32	4	4	4	4
1x	32	10	11.4	8	10
2x	32	13.3	16	8	10

FULL SHUTDOWN MODE

The MCP3911 offers the ability to put the device into extreme low power mode for situations when the ADCs are not being used. These modes shut off the entire analog section of the chip and consume less than 1 micro amp of power. This is defined as “FULL SHUTDOWN MODE” and can be entered by setting the shutdown bits in the CONFIG register. This mode disables everything in the device, including the POR, so care should be taken when using this shutdown mode.

Detecting a POR event inside the MCP3911

In certain applications, it may be useful for the system to know if a Power on Reset (POR) event has occurred inside the MCP3911. This can be caused if there is a glitch or other noise on the power supply and would erroneously reset all the configuration settings back to zero without the host MCU being aware (unless a check of the registers or a test against the configuration CRC is done).

One method of doing this would be to check the timing of the data ready (DR) pulses coming from the device. A POR is going to cause two extra 1/DRCLK time periods before the first DR pulse after POR, due to the SINC filter settling time.

Accuracy Optimization

Optimizing the device for proper AMCLK speeds and low power modes is not the only way to get the most out of the MCP3911. Using the device to get optimal accuracy from the analog-to-digital conversion is the primary concern in many applications. This section will discuss how to get the best dynamic performance (SINAD, and Total Harmonic Distortion (THD)) from the device under various situations.

CORRECT USE OF THE MCP3911 DITHERING BLOCK

The dithering block of the MCP3911 introduces non-correlated pseudo-random noise into the modulator output of the MCP3911, adding to the overall noise floor of the device. This additive noise, however, effectively lowers any correlated noise created by the MCP3911 device itself. This is the reason for decreased THD and improved INL for the device. However, the overall accuracy is typically denoted by looking at the Effective Number of Bits (ENOB) calculated from SINAD, which is a combination of the harmonics included in the THD specification, and the noise floor, accurately described by the Signal-to-Noise ratio (SNR). The important thing to note here is that since the dithering block is adding noise, depending on which OSR you are using, the oversampling may or may not be able to effectively remove the uncorrelated noise added by the dithering block. The following figure shows SINAD versus OSR at the different dithering options (see Figure 6).

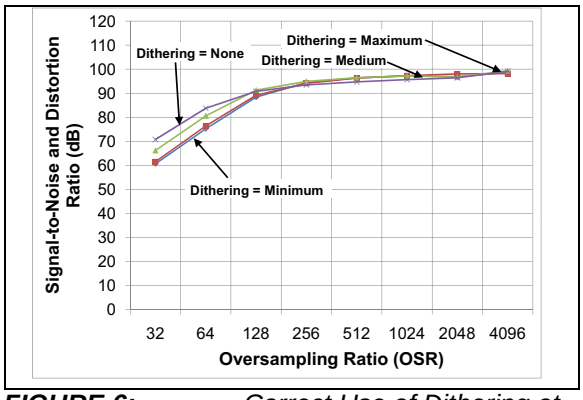

FIGURE 6: *Correct Use of Dithering at Various OSR Settings.*

It can be shown that for the lower OSR settings (OSR=32, OSR=64), the dithering should be turned off, or set to none. This will increase the overall performance by many dB and at least 1-2 bits of performance.

At the higher OSR, the dithering block has less of an impact, and should typically be turned ON, due to the improvement in THD, shown below:

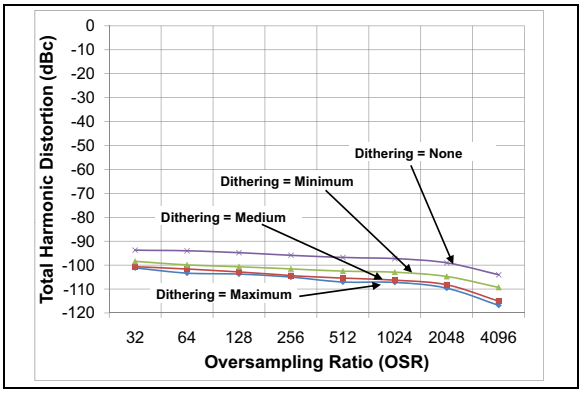

FIGURE 7: *THD vs. OSR.*

Here, the effect of the dithering block is lessened at the lower OSRs for removing the correlated noise, such as THD.

Hardware Layout / PCB Grounding

The MCP3911 is a mixed signal IC with both analog and digital ports. For power, it has both analog (AV_{DD}) and digital (DV_{DD}) pins. For grounding, it has both analog and digital ground pins as well, labeled AGND and DGND, respectively. An MCP3911 system will also include a microcontroller or DSP. As the device has been primarily designed for power and energy measurement-type applications, direct connection to the outside world via a high voltage power line is also a likely scenario, and a hurdle towards a low noise PCB design.

The schematic and layout discussed in this section are from a meter designed with the MCP3911 and PIC18F65J90. Complete schematic, layout, Gerbers and BOM are located on the MCP3911 product page on Microchip's web site.

The first point of discussion is the power supply, shown in Figure 8. This shows the connection directly to a high voltage line, e.g. a two-wire 120V or 220V system. A current sensing shunt is used for the current measurement on the high side (line side), and this also supplies the ground for the system. This is necessary, as the shunt is connected directly to the channel input pins of the MCP3911. If the shunt is off-board, it will require wires coming from the shunt to the inputs of the PCB here CP4 and CP5. To reduce sensitivity to external influences such as Electromagnetic Interference (EMI), these two wires should form a twisted pair, not shown in the figure.

Here you can see the shunt, which is connected across connection points CP4 and CP5. It is also connected to the ground of the system, initially to a node described here as GROUND B or GNDB. This is the most noisy place on the meter, as it is tied directly to the outside world, at the connection to the line. L4 and C13 provide some immunity to external noise. The capacitive power supply created by C12, C14, R11, D3, and D2 is more completely described in AN994 "IEC Compliant Active-Energy Meter Design" (DS00994B), also available on the MCP3911 product page on Microchip's web site. This document details component value selection for this part of the circuit. For this application note and the focus of discussion here, we are interested in the grounding and power scheme of this circuit. Note that the power supply components are all connected to GNDB, with inductive choke L5 separating GNDB from a new ground, GNDA, or Analog Ground.

Also shown here is the separation of a 3.3V digital and 3.3V analog supply. Depending on the cost sensitivity of the application, a single regulator with adequate filtering between a digital and analog supply rail might be sufficient. The most conservative approach is shown here.

C11 and C17 would represent the analog and digital "start' points, where sensitive components would be caught on power lines stemming from this base charging locale.

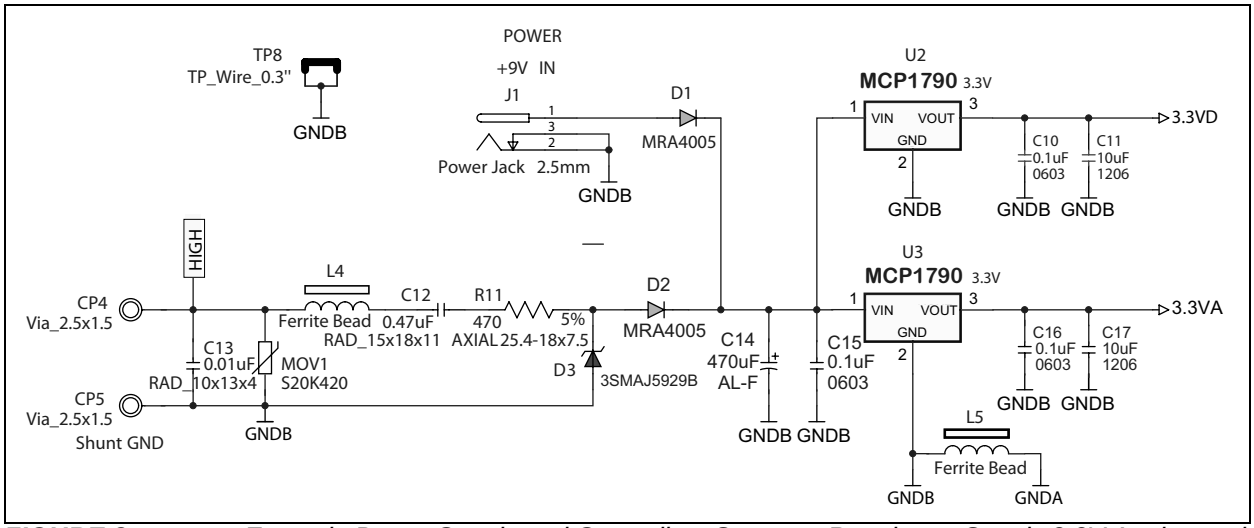

FIGURE 8: *Example Power Supply and Grounding, Separate Regulators Supply 3.3V Analog and 3.3V Digital.*

The analog ground (GNDA) is separated out to be home to the most noise sensitive part of the application circuit, where the signal sizes would typically be the smallest. In energy metering and power monitoring systems, this sensitive part is always the current sensing area of the PCB.

Small power shunts and small currents lead to very small signals going into the current channel of the MCP3911. For example, a 200 mΩ shunt measuring a current of 50 mA produces a peak-to-peak voltage of 28.2 µV. ($200 \times 10^{-6}\ \Omega \times 50 \times 10^{-3}$ A x 2 x sqrt(2) = 28.2 x 10^{-6} V). These small signals must all be kept separate from other parts of the system.

Taking a closer look at Figure 9, you will notice that all components associated with the current input path are connected to the analog ground (GNDA). Also note that the voltage reference bypass capacitors C8 and C9 are also connected to this ground plane. The analog ground and the analog V_{DD} are also connected and bypassed to GNDA. DGND and the digital side of the device are connected to GNDB.

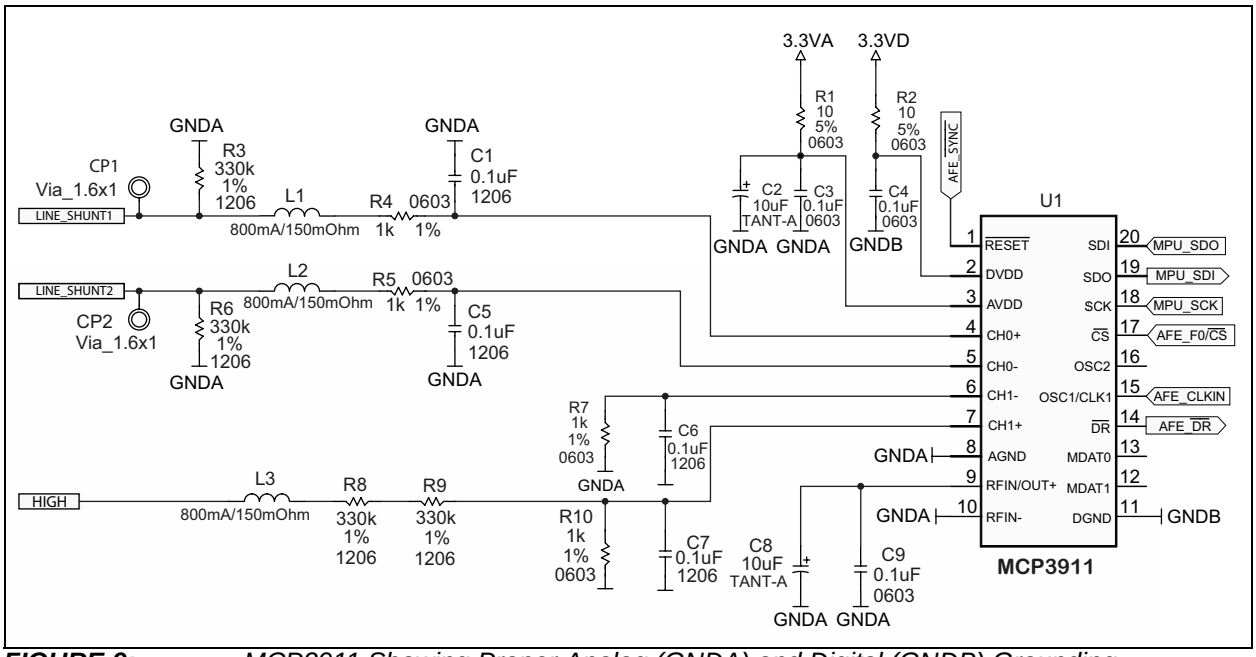

FIGURE 9: *MCP3911 Showing Proper Analog (GNDA) and Digital (GNDB) Grounding.*

PCB LAYOUT

For component placement and layout, the utmost care must be given to this area also. The traces on the PCB must be kept as short as possible, and any symmetry within the differential pair must be maintained.

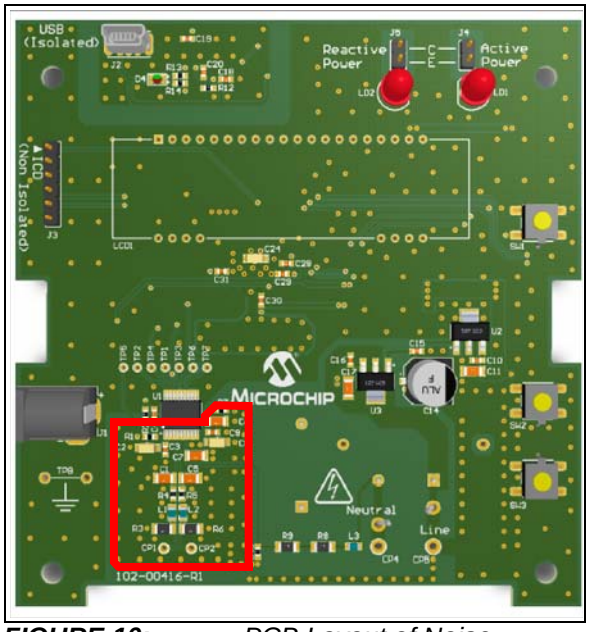

FIGURE 10: *PCB Layout of Noise Sensitive Components; Red Line Represents Analog Ground Plane AGND.*

The red line in Figure 10 represents the AGND section of the PCB. The power supply and MCU are separated on the right hand side of the PCB, surrounded by the digital ground plane. The MCP3911 is kept on the left hand side, surrounded by the analog ground plane.

The back side of the board shows the same ground plan, again surrounded in red. There are two separate power supplies going to the digital section of the system and the analog section, including the MCP3911. Here you can also see the ferrite bead that is connecting the analog and digital ground places, circled in yellow in Figure 11.

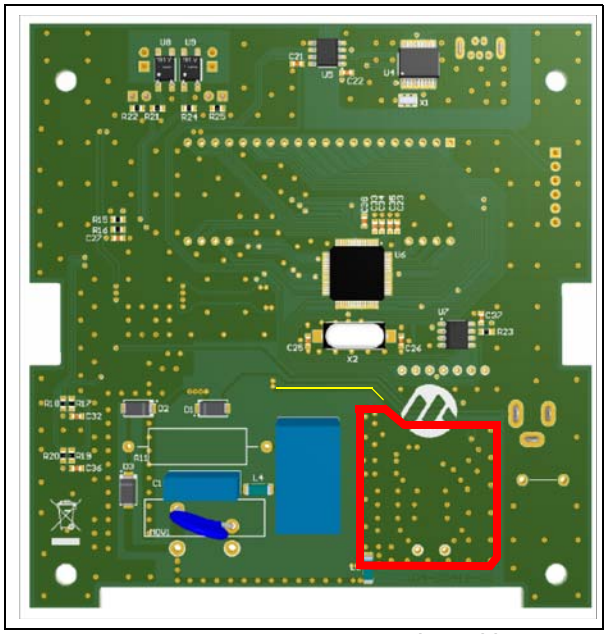

FIGURE 11: *MCP3911 Design with Proper Analog and Digital Grounding and Power Supply Layout.*

The ferrite bead between the digital and analog ground planes helps to keep high frequency noise from entering through the device. Also, they are typically placed on the shunt inputs and into the power supply circuit for additional protection.

Summary

The MCP3911 is a highly accurate analog-to-digital converter that can achieve 15.5 effective number of bits (ENOB) with extremely low signal levels. Proper PCB design is essential, especially when dealing with primary side high-voltage designs. The device is extremely configurable and offers the user many choices for varying applications. When used correctly, it offers a powerful solution to analog-to-digital conversion needs.

REFERENCE

[1] MCP3911 Data Sheet, “3.3V Two-Channel Analog Front End”, Microchip Technology Inc., DS22286, 2012.

NOTES:

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