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High-Quality Audio Applications Using the PIC32

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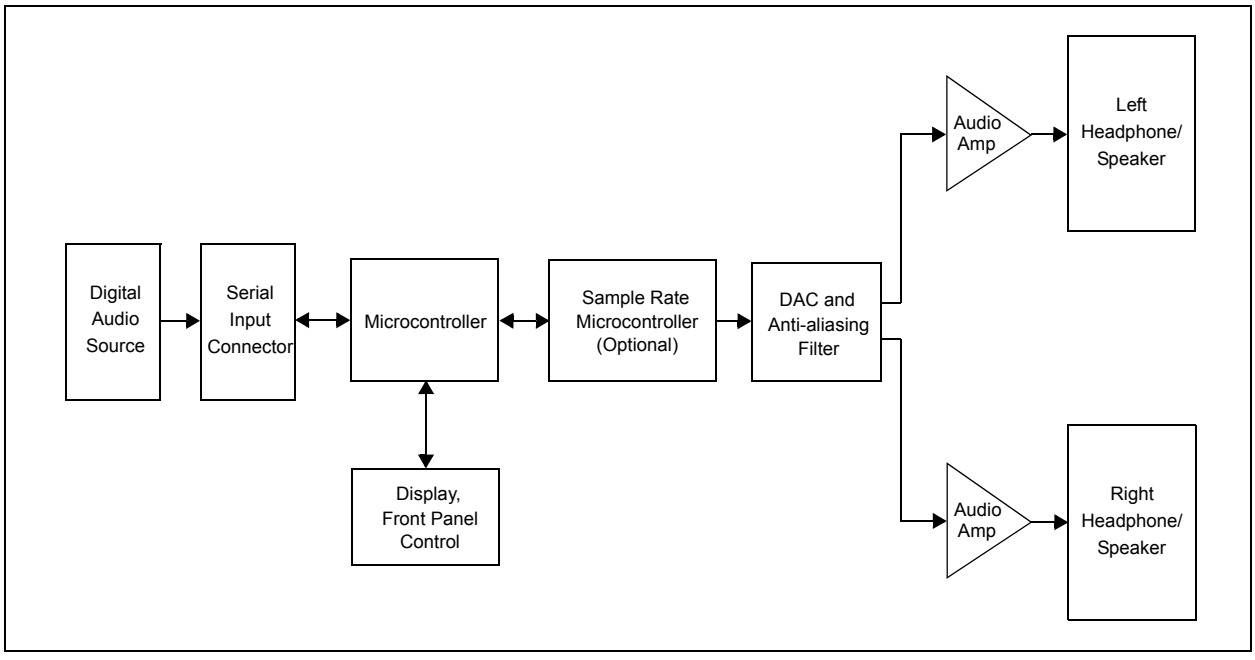
When designing audio docking stations and accessories for portable digital audio devices, and other digital audio sources, designers are constrained by cost, while trying to deliver the highest-quality audio playback.

In a typical docking station and device accessory, a digital audio source that plugs into the unit sends a serial stereo audio data stream over the dock's data transfer interface, such as USB. The dock captures the data stream while performing other crucial tasks, and routes the stream to an audio Codec or Digital-to-Analog Converter (DAC) at a specific sample rate, as shown in Figure 1.

The captured stereo audio stream then flows through a serial interface to the codec or DAC. Since there are many possible sources of digitized audio, and not all of the sources use the same sampling rate, this serial interface typically adapts the sampling frequency to the source, or converts the sampled data stream into a common data rate. Therefore, one of the challenges in the design of the docking system or device accessory is to perform the sample-rate conversion without degrading the audio quality, and at the lowest cost possible. To deal with these challenges, designers have typically used a dedicated sample-rate conversion circuit and/or a high-end audio DAC that incorporates complex Phase-Locked Loops (PLLs) to ensure flexible sample rates for stable communication of the sampled audio data.

FIGURE 1: TYPICAL AUDIO APPLICATION



The USB interface is a convenient interface for the transfer of audio data. However, to meet the requirements of professional audio, the subtle loss of quality due to USB clock and codec clock mismatch must be addressed.

In this application note, the available audio-specific features of the PIC32 MCU are explored to address these needs. The SPI module supports different standard audio communication modes and offers high bit resolution for high-quality audio applications. The flexible reference clock output feature of the PIC32 MCU can be used to provide the master clock to the analog front-end to generate the different sample rates. The reference clock output also eliminates the need for an external crystal/oscillator by a codec. It also eliminates the need for a PLL on the codec. The reference clock output can be tuned to prevent buffer underrun and overrun that arise because of clock mismatches. The PIC32 MCU also offers the USB Host and Device module with flexible PLL clocking schemes at low power.

DIGITAL AUDIO DATA BASICS

When analog audio is converted into a discrete digital format, the analog signal is sampled at a frequency of at least twice the highest frequency component in the analog signal, or the Nyquist rate. Therefore, an audio signal that spans 0 to 20 kHz can be sampled at a data rate of 44.1 kHz, which in this case, is the suitable Nyquist rate, so that the signal can be reconstructed without aliasing when converted back to the analog domain. In addition to the sampling rate, data bit resolution can be 16-bit or 24-bit stereo audio data. For compact disc (CD) quality audio, the standard is 16-bit resolution with a 44.1 kHz sample rate. However, there are higher-performance CD music options. One such standard encodes the data with a 24-bit resolution and increases the sampling rate to 96 kHz. For professional audio, the audio files are encoded with a resolution of 24 bits per sample, which provides headroom when the audio is mixed and manipulated. Also, the resolution choice allows for the trade-off of sound quality versus file size even with compression.

The USB interface can readily handle the streaming of high-quality audio over isochronous transfers. Its ability to deliver high-quality audio is quite evident, as it is popular among many audio users. With its universal ease-of-use, USB audio can transfer high-resolution and high-sample-rate audio with negligible jitter, when packaged with a flexible audio interface. Isochronous data transfer, amongst its various other uses, is utilized to stream audio data to and from a source at a constant rate in real time.

Stereo audio data packets, with size governed by the sample rate of the audio stream, are transferred as part of USB frames every 1 ms on the USB full-speed link. USB audio also provides controls for common features such as volume, tone, gain control, and equalizers, among many control and processing units.

The differences in bit rates and sample rates require the hardware in the playback system, or dock, to be able to handle the differing rate data streams. To do that, the system must either use a more complex DAC that is expensive and can phase-lock to each sample rate and adjust itself to each playback option, or use an external sample-rate converter IC with the low-cost DAC, or convert all the streams into a standard sample rate and bit rate using an algorithm running on a microcontroller that a simple low cost DAC can handle. The PIC32 MCU offers a flexible reference clock output and audio mode to address these requirements to achieve high-quality audio while maintain a low design cost. The serial interface with the Audio mode and flexible reference clock output module are explored in the following sections.

PIC32 SERIAL PERIPHERAL INTERFACE (SPI) MODULE WITH AUDIO MODE

Most codecs offer serial communication over a 4-line serial interface. The transmission and reception of the stereo audio samples between the MCU and codec occur over this serial interface. Typical serial interfaces have the following signals:

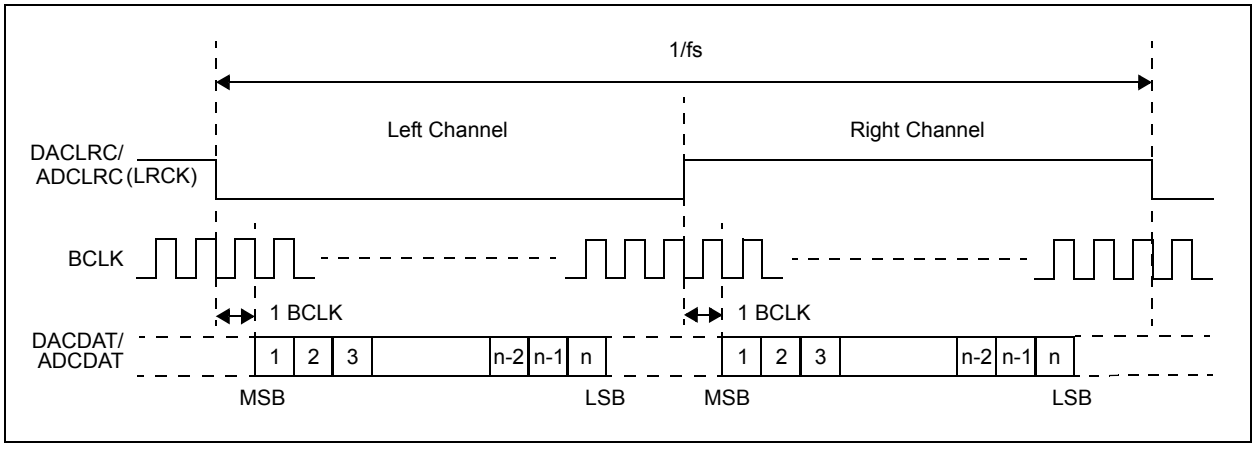
- Serial Data Output (SDO) to transmit stereo audio data to the codec
- Serial Data Input (SDI) to receive stereo audio data from the codec
- Serial Bit Clock (SCK/BCLK) is the required bit clock provided by the Master
- Left/Right Clock (LRCK) is the phase clock provided by the Master for stereo data

PIC32 devices have a SPI module with Audio mode. Audio mode offers various interface formats, bit resolutions, and Master/Slave configurations. The communication modes supported include the following:

- **I²S Format**

  I²S mode is where the Most Significant Byte (MSB) is available on the second rising edge of the BCLK following a LRCK transition. For more information on the I²S protocol, refer to the I²S Bus Specification from Philips Semiconductors (http://www.classic.nxp.com/acrobat_download2/various/I2SBUS.pdf).

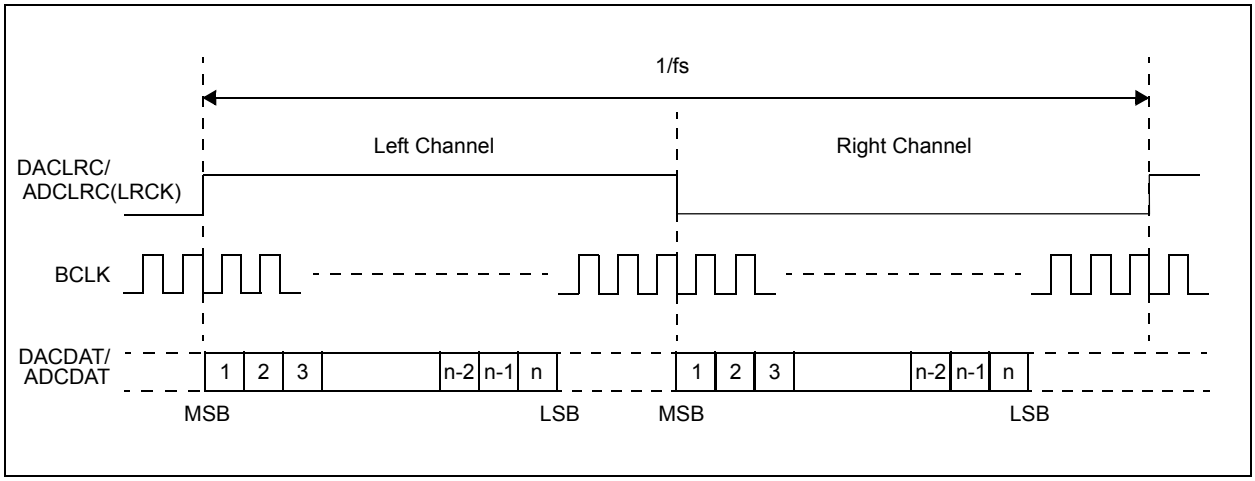
FIGURE 2: I²S FORMAT



- **Left-Justified Format**

  Left-Justified mode is where the MSB is available on the first rising edge of BCLK following a LRCK transition

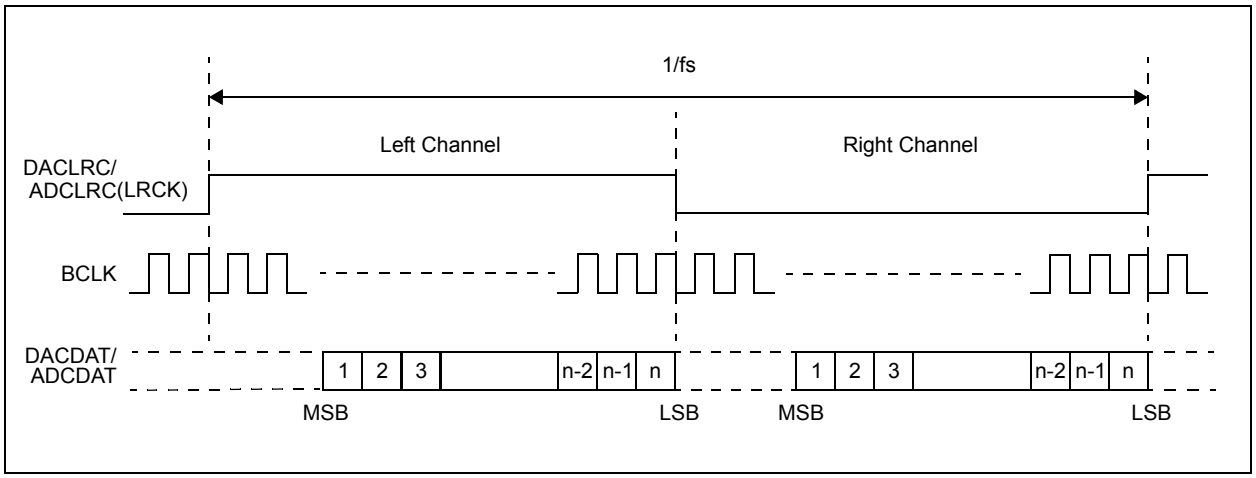
FIGURE 3: LEFT-JUSTIFIED FORMAT



- **Right-Justified Format**

  Right-Justified mode is where the Least Significant Byte (LSB) is available on the rising edge of the BCLK preceding a LRCK transition and the MSB is still transmitted first.

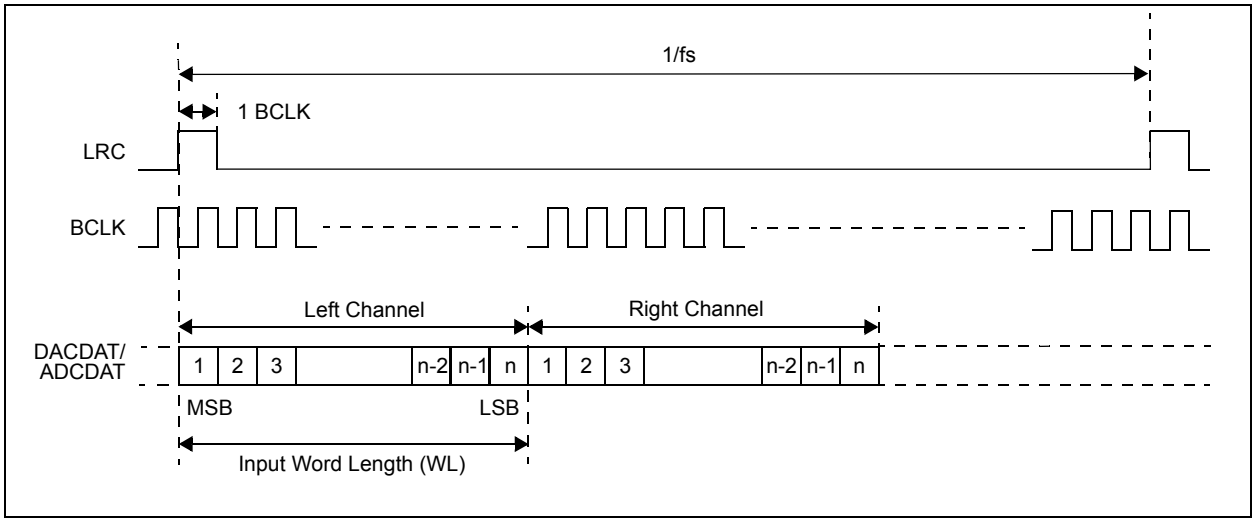
FIGURE 4: RIGHT-JUSTIFIED FORMAT



- **DSP/PCM Format**

  In DSP/PCM mode, the left channel MSB is available on the first rising edge of the BCLK following a rising edge of the LRC. Right channel data immediately follows left channel data. Depending on word length, the BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

FIGURE 5: DSP/PCM FORMAT



PIC32 Audio mode supports 16, 24, and 32-bit stereo audio data. It also provides advanced error handling with receive overflow and transmit underrun flags and control bits to disable them as required. Also, the clocks generated by the BCLK and the LRC when the PIC32 MCU is a serial Master are free running, which is essential for uninterrupted audio data transfer in streaming applications.

The audio codecs and DACs allow either or both of these configurations: Master or Slave. In the PIC32 SPI Audio mode Master configuration, the PIC32 MCU provides the BCLK and the LRCK to the codec. This configuration is shown in Figure 6. In the PIC32 SPI Audio mode Slave configuration, the codec provides the Bit Clock (BCLK) and Stereo phase clock (LRCK) to the PIC32 MCU. This configuration is shown in Figure 7.

PIC32 devices also provide a control interface channel over the Inter-Integrated Circuit™ (I^2C™) peripheral module. The control interface is used to configure the codec for a specific mode of operation by configuring the control registers on the codecs.

FIGURE 6: PIC32 SPI-CODEC CONFIGURATION WITH PIC32 SPI AS MASTER AND THE CODEC AS SLAVE

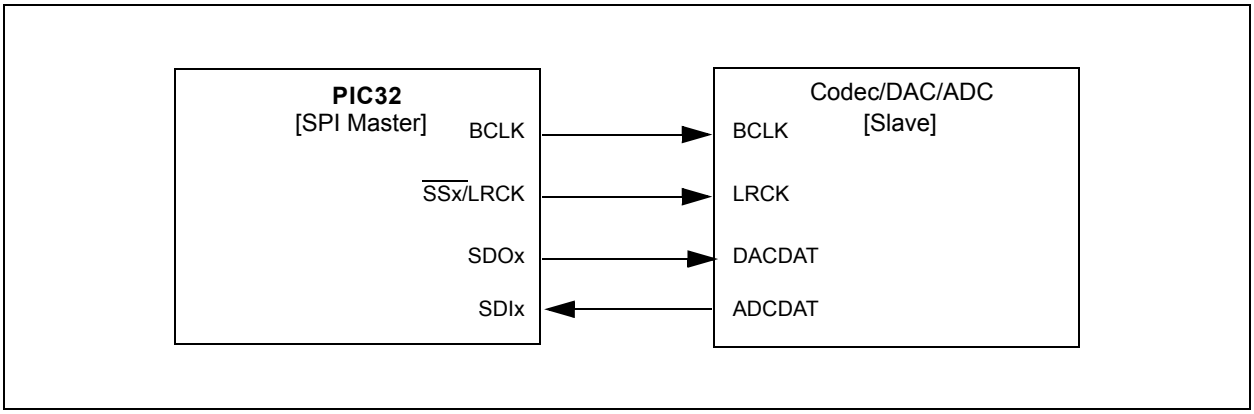
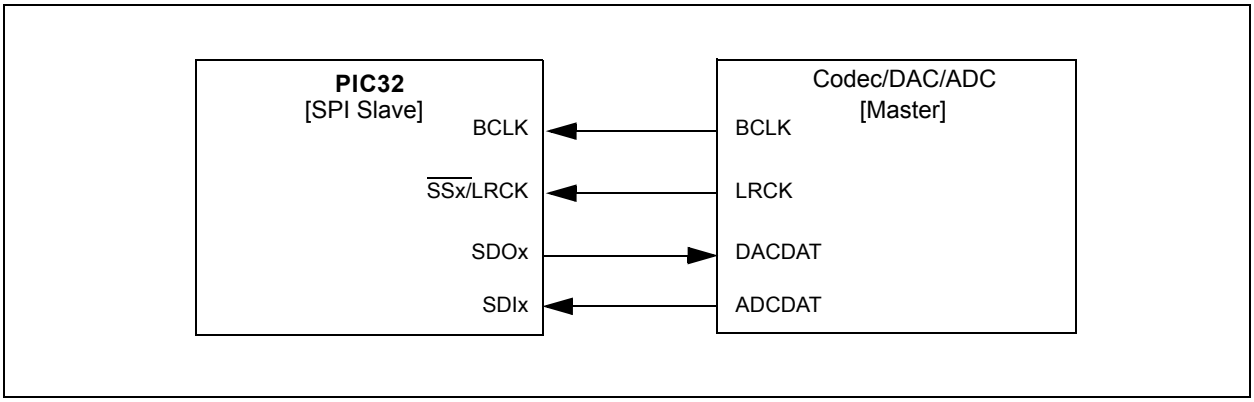


FIGURE 7: PIC32 SPI-CODEC CONFIGURATION WITH PIC32 SPI AS SLAVE AND THE CODEC AS MASTER



FLEXIBLE REFERENCE CLOCK OUTPUT

The PIC32 devices have a flexible reference clock output. The reference clock output module (REFCLKO) can be used to generate the fractional clock that can be used by audio codec/DACs to accommodate various sample rates. Typical examples of these sample rates and associated master clocks are shown in Table 1. The REFCLKO module can be used to generate these audio specific Master clocks and not limited to just these.

The reference clock can be mapped to any port pin on the device if the Peripheral Pin Select (PPS) functionality permits on the specific device. REFCLKO can be configured to the source clock for the SPI module on the PIC32 MCU instead of the peripheral bus clock. This ensures synchronization of the USB clock with the SPI channel clock to minimize effects of clock jitter when the USB PLL clock is selected as the source clock for the REFCLKO. The stereo word select signal and the bit clock will be synchronized with reference clock output since all of them are sourced off the reference clock output.

FIGURE 8: SPI AND CODEC CONFIGURATION SHOWING THE REFERENCE CLOCK OUTPUT SIGNAL

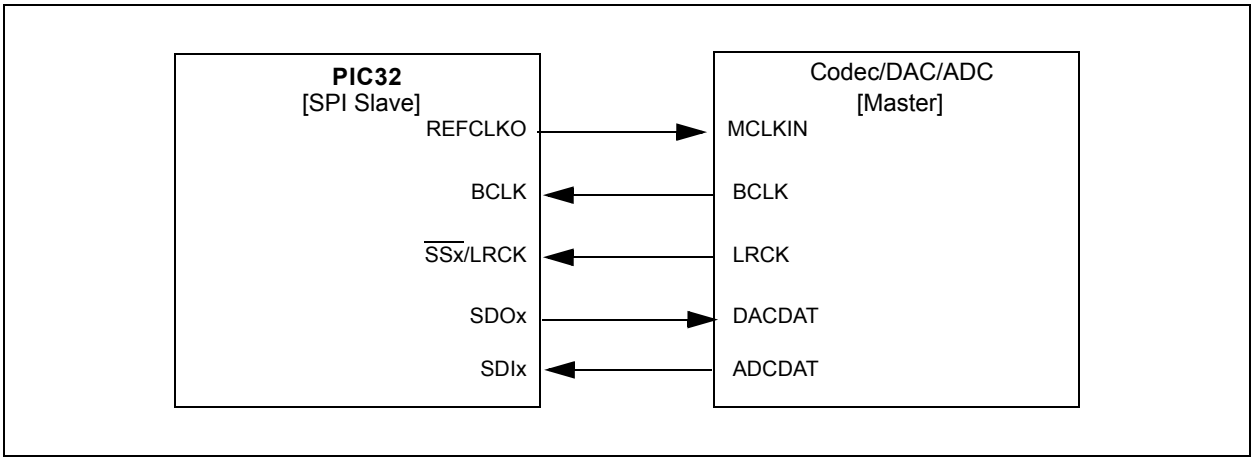


TABLE 1: TYPICAL MASTER CLOCKS AND BIT CLOCKS REQUIRED BY THE CODEC/DAC/ADC FOR DIFFERENT AUDIO SAMPLE RATES

Sample Rate (kHz)	Codec Master Clock/Time Base with Different Oversampling (MHz)							Bit Clock (MHz)	
fs	128 fs	192 fs	256 fs	384 fs	512 fs	768 fs	1152 fs	32 fs	64 fs
32.0	—	—	8.1920	12.2880	16.3840	24.5760	36.8640	1.024	2.0480
44.1	—	—	11.2896	16.9344	22.5792	33.8688	—	1.4112	2.8224
48.0	—	—	12.2880	18.4320	24.5760	36.8640	—	1.536	3.0720
88.2	11.2896	16.9344	22.5792	33.8688	—	—	—	2.8224	5.6448
96.0	12.2880	18.4320	24.5760	36.8640	—	—	—	3.072	6.1440
176.4	22.5792	33.8688	—	—	—	—	—	5.6448	11.2896
192.0	24.5760	36.8640	—	—	—	—	—	6.144	12.2880

The clock source for the reference clock output module has various options. It can be selected from USB-PLL, Primary PLL, POSC, FRC, SOSC, LPRC, PBCLK, SYSCLK clocks. Based on the selected clock source, a fractional divisor needs to be configured for the REFCLKO to generate the needed MCLK based on the oversampling rate as noted in Table 2. The fractional divisor needed is configured as an integer part and fractional part determined by RODIV and REFOTRIM bits in the REFOCON register, respectively. Figure 9 shows the PIC32 Oscillator module with the reference clock output indicating the different clock sources for the reference clock output and the divider with the trimming scheme.

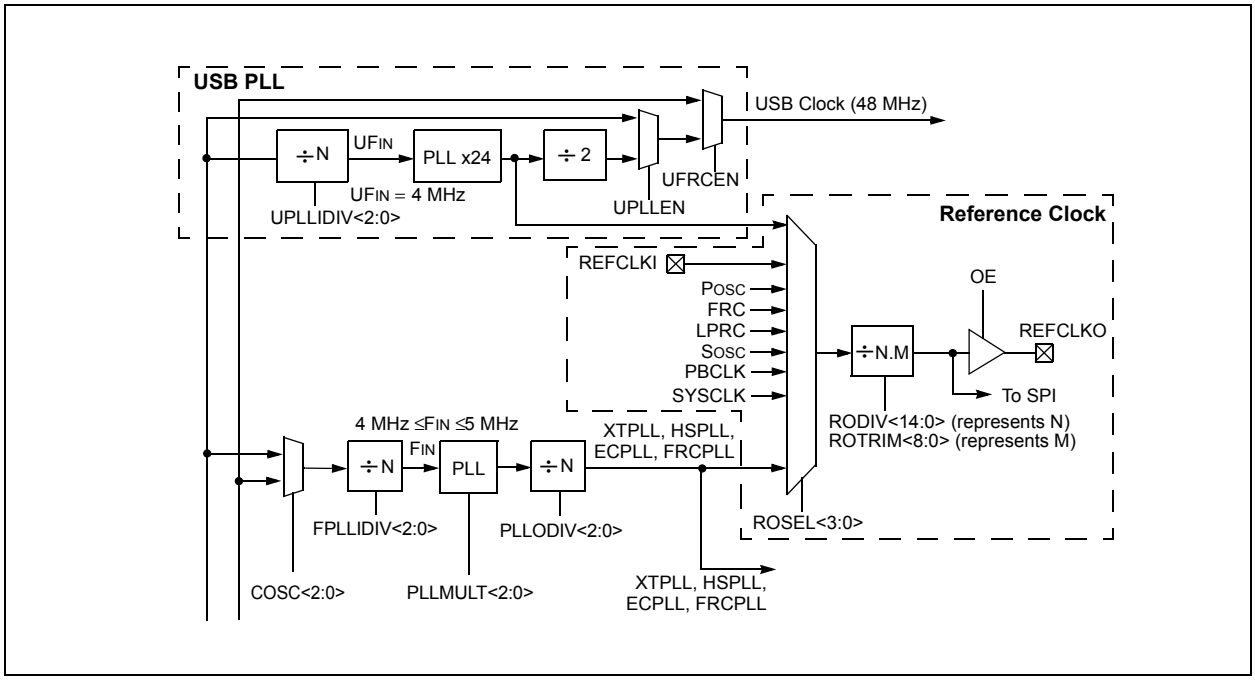
When the PIC32 SPI is the Master, the BCLK and the LRCK are generated by the device. With REFCLKO as the clock source for the SPI module, the BCLK can be configured by loading the appropriate values in the SPI Baud Rate Generator register, SPIxBRG. If needed, the REFCLKO can provide the master clock input to the codec.

As shown in Table 2, the SPIxBRG register values and the required REFCLKO frequencies for the audio sample rates are 32/44.1/48 kHz for stereo audio data with both 16-bit and 24-bit resolution. The bit clock, BCLK, can be 32 fs or 64 fs. When the PIC32 SPI is the Slave, the BCLK and the LRCK are generated by the codec. The reference clock output can provide the master clock for the codec/DAC.

TABLE 2: BAUD RATE VALUES WHEN THE PIC32 SPI IS CONFIGURED AS A MASTER

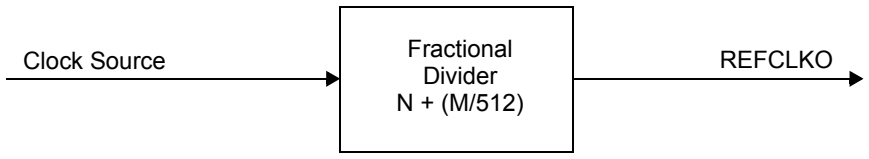
MCLK (MHz)	Sample Rate (kHz)	Bit Clock (MHz)		SPIxBRG	
		32 fs (16-bit)	64 fs (24-bit)	32 fs (16-bit)	64 fs (24-bit)
11.2896	44.1	1.4112	2.8224	4	2
12.2880	48	1.536	3.072	4	2
	32	1.024	2.048	6	3
8.1920	32	1.024	2.048	4	2

FIGURE 9: BLOCK DIAGRAM OF THE PIC32 OSCILLATOR SHOWING THE REFERENCE CLOCK OUTPUT



Lets explore an example of generating a REFCLKO signal. If the required MCLK is 12.288 MHz and if the USB-PLL clock of 96 MHz is used as source for the reference clock output, the required divisor is 7.8125. The divisor needs to be programmed for a half period of 3.90625, which is (7.8125/2). The RODIV bits will be configured with a value of 3 and ROTRIM configured for 464/512 = 0.90625.

EXAMPLE 1: RODIV AND ROTRIM VALUES FOR REFCLKO OF 12.288 MHz



MCLK		= 12.288 MHz
Clock Source USB-PLL		= 96 MHz
REFCLKO Divisor		= (Clock source/MCLK)/2 = (96 MHz/12.288 MHz)/2 = 3.90625 = 3(464/512)
RODIV	(N)	= 3
ROTRIM	(M)	= 464

Table 4 provides the required RODIV and ROTRIM values needed for the standard audio MCLKs previously listed in Table 1. The clock source selected here is the USB-PLL clock. However, any other clock source can be selected and the RODIV and ROTRIM values can be calculated in a similar manner.

The reference clock output can be changed with a fine precision. The unit resolution is between approximately 0.02 to 0.05% based on the generated clock frequency. This ensures that the sample rate deviation is well below the limits required by the codec when the reference clock output is only being used as the SPI clock source and not as the master clock to the codec. If the reference clock output is used as the master clock for the codec, the deviation is only limited by the specification of the codec.

Table 3 shows an example of an audio master clock generated by an expensive codec with flexible internal PLL using a standard external crystal of 12MHz and the master clock using reference clock output. The data indicate that the master clock generated by the PIC32 reference clock output is very close to the required master clock. Also the reference clock output performs as good as or better than the master clock generated using the internal PLL on an expensive codec. This would eliminate the need for a PLL on the codec or DAC used as an analog front end and eliminate the need for an external crystal used as time base for the codec. This will result in cost savings in the audio design while providing the same or better quality than an expensive codec.

TABLE 3: COMPARISON OF MASTER CLOCK GENERATED USING THE CODEC PLL AND REFERENCE CLOCK OUTPUT ON A PIC32 DEVICE

Expected Master Clock (MHz)	Average Master Clock using External Crystal (MHz)	Average Master Clock using REFCLKO (MHz)
8.192	8.192	8.192
11.2896	11.2889025	11.28893
12.288	12.288	12.288

TABLE 4: DIVISOR AND TRIMMING VALUES FOR DIFFERENT MASTER CLOCKS

MCLK (MHz)	Divisor with USB-PLL of 96 MHz as Clock Source	RODIV (N)	ROTRIM (M/512)	Observed MCLK (MHz)	%Deviation
8.1920	5.859375	5	440	8.1920	0
11.2896	4.251701	4	128	11.28893	0.005937
12.2880	3.90625	3	464	12.2880	0
16.3840	2.929688	2	476	16.3840	0
16.9344	2.834467	2	427	16.93728	0.01703
18.4320	2.604167	2	309	18.43661	0.02501
22.5792	2.12585	2	64	22.58824	0.04002
24.5760	1.953125	1	488	24.5760	0
33.8688	1.417234	1	213	33.85124	0.051848
36.8640	1.302083	1	154	36.84558	0.049975

Table 5, Table 6, and Table 7 show examples of the signal quality metrics, SNR and THD, for a set of (pure) audio tones generated using external crystal with internal PLL on the codec and using the reference clock output as master clock on the same codec. The SNR metric or Signal-to-Noise Ratio measures the power of the noise induced compared to the signal. The higher the SNR metric the better is the quality of the signal produced. The THD metric or the total harmonic distortion measures the strength of harmonic distortion caused by the harmonics of the fundamental frequency. The lower the THD metric the better is the quality of the signal produced. The SNR and THD data below indicates that quality of audio signal generated by an AFE with reference clock output as the time base performs exceptionally compared to that of a very expensive codec with internal PLL.

TABLE 5: OBSERVED THD AND SNR USING CODEC PLL AND PIC32 REFERENCE CLOCK OUTPUT – SAMPLE RATE OF 32 kHz, EXPECTED MASTER CLOCK OF 8.192 MHz

fs = 32 kHz	Using External Crystal as Time Base			Using Reference Clock Output as Time Base		
Expected Frequency (Hz)	Average Observed Frequency (Hz)	THD (%)	SINAD (dB)	Average Observed Frequency (Hz)	THD (%)	SINAD (dB)
500	499.9649	0.002	88.62	499.9668	0.00224	88.476
1000	999.9318	0.00224	88.752	999.9342	0.002	88.752
1500	1499.895	0.00208	88.308	1499.901	0.00192	88.308
10000	9999.318	0.002	82.212	9999.335	0.002	82.212

TABLE 6: OBSERVED THD AND SNR USING CODEC PLL AND PIC32 REFERENCE CLOCK OUTPUT – SAMPLE RATE OF 44.1 kHz, EXPECTED MASTER CLOCK OF 11.2896 MHz

fs = 44.1 kHz	Using External Crystal as Time Base			Using Reference Clock Output as Time Base		
Expected Frequency (Hz)	Average Observed Frequency (Hz)	THD (%)	SINAD (dB)	Average Observed Frequency (Hz)	THD (%)	SINAD (dB)
500	499.9649	0.00208	88.632	499.9668	0.00168	88.62
1000	999.9318	0.00184	88.332	999.9342	0.002	88.548
1500	1499.895	0.00168	88.38	1499.901	0.00176	88.212
10000	9999.318	0.00192	83.148	9999.335	0.00208	82.968

TABLE 7: OBSERVED THD AND SNR USING CODEC PLL AND PIC32 REFERENCE CLOCK OUTPUT – SAMPLE RATE OF 48 kHz, EXPECTED MASTER CLOCK OF 12.288 MHz

fs = 48 kHz	Using External Crystal as Time Base			Using Reference Clock Output as Time Base		
Expected Frequency (Hz)	Average Observed Frequency (Hz)	THD (%)	SINAD (dB)	Average Observed Frequency (Hz)	THD (%)	SINAD (dB)
500	499.9959	0.002	88.62	499.9965	0.00224	88.476
1000	999.9938	0.00224	88.368	999.9932	0.002	88.752
1500	1499.989	0.00208	88.332	1499.997	0.00192	88.308
10000	9999.915	0.002	82.164	9999.934	0.002	82.212

Tuning Reference Clock Output

The reference clock output has the ability to be tuned on-the-fly, and can be tuned in steps between a specified range. The range should be such that it ensures a swing of the sample rate, typically about ±0.2%, which is well below a range that might introduce audible artifacts. For example, a swing of ±0.2% of the data stream with a sample rate of 48 kHz requires a tuning of the reference clock output between the ranges of 12,263,424 Hz and 12,312,576 Hz.

Table 8 lists the required RODIV and ROTRIM values for tuning the sample rate within ±200 Hz of the sample rate. The required Master Clock column indicates that the sample rate to be tuned between the range of 47.9 kHz to 48.1 kHz, ROTRIM needs to be tuned between 459 to 468 and the required RODIV is 3. Similar tuning ranges for RODIV and ROTRIM to tune the reference clock output can be determined for other standard audio sample rates.

The tuning capability of REFCLKO prevents buffer underrun and overrun and alleviates the audible clicks, as discussed in **"USB Clock Mismatch"**.

TABLE 8: REFCLKO TUNING EXAMPLE WITH RODIV AND ROTRIM VALUES FOR 48 kHz AUDIO STREAM

LRCK (Hz)	MCLK (Hz)	Divisor	RODIV	ROTRIM
47800	12236800	3.922594	3	472
47810	12239360	3.921774	3	471
47820	12241920	3.920954	3	471
47830	12244480	3.920134	3	471
47840	12247040	3.919314	3	470
47850	12249600	3.918495	3	470
47860	12252160	3.917677	3	469
47870	12254720	3.916858	3	469
47880	12257280	3.91604	3	469
47890	12259840	3.915222	3	468
47900	12262400	3.914405	3	468
47910	12264960	3.913588	3	467
47920	12267520	3.912771	3	467
47930	12270080	3.911955	3	466
47940	12272640	3.911139	3	466
47950	12275200	3.910323	3	466
47960	12277760	3.909508	3	465
47970	12280320	3.908693	3	465
47980	12282880	3.907878	3	464
47990	12285440	3.907064	3	464
48000	12288000	3.90625	3	464
48010	12290560	3.905436	3	463
48020	12293120	3.904623	3	463
48030	12295680	3.90381	3	462
48040	12298240	3.902998	3	462
48050	12300800	3.902185	3	461
48060	12303360	3.901373	3	461
48070	12305920	3.900562	3	461
48080	12308480	3.89975	3	460
48090	12311040	3.898939	3	460
48100	12313600	3.898129	3	459
48110	12316160	3.897319	3	459
48120	12318720	3.896509	3	459
48130	12321280	3.895699	3	458
48140	12323840	3.89489	3	458
48150	12326400	3.894081	3	457
48160	12328960	3.893272	3	457
48170	12331520	3.892464	3	456
48180	12334080	3.891656	3	456
48190	12336640	3.890849	3	456
48200	12339200	3.890041	3	455

Legend: Shaded cells indicate Sample Rate Tuning Range values.

USB CLOCK MISMATCH

USB specifications require a tolerance budget and a limit on the USB clock frequency as a way to achieve immunity to radio interference. The USB clock with the allowed tolerance budget results in reduced audio quality if there is a USB clock mismatch.

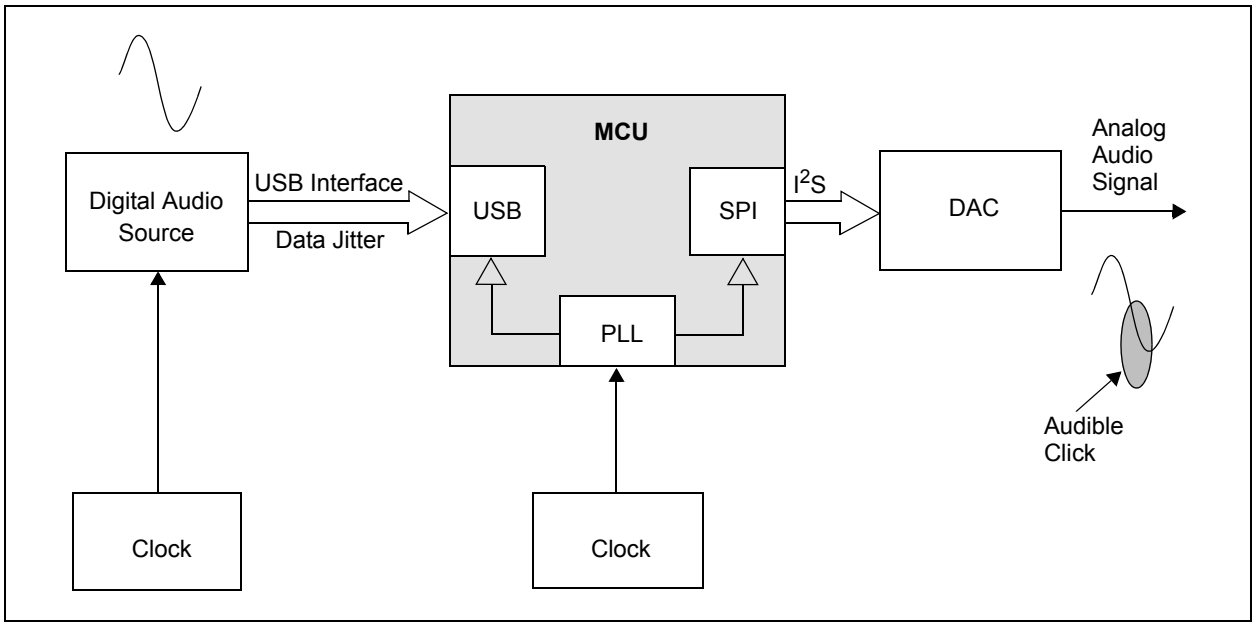
The real-time streaming audio samples must arrive at precise regular time intervals so that the DAC can convert the digital samples to an analog signal with the expected constant rate at which it is configured. The DAC clock that expects and receives the audio samples at a particular sample rate cannot miss even a single sample. A missing sample manifests as a subtle click for the listener, since the DAC fails to generate an accurate representation of the streamed audio signal. On a microcontroller or microprocessor with an embedded USB module, the USB clock is sourced from an independent clock such as an on-chip PLL with an external crystal oscillator of specific value. Since the clock is not sourced from the USB interface, the mismatch in clocks introduces buffer overrun or underrun, causing audible clicks as shown in Figure 10.

An easy solution for the audio data underrun or overrun issue as related to audio-quality degradation, is to use a good Asynchronous Sample Rate Converter (ASRC), where the input sample rate is estimated with jitter attenuation, and the internal filters are dynamically tuned for a new sample rate. However, a good ASRC is very expensive and the system still requires a DAC for analog conversion.

As an effective low-cost solution, the USB audio packets are buffered and the clocks of the codec or DAC can be tuned to prevent underrun or overrun using a feedback mechanism. The feedback mechanism monitors the buffer level and ensures it stays within an acceptable range, while achieving at least the same quality achieved by an expensive ASRC.

The reference clock output with USB-PLL clock as its source can be used to generate and tune the required master clock, as discussed in **"Tuning Reference Clock Output"**. This capability prevents buffer underrun and overrun while maintaining an acceptable DAC sample rate with a swing range of 0.2%. This is the lowest-cost solution compared to the other two while still achieving high-quality audio.

FIGURE 10: CLOCK JITTER DAC UNDERRUN OR OVERRUN MANIFESTING AS SUBTLE AUDIBLE CLICKS



PIC32 USB DIGITAL AUDIO ACCESSORY BOARD AND APPLICATION DEMONSTRATION

As an example, all of the features discussed in this application note are implemented in the PIC32 USB Headset application project available for the PIC32 USB Digital Audio Accessory Board. For more information about the board and the demonstration application, please visit www.microchip.com/pic32tools, and click the PIC32 USB Digital Audio Accessory Board link.

CONCLUSION

The SPI module with Audio mode and the USB On-The-Go (OTG) module in PIC32 devices can be used for high-quality audio applications.

The versatility and flexibility of the features on PIC32 32-bit MCUs can be used to deliver a professional audio-quality solution, while keeping the cost and power consumption low.

Key features of PIC32 devices in support of high-quality audio are:

- SPI module with I^2S and other data format modes,
- Ability to handle 16 and 24-bit stereo audio data streams
- Flexible reference clock output that can be used to generate the standard audio master clocks and can be tuned on-the-fly
- Loss of quality due to USB clock mismatch is addressed by tuning the sample rate
- USB OTG module provides the ability to stream digital audio

APPENDIX A: SOURCE CODE

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