AN1335

Phase-Shifted Full-Bridge (PSFB) Quarter Brick DC/DC Converter Reference Design Using a dsPIC® DSC

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ABSTRACT

This application note provides the digital implementation of a telecom input 36 VDC-76 VDC to output 12 VDC, 200W Quarter Brick DC/DC Brick Converter using the Phase-Shifted Full-Bridge (PSFB) topology. This topology combines the advantages of Pulse-Width Modulation (PWM) control and resonant conversion.

The dsPIC33F “GS” family series of Digital Signal Controllers (DSCs) was introduced by Microchip Technology Inc., to digitally control Switched Mode Power Converters. The dsPIC33F “GS” family of devices consists of an architecture that combines the dedicated Digital Signal Processor (DSP) and a microcontroller. These devices support all of the prominent power conversion technologies that are used today in the power supply industry.

In addition, the dsPIC33F “GS” family of devices controls the closed loop feedback, circuit protection, fault management and reporting, soft start, and output voltage sequencing. A DSC-based Switched Mode Power Supply (SMPS) design offers reduced component count, high reliability and flexibility to have modular construction to reuse the designs. Selection of peripherals such as the PWM module, Analog-to-Digital Converter (ADC), Analog Comparator, Oscillator and communication ports are critical to design a good power supply. MATLAB® based simulation results are compared to the actual test results and are discussed in subsequent sections.

INTRODUCTION

Recently, Intermediate Bus Converters (IBCs) have become popular in the telecom power supply industry. Most telecom and data communication systems contain ASIC, FPGAs and integrated high-end processors. These systems require higher currents at multiple low-level voltages with tight load regulations. Traditionally, bulk power supplies deliver different load voltages. In the conventional Distributed Power Architecture (DPA), the front-end AC/DC power supply generates 24V/48V and an individual isolated Brick Converter supports the required low system voltages. These systems become inefficient and costly where very low voltages are required. In the Intermediate Bus Architecture (IBA), the IBC generates 12V/5V. Further, these voltages are stepped down to the required load voltages by Point of Loads (PoLs).

In IBA, the high-density power converters, IBC and PoLs are near to the load points, which bring considerable financial gains with the improved performance. Because these converters are at the load points, PCB design will be simpler with reduction in losses.

Electromagnetic Interference (EMI) is also considerably reduced due to minimum routing length of high current tracks. Due to the position of these converters, the transient response is good and the system performance is improved. Modern systems require voltage sequencing, load sharing between the converters, external communication and data logging.

Conventional Switched Mode Power Supplies are designed with Analog PWM control to achieve the required regulated outputs, and an additional microcontroller performs the data communication and load sequencing. To maximize the advantages of IBC, the converter must be designed with reduced component count, higher efficiency, and density with lower cost. These requirements can be achieved by integrating the PWM controller, communication and load sharing with the single intelligent controller. The dsPIC33F “GS” family series of DSCs have combined these design features in a single chip that is suitable for the bus converters.

Some of the topics covered in this application note include:

- DC/DC power module basics
- Topology selection for the Quarter Brick DC/DC Converter
- DSC placement choices and mode of control
- Hardware design for the isolated PSFB Quarter Brick DC/DC Converter
- Planar magnetics design
- Digital PSFB Quarter Brick DC/DC Converter design
- Digital control system design
- Digitally controlled load sharing
- MATLAB modeling
- Digital nonlinear control techniques
- Circuit schematics and laboratory test results
- Test demonstration

FIGURE 1: DISTRIBUTED POWER ARCHITECTURE (DPA)

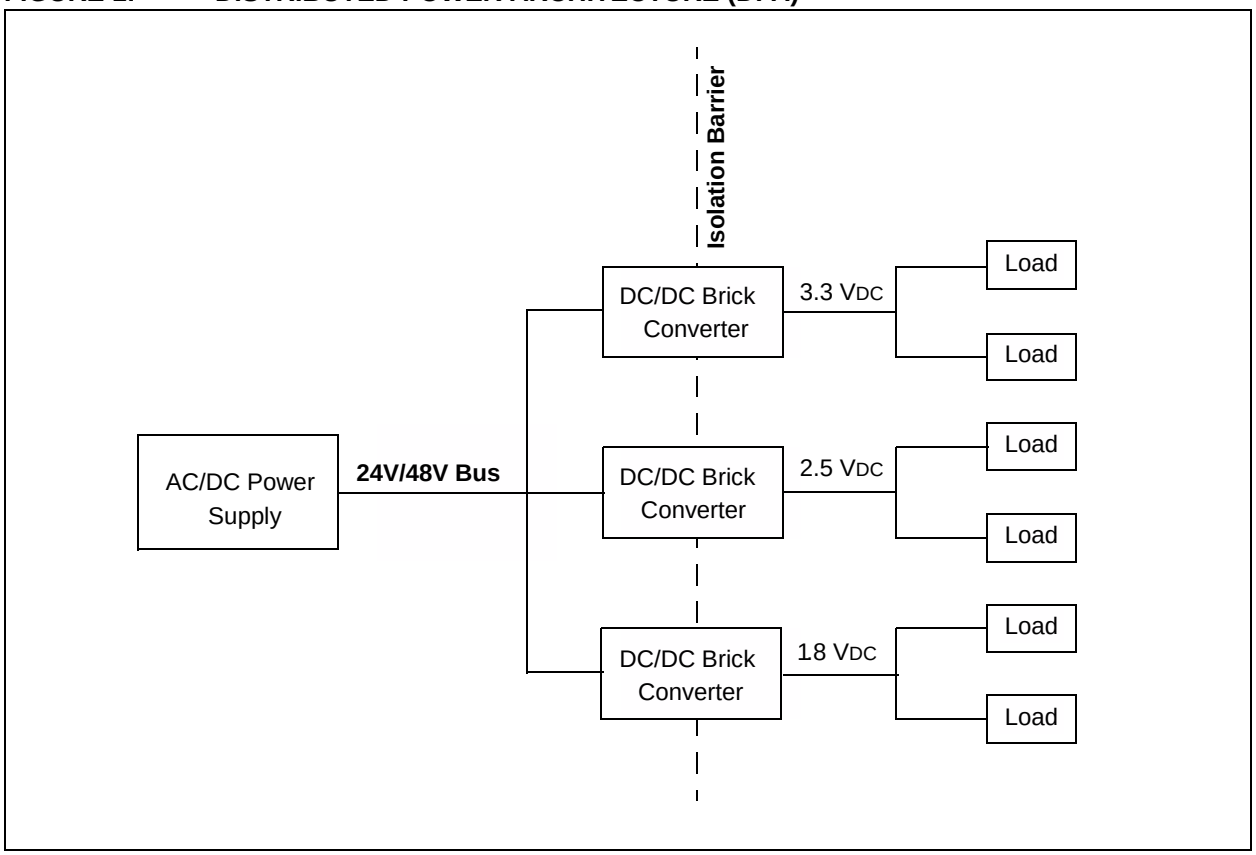
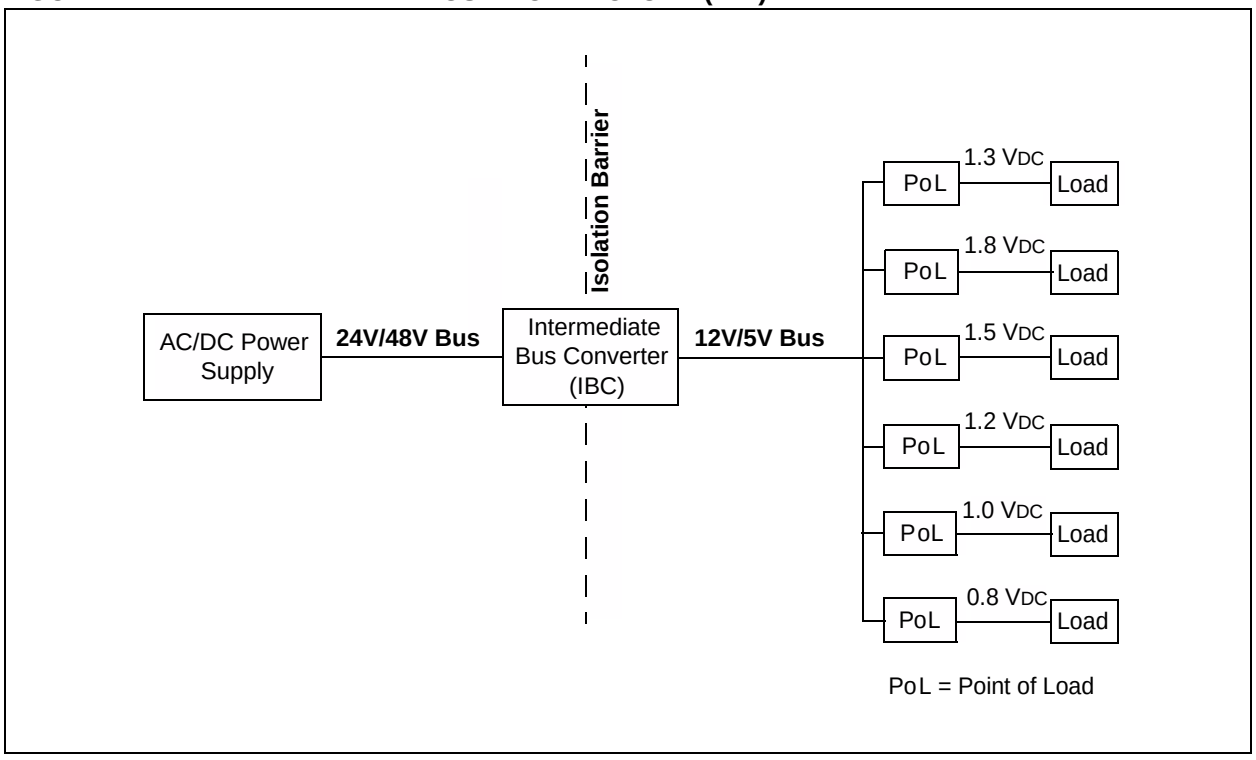


FIGURE 2: INTERMEDIATE BUS ARCHITECTURE (IBA)



QUARTER BRICK CONVERTER

The Distributed-Power Open Standards Alliance (DOSA) defines the specifications for the single output pin Quarter Brick DC/DC Converter. These specifications are applicable to all Quarter Bricks (unregulated, semi-regulated and fully regulated) for an output current range up to 50A.

The AC/DC converter output is 48V in the IBA. This voltage is further stepped down to an intermediate voltage of 12V by an isolated IBC. This voltage is further stepped down to the required low voltage using PoL.

DOSA Quarter Brick DC/DC converters are offered in through-hole configurations only.

Some advantages of the Quarter Brick Converter are:

- Improved dynamic response
- Highest packaging density
- Improved converter efficiency
- Isolation near the load end
- Output voltage ripple below the required limit

DC/DC POWER MODULES BASICS

Before discussing the design aspects of the Quarter Brick Converter, the following requirements should be understood:

- Input Capacitance
- Output Capacitance
- Remote ON/OFF Control
- Ripple and Noise
- Remote Sense
- Forced Air Cooling
- Overvoltage
- Overcurrent

Input Capacitance

For DC/DC converters with tight output regulation requirements, it is recommended to use an electrolytic capacitor of 1 µF/W output power at the input to the Quarter Brick Converter. In the Quarter Brick Converter designs, these capacitors are external to the converter.

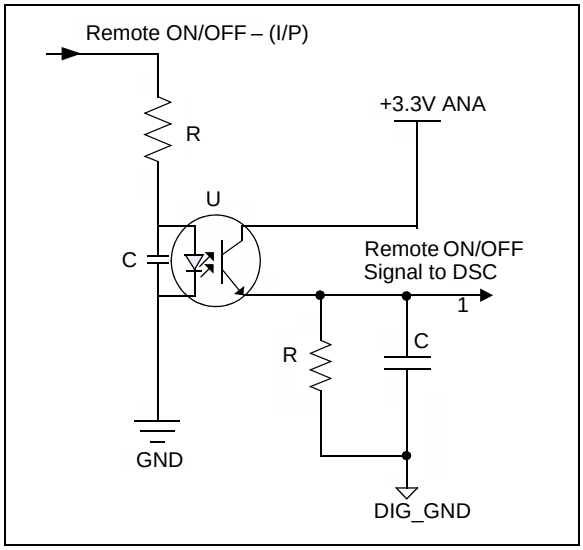
Output Capacitance

To meet the dynamic current requirements and the output voltage regulations at the load end, additional electrolytic capacitors must be added. As a design guideline, in Quarter Brick Converter designs, 100 µF/A to 200 µF/A of output current can be added and an effective lower Equivalent Series Resistance (ESR) can be achieved by using a number of capacitors in parallel.

Remote ON/OFF Control

Remote ON/OFF control is used to enable or disable the DC/DC converter through an external control signal. The most common method to enable or disable the converter is from the primary side (input side). Because the controller exists in the secondary side of the isolated barrier, an isolation circuit must be used to transfer the signal from the primary side to the secondary side. This can be achieved using the opto-isolator, which is illustrated in Figure 3.

FIGURE 3: REMOTE ON/OFF



Ripple and Noise

The output of a rectifier consists of a DC component and an AC component. The AC component, also known as ripple, is undesirable and causes pulsations in the rectifier output. Ripple is an artifact of the power converter switching and filtering action, and has a frequency of some integral multiple of the power converter operating switching frequency.

Noise occurs at multiples of the power converter switching frequency, and is caused by a quick charge and discharge of the small parasitic capacitances in the power converter operations. Noise amplitude depends highly on load impedance, filter components and the measurement techniques.

Remote Sense

Remote sense can be used to compensate voltage drop in the set voltage when long traces/wires are used to connect the load. In applications where remote sensing is not required, the sense pins can be connected to the respective output pins.

Forced Air Cooling

To remove heat from the high density board mount power supplies, forced air cooling is applied using a fan.

Forced air cooling greatly reduces the required PCB size and heat sink. However, installation of a fan consumes additional power, causes acoustic noise and also the maintenance requirements are significant.

In forced air cooling SMPS applications, reliability of the converter highly depends on the fan. A temperature sensing device is used to monitor the temperature and shuts down the converter when the Quarter Brick Converter exceeds the maximum operating temperature.

Overvoltage

Overvoltage protection is required to protect the load circuit from excessive rated voltage because of a malfunction from the converter's internal circuit. This protection can be implemented by Latch mode or Cycle-by-Cycle mode. In Latch mode, the circuit will be in the OFF condition on the occurrence of overvoltage fault until the input voltage is cycled. The system automatically recovers in the Cycle-by-Cycle mode. If faults still exist in the system, the system is turned OFF and this cycle is repeated.

Overcurrent

Overcurrent protection prevents damaging the converter from short circuit or overload conditions. In Hiccup mode, the converter will be OFF when an overcurrent or short circuit occurs, and will recover in the specified time period. If the converter still sees the fault, it will turn OFF the converter again and this cycle repeats. In the Latch mode, the circuit is recovered only after recycling the input power.

TOPOLOGY SELECTION

The bus converter specifications are standardized, and are used or assembled as one of the components in the final system. The user must consider the end-system characteristics such as reliability, efficiency, foot prints and cost. There is no universally accepted topology for the bus converters. However, the following sections describe a few topologies that are commonly used for DC/DC converter applications with their pros and cons.

A fundamental distinction among the PWM switching topologies is hard switching and soft switching/ resonant topologies. Typically, high frequency switching power converters reduce the size and weight of the converter by using small magnetics and filters. This in turn increases the power density of the converter. However, high frequency switching causes higher switching losses while the switch turns ON or OFF, which results in a reduction in the efficiency of the converter.

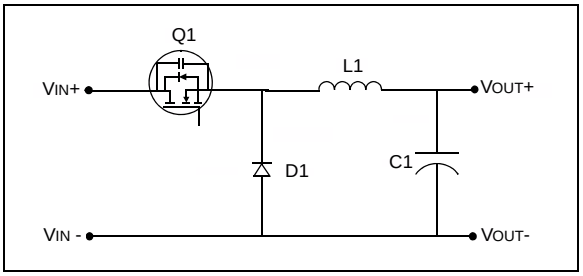
Soft switching techniques are used to reduce the switching losses of the PWM converter by controlling the ON/OFF switching of the power devices. Soft switching can be done using the Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) techniques. These soft switching techniques have some design complexity and in turn, produce higher efficiency at high-power levels.

Non-Isolated Forward Mode Buck Converter

If the required output voltage is always less than the specified input voltage, the Buck Converter can be selected from the following three basic topologies: Buck, Boost and Buck Boost.

The Buck topology can be implemented in the isolated and non-isolated versions. As per the bus converter specification requirement, isolated converter design is selected for this application. In the Forward mode Buck Converter, energy is transferred from the primary side to the secondary side when the primary side switch is turned ON. The output voltage can be controlled by varying the duty cycle with respect to the input voltage and load current. This is done with the feedback loop from the output that controls the duty cycle of the converter to maintain the regulated output.

FIGURE 4: NON-ISOLATED FORWARD MODE BUCK CONVERTER

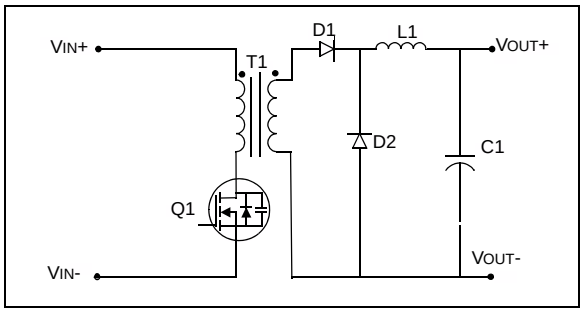


Isolated Forward Converter

In the Forward Converter, the energy from the input to the output is transferred when the switch Q1 is ON. During this time, diode D1 is forward biased and diode D2 is reverse biased. The power flow is from D1 and L1 to output. During the switch Q1 OFF time, the transformer (T1) primary voltages reverse its polarity due to change in primary current. This also forces the secondary of T1 to reverse polarity. Now, the secondary diode, D2 is forward biased and freewheels the energy stored in the inductor during switch Q1 ON time. This simple topology can be used for power levels of 100W. Some of the commonly used variations in Forward

Converter topologies are active Reset Forward Converter, Two Transistor Forward or Double-ended Forward Converter.

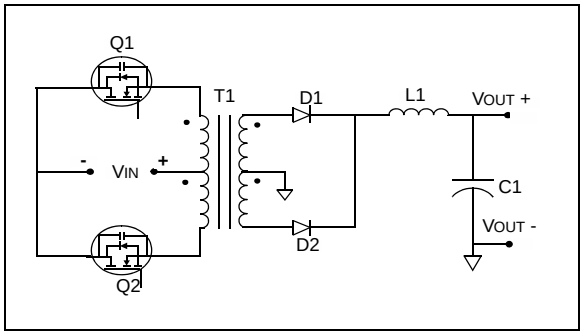
FIGURE 5: ISOLATED FORWARD CONVERTER



Push-Pull Converter

The Push-Pull Converter is a two transistor topology that uses a tapped primary on the converter transformer T1. The switches Q1 and Q2 conduct their respective duty cycles and the current in the primary changes, resulting in a bipolar secondary current waveform. This converter is preferred in low input voltage applications because the voltage stress is twice the input voltage due to the tapped primary transformer.

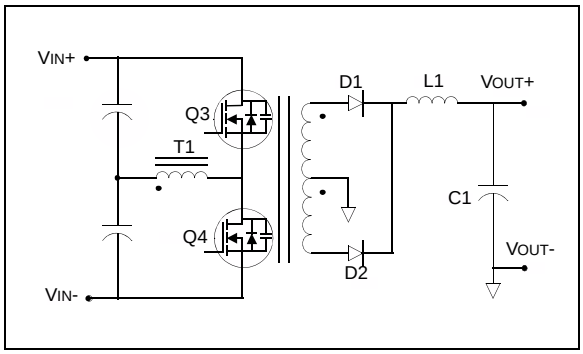
FIGURE 6: PUSH-PULL CONVERTER



Half-Bridge Converter

Half-Bridge converters are also known as two switch converters. Half the input voltage level is generated by the two input capacitors, C1 and C2. The transformer primary is switched alternatively between V_{IN}^{+} and input return V_{IN}^{-} such that the transformer primary sees only half the input voltage ($V_{IN}/2$). The input switches, Q1 and Q2, measure the maximum input voltage, V_{IN} compared to 2 * V_{IN} in the Push-Pull Converter. This allows the Half-Bridge Converter to use higher power levels.

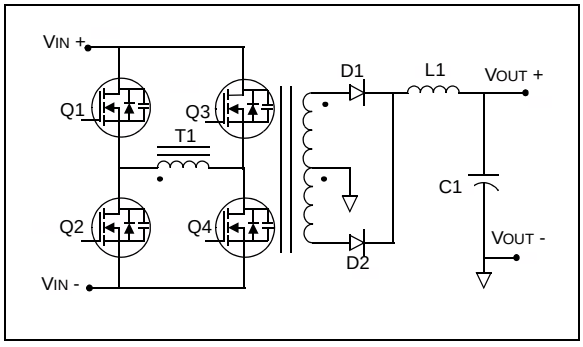
FIGURE 7: HALF-BRIDGE CONVERTER



Full-Bridge Converter

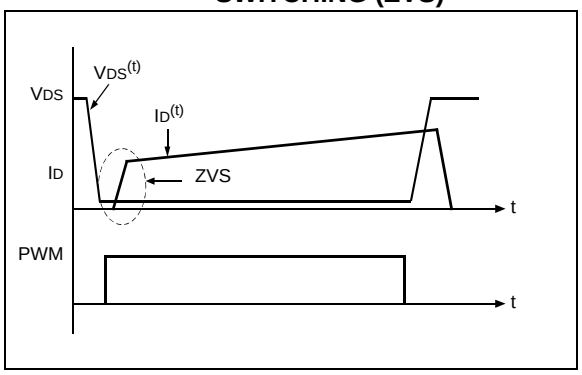
The Full-Bridge Converter is configured using the four switches: Q1, Q2, Q3 and Q4. The diagonal switches Q1, Q4 and Q2, Q3 are switched ON simultaneously. This provides full input voltage (V_{IN}) across the primary winding of the transformer. During each half cycle of the converter, the diagonal switches Q1, Q4 and Q2, Q3 are turned ON, and the polarity of the transformer reverses in each half cycle. In the Full-Bridge Converter, at a given power compared to the Half-Bridge Converter, the switch current and primary current will be half. This makes the Full-Bridge Converter suitable for high-power levels.

FIGURE 8: FULL-BRIDGE CONVERTER



However, the diagonal switches are hard switched resulting in high turn ON and turn OFF switching losses. These losses increase with frequency, which in turn limits the frequency of the operation. To overcome these losses, the PSFB converter is introduced. In this topology, the switch turns ON after discharging the voltage across the switch. This eliminates the turn ON switching losses.

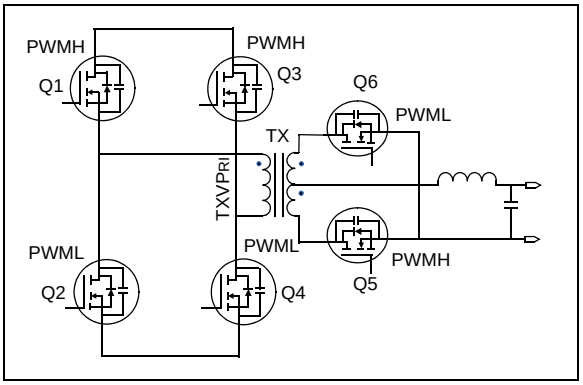
FIGURE 9: ZERO VOLTAGE SWITCHING (ZVS)



Synchronous Rectification

In synchronous rectification, the secondary diodes, D1 and D2 are replaced with MOSFETs. This yields lower rectification losses because a MOSFET will have minimum DC losses compared to the Schottky rectifiers. The forward DC losses of a Schottky rectifier diode will be forward voltage drop multiplied by the forward current. The power dissipation by a conducting MOSFET will be $R_{DS(ON)}$ multiplied by the square of the forward current. The loss comparison will be significant at considerably higher current >15A and lower output voltages.

FIGURE 10: FULL-BRIDGE CONVERTER WITH SYNCHRONOUS RECTIFICATIONS



This configuration involves complexity and cost to an extent because a gate drive circuit is required to control the synchronous MOSFET. The efficiency of this configuration can be further increased by designing the complex gate drive signals, which are discussed in the section **"Digital Nonlinear Implementations"**.

Many topologies are available and one of them can be chosen depending on the given power level, efficiency of the converter, input voltage variations, output voltage levels, availability of the components, cost, reliability of the design, and good performance characteristics.

With the discussed advantages for the topologies and efficiency considerations, the PSFB topology was selected for the Quarter Brick DC/DC Converter design. The operation, design and performance of this topology is discussed in following sections.

TABLE 1: TOPOLOGY COMPARISON

Topology	No. of Switches in the Primary	Stress Level of Primary Switches	Power Levels (Typical)
Forward converter	2	V_{IN}	100W
Push-Pull converter	2	2 * V_{IN}	150W
Half-Bridge converter	2	V_{IN}	200W
Full-Bridge converter	4	V_{IN}	~ 200W
PSFB converter	4	V_{IN}	~ 200W

PRIMARY SIDE CONTROL VS. SECONDARY SIDE CONTROL

After selecting the topologies based on the merits for the given application, the next challenge faced by designers is to position the controller either on the primary or secondary side. The power converter demands the galvanic isolation between primary (input) and secondary (output load) due to safety reasons. There should not be any direct conductive path between the primary and secondary.

Isolation is required when signals are crossing from the primary to the secondary and vice versa. The power path isolation will be given by the high frequency transformers. Gate drive signals can be routed through optocouplers or gate drive transformers.

In the primary side controllers, the output feedback signal is transferred from the secondary to the primary using the optocouplers. These devices have limited bandwidth, poor accuracy, and tend to degrade over time and temperature.

Again, the transfer of signals from the primary to the secondary or the secondary to the primary is dependant on the features demanded by the application. Figure 11, Figure 12 and Table 2 show the comparison between the primary side controller and the secondary side controller. The secondary side controller is selected in this application.

FIGURE 11: SECONDARY SIDE CONTROL

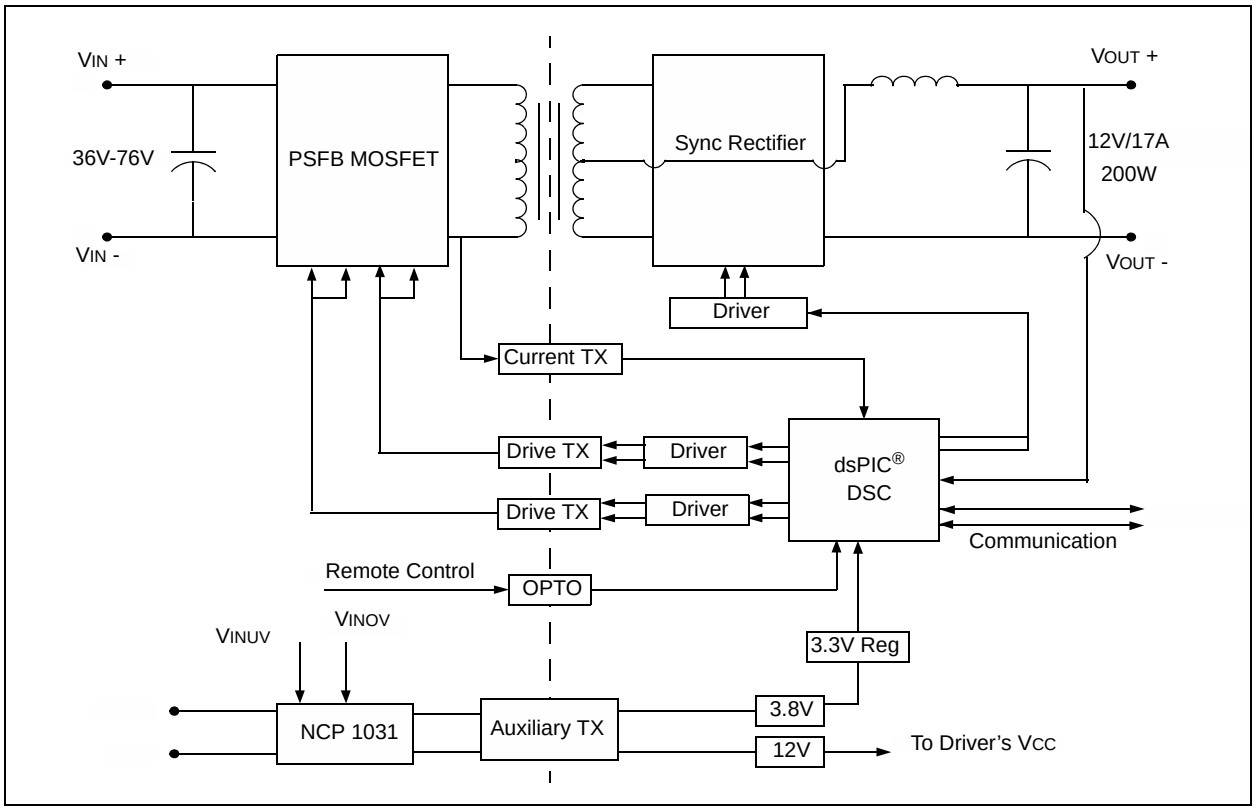
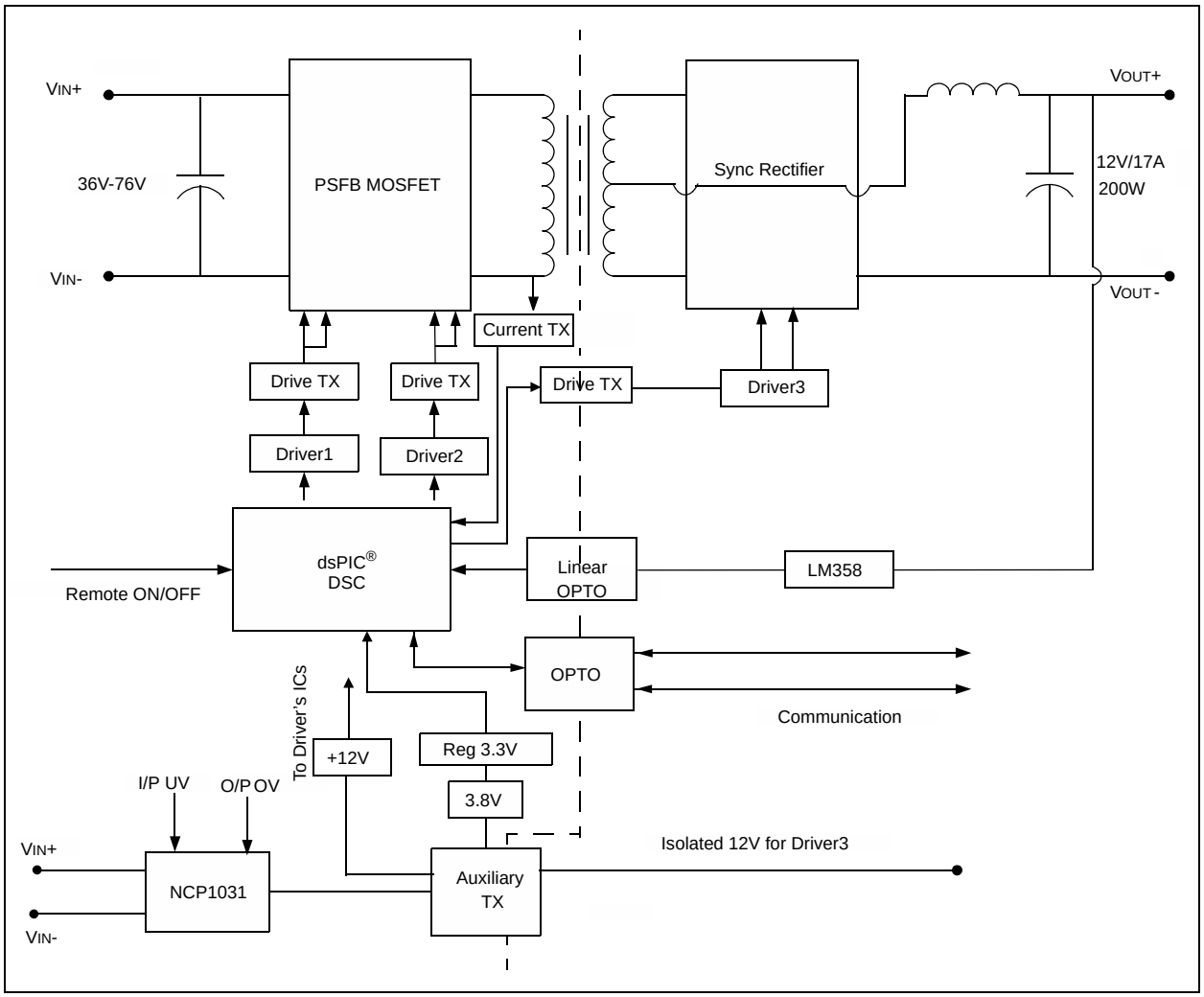


TABLE 2: PRIMARY SIDE CONTROL VS. SECONDARY SIDE CONTROL

Primary Side dsPIC® DSC Control	Secondary Side dsPIC® DSC Control
Isolated feedback is required to regulate the output. A linear optocoupler can be used to achieve the regulation, which requires an auxiliary supply and an amplifier in the secondary.	Isolated feedback is not required because the controller is on the secondary.
Remote ON/OFF signal isolation is not required.	Remote ON/OFF signal isolation is required.
Isolation is required for communication signals.	Isolation is not required for communication signals.
Load sharing signal is transferred from the secondary to the primary.	Load sharing isolation is not required because the controller is in the secondary.
Overvoltage protection signal is transferred from the secondary to the primary.	Isolation for overvoltage is not required because the controller is in the secondary.
Frequency synchronization signal is transferred from the secondary to the primary.	Isolation for frequency synchronization is not required because the controller is in the secondary.
Input undervoltage and overvoltage can be measured without isolation.	Isolation is required. However, in this application, the input undervoltage or overvoltage protection is provided by the NCP 1031 auxiliary converter controller.
Gate drive design for the primary side switches is simple.	Gate drive is transferred from the secondary to the primary either by using driver transformers or opto isolators.

FIGURE 12: PRIMARY SIDE CONTROL



VOLTAGE MODE CONTROL (VMC) VS. CURRENT MODE CONTROL (CMC)

The preference to implement VMC or CMC as the feedback control method is based on application-specific requirements. In VMC, change in load current will have effect on the output voltage before the feedback loop reacts and performs a duty cycle correction. In CMC, change in load current is sensed directly and corrects the loop before the outer voltage loop reacts.

This cause and then react process in the VMC is slower to respond than in the CMC for highly varying load transients.

The fundamental difference between VMC and CMC is that CMC requires accurate and high grade current sensing. In VMC, output voltage regulation is independent of the load current. Therefore, relatively low grade current sensing is enough for overload protection. This saves significant circuit complexity and power losses.

TABLE 3: VMC AND CMC DIFFERENCES

VMC	CMC
Single feedback loop.	Dual feedback loop.
Provides good noise margin.	Poor noise immunity.
Current measurement not required for feedback.	Current measurement required.
Slope compensation not required.	Slope compensation required, instability at more than 50% duty cycles.
Poor dynamic response.	Good dynamic response.

FIGURE 13: VOLTAGE MODE CONTROLLER (VMC)

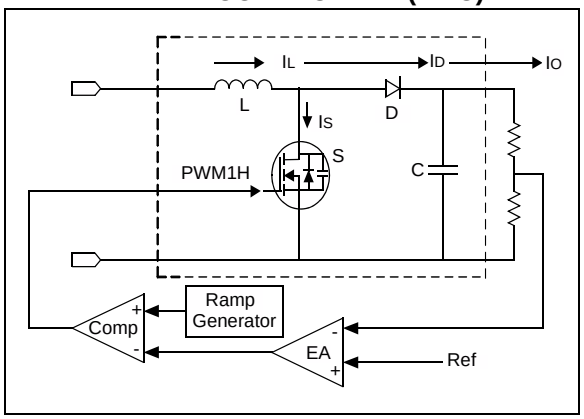
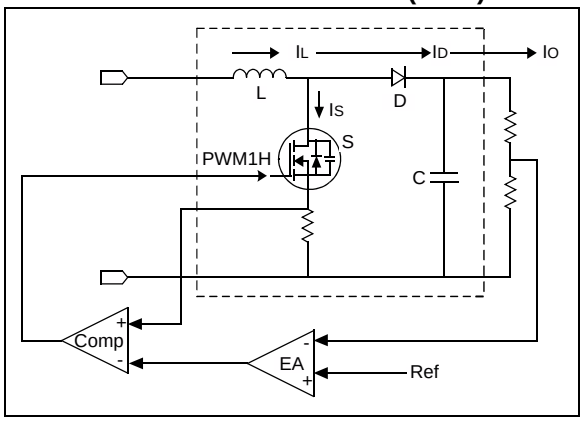


FIGURE 14: CURRENT MODE CONTROLLER (CMC)



HARDWARE DESIGN FOR THE ISOLATED QUARTER BRICK DC/DC CONVERTER

The average Current mode control PSFB topology with secondary side controller was selected for this design. The digital Quarter Brick DC/DC Converter design is discussed in the following sections.

Phase-Shifted Full-Bridge (PSFB) Converter Design

High switching frequency and high voltage stress on the primary side transistors produce switching losses. PSFB transformer isolated buck converter attains zero voltage transition (ZVT) without increasing the MOSFET's peak voltage stress.

In Figure 15, MOSFET (Q1-Q4), body diodes (D1-D4) output capacitance ($C_{OSS}1$-$C_{OSS}4$) leakage inductance of the transformer are illustrated. Leakage inductance causes the full-bridge switching network to drive an effective inductive load, and results in ZVT on the primary side switching devices.

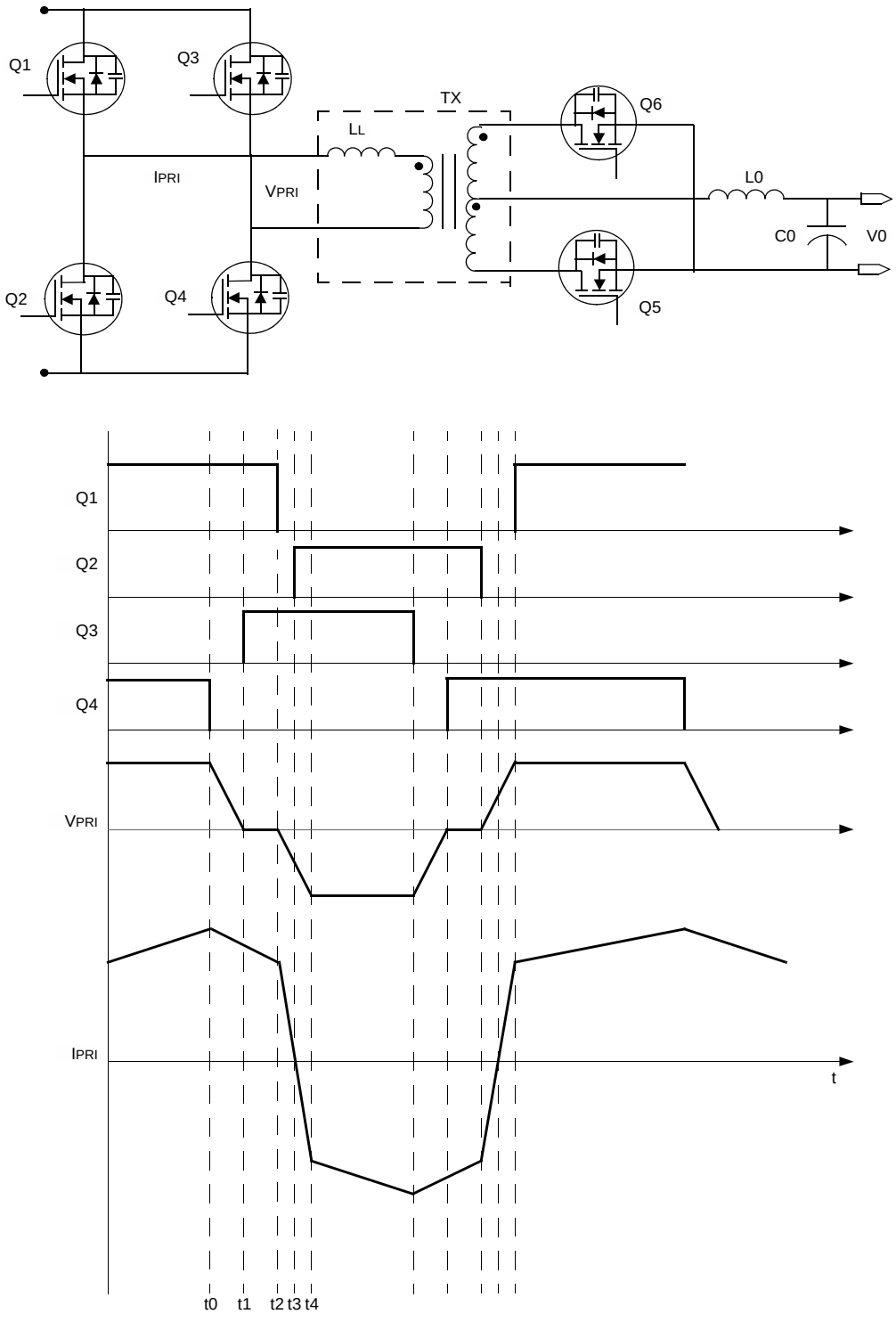
The output voltage is controlled through a phase shift between the two half-bridge. Both halves of the bridge switch network operate with a 50% duty cycle and the phase difference between the half-bridge switch networks is controlled. A maximum duty cycle of 50% ensures that the gate drive transformer and gate drive circuit design will be simple.

The ZVT is load related and at some minimum load, the ZVT will be lost. Linear output voltage control can be achieved by controlling the phase shift between the right leg and left leg of the bridge configuration.

In ZVT, the switches are turned ON when the voltage seen by the switches are zero, resulting in no switch ON losses. Phase shift control of a Full-Bridge Converter can provide ZVT in the primary side which results in lower primary side switching losses and lower EMI losses.

Operation of the PSFB converter and detailed primary side waveforms with different time intervals are illustrated in Figure 15.

FIGURE 15: PSFB CONVERTER WITH FULL WAVE SYNCHRONOUS RECTIFICATION-OPERATIONAL WAVEFORMS



- **Initial Conditions t0:** Q1 = ON; Q4 = ON; Q2 = OFF; Q3 = OFF

The PSFB converter operation is described with the power transfer from primary side to secondary side with the conduction of diagonal switches, Q1 and Q4. The primary side current (I_{PRI}) was conducting through the switches, Q4 and Q1, but in this period, the full input voltage V_{IN} is across the primary side of the transformer TX and V_{IN}/N is across the secondary of the transformer. The slope of the current is determined by V_{IN}, magnetizing inductance and the output inductance.

- **Time interval t0 to t1:** Q1 =ON; Q4 = OFF; Q2 =OFF; Q3 = OFF

Switch Q4 is turned OFF and Switch Q1 remains ON, the primary current continues to flow taking the Q4 switch output capacitor C4. This charges the capacitor C4 to V_{IN} from 0V, at the same time the capacitor C3 of Switch Q3 is discharged because its source voltage rises to input voltage V_{IN}. This transition puts Q3 with no drain to source voltage prior to turn ON and ZVS can be observed. Therefore there will not be any turn ON switching losses. During this transition period, the primary voltage of the transformer decreases from V_{IN} to zero, and the primary no longer supplies power to the output. Simultaneously, the energy stored in the output inductor starts supplying the decaying primary power.

- **Time interval t1 to t2:** Q1 = ON; Q3 = ON; Q4 = OFF; Q2 =OFF; D3 = ON

After Q3 output capacitance is charged to full input voltage V_{IN}, the primary current free wheels through switch Q1 and body diode D3 of switch Q3. The current remains constant until the next transition occurs. Q3 can be turned ON any time after t1 and the current shares between the body diode D3 and the switch Q3 channel.

- **Time interval t2 to t3:** Q3 = ON; Q1 = OFF; Q4 = OFF; Q2 =OFF;

At time t2, Q1 is turned OFF, the primary current continues to flow through the body diode, D1 of the switch Q1. The direction of the current flow increases the switch Q1 source to drain voltage, and voltage across the switch Q2 decreases from high to lower voltage. During this transition, the primary current decays to zero. ZVS of the left leg switches depending on the energy stored in the resonant inductor, conduction losses in the primary switches and the losses in the transformer winding. Because the left leg transition depends on leakage energy stored in the transformer, it may require an external series inductor if the stored leakage energy is not enough for ZVS. When Q2 is then turned ON in the next interval, voltage VIN is applied across the primary in the reverse direction.

- **Time interval t3 to t4:** Q3 = ON; Q2 = ON; Q1 = OFF; Q4 = OFF;

In this time interval, both the diagonal switches Q3 and Q2 are ON and input voltage V_{IN} is applied across the primary of transformer. The rate of rise of the current is determined by the input voltage V_{IN}, magnetizing inductance and the output inductance. However, the current flows at negative value as opposed to zero. Now, the current flowing through the primary switches is the magnetizing current along with the reflected secondary current into the primary.

The input voltage, the transformer turns ratio and output voltage determine the exact diagonal switch ON time. After the switch-on time period of the diagonal switches, Q3 is turned OFF at t4. One switching cycle is completed when the switch Q3 is turned OFF and the resonant transition to switch Q4 starts.

In the PSFB converter, the left leg transition requires more time than the right leg transition to complete. The maximum transition time occurs for the left leg at minimum load current and maximum input voltage, while minimum transition time occurs for the right leg at maximum load current and minimum input voltage.

To achieve ZVT for all the switches, the leakage inductor must store sufficient energy to charge and discharge the output capacitance of the switches in the allocated time. The energy stored in the inductor must be greater than the capacitive energy required for the transition.

HARDWARE DESIGN AND SELECTION OF COMPONENTS

Selection of components for a quarter brick converter design is critical to achieve high efficiency and high density.

Specifications

- Input voltage: V_{IN} = 36 V_{DC}-76 V_{DC}
- Output voltage: V_O = 12V
- Rated output current: I_{ORATED} = 17A
- Maximum output current: I_O= 20A
- Output power: P_O = 200W
- Estimated efficiency: 95%
- Switching frequency of the converter: F_{SW} = 150 kHz
- Switching period of the converter: T_P = 1/150 kHz = 6.66 µs
- Chosen duty cycle: D = 43.4%
- Full duty cycle: D_{MAX} = 2 * 43.4% = 86.8%
- Input power pin = 214.75W

EQUATION 1: TURN ON TIME

$$TurnOnTime = 6.66\mu s \times \frac{43.4}{100} = 2.89\mu s$$

PSFB MOSFET Selection

EQUATION 2:

Input line current at 36V

$$I_{AVE} = \frac{P_{IN}}{V_{INMIN}} = 5.96A$$

Maximum Line Current at 36V

$$I_{MAX} = \frac{I_{AVE}}{D_{MAX}} = \frac{5.96}{0.868} = 6.87A$$

Line rms current at 36V

$$I_{RMS} = I_{MAX} \times \sqrt{D} = 6.40A$$

Switch rms current at 36V

$$I_{SRMS} = I_{MAX} \times \sqrt{\frac{D}{2}} = 4.53A$$

Because the maximum input voltage is 76 VDC, select a MOSFET voltage rating that is higher than 76V and the current rating higher than IMAX at 36 VDC.

The device selected is Renesas HAT2173 (LFPAK), and has VDS 100V, ID 25A, RDS(ON) 0.015E.

RDS(ON) HOT can be calculated either from the graphs provided in the data sheet or by using the empirical formula shown in Equation 3.

EQUATION 3: RDS(ON) EMPIRICAL FORMULA

$$R_{DS(ON)}\,HOT = R_{DS(ON)\,@\,25} * [1+0.0075*(T_{MAX}-T_{AMB})]$$

$$R_{DS(ON)}\,HOT = 0.02625E$$

where:

$R_{DS(ON)}$ at 25 = 0.015E

Maximum junction temperature, $T_{MAX} = 125^oC$

Ambient temperature, $T_{AMB} = 25^oC$

EQUATION 4:

Conduction losses of the MOSFET at 48V:

$$P_{COND} = I^2_{SRMS} \times R_{DS(ON)}HOT = 0.171W$$

where:

I_{SRMS} = Switch rms current

Conduction losses of all the four PSFB MOSFETs = 0.687W

EQUATION 5: SWITCHING LOSSES OF MOSFET

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_{SRMS} \times T_F \times F_{SW} = 0.05W$$

where:

T_F = Fall time of the MOSFET = 5.7ns

Switching losses of all the four PSFB MOSFETs = 0.21W

In the ZVT, MOSFETs have only turn OFF switching losses.

EQUATION 6: MOSFET GATE CHARGE LOSS

$$MOSFETGateChargeLosses = Q_G \times F_{SW} \times V_{DD} = 0.126W$$

where:

For all the four PSFB MOSFETs = 0.504W

Bias voltage to the gate drive, V_{DD} = 12V

MOSFET total gate charge Q_G = 70 ns

Synchronous MOSFET Selection

The ability of the MOSFET channel to conduct current in the reverse direction makes it possible to use a MOSFET where a fast diode or Schottky diode is used. In the fast diodes, junction contact potential limits to reduce the forward voltage drop of diodes. Schottky diodes will have reduced junction potential compared to the fast diode. In the MOSFETs, the conduction losses will be $R_{DS(ON)} * I^2_{RMS}$. The on-resistance can be decreased by using parallel MOSFETs; this will reduce the losses further significantly.

When full wave center tapped winding is used in the transformer secondary side, the MOSFET voltage stress is twice the output voltage, as shown in Equation 7.

EQUATION 7: MOSFET VOLTAGE STRESS

$$MOSFETVoltageStress = 2 \times (V_O + V_{FET} + V_{DROP})$$
$$= 2 \times (12 + 0.6 + 0.2)$$
$$= 25.6V$$

where:

Secondary MOSFET Drop, V_{FET} = 0.6V

Total Trace Drops, V_{DROP} = 0.2V

This is the minimum voltage stress, seen by the MOSFET when the lower input voltage is 36V. For the maximum input voltage of 76V, the stress is as shown in Equation 8.

EQUATION 8:

$$MOSFET\ Voltage\ Stress\ @\ 76V = 76 \times \frac{25.6}{36} = 54.04V$$

The device selected is Renesas HAT2173 (LFPAK).

Transformer Design

DESIGN CONSIDERATIONS FOR RESONANT TANK CIRCUIT ELEMENTS

Design of resonant tank is critical to achieve ZVT. Resonant capacitor (CR) and resonant Inductor (LR) forms resonant tank. A factor of 4/3 is multiplied to the Output Capacitance of MOSFET (COSS) to accommodate the increase in capacitance with voltage, and a factor of two is also multiplied because two output capacitances (COSS) will come in parallel in each resonant transition.

EQUATION 9:

$$TotalResonantCapacitance, C_R = \frac{4}{3} \times 2 \times C_{OSS} + C_{TX}$$
$$= \frac{8}{3} \times C_{OSS} + C_{TX}$$
$$= 1.387nF$$

where:

C_{OSS} = Output capacitance of the MOSFET
= 5.20E-10F

C_{TX} = Transformer capacitance (neglected)

$$ResonantTankFrequency, F_R = \frac{1}{2\pi\sqrt{L_R \times C_R}}$$

where:

L_R = Transformer leakage inductance + Additional leakage inductance

The maximum transition cannot exceed one-fourth of the resonant period to gain the ZVT.

EQUATION 10: TTRANSMAX

$$MaximumTransitionTime, T_{TRANSMAX} = \frac{\pi}{2} \cdot \sqrt{(L_R \cdot C_R)}$$

The capacitive energy required to complete the transition, ECR is shown in Equation 11.

EQUATION 11:

$$E_{CR} = \frac{1}{2} \times C_R \times (V_{INMAX})^2$$

where:

$V_{IN\ MAX}$ = maximum input voltage

The energy stored in the resonant inductor LR must be greater than the energy required to charge and discharge the COSS of the MOSFET and transformer capacitance CTX of the leg transition within the maximum transition time.

The energy stored in the resonant inductor (LR), is as shown in Equation 12.

EQUATION 12: ENERGY STORED IN THE RESONANT INDUCTOR (LR)

$$E_{LR} = \frac{1}{2} \times L_R \times I^2_{PRI}$$

The slope of the primary current during transition is as shown in Equation 13.

EQUATION 13:

$$\frac{V_P}{L_R} = \frac{I_{PRI}}{T_{TRANS}}$$

$$MaximumPrimaryCurrent, I_{PRI} = \frac{N_S}{N_P} \times I_O$$
$$= 6.8A$$

where:

I_O = Output current

N_P = TX primary turns = 5

N_S = TX secondary turns = 2

V_P = Input voltage = 32.5V

F_{SW} = Converter switching frequency

T_P = Switching period = $1/F_{SW}$

Resonant transition estimated $T_{TRANS} = 0.15 * T_P$

EQUATION 14: T_{TRANS}

$$T_{TRANS} = 2 \times I_{PRI} \times \frac{L_R}{V_P}$$

Two transitions per period. Hence, multiplied with 2.

EQUATION 15: L_R

$$L_R = \frac{T_{TRANS}}{2} \times \frac{V_P}{I_{PRI}}$$

$$L_R = 2.3\mu H$$

The energy stored in the inductor, ELR must be greater than the capacitive energy, ECR, which is required for the transition to occur within the allocated transition time.

EQUATION 16:

$$E_{LR} > E_{CR} = \frac{1}{2} \times L_R \times I^2_{PRIMIN} > \frac{1}{2} \times C_R \times V^2_{INMAX}$$

$$I_{PRIMIN} > \sqrt{C_R \times \frac{(V_{IN})^2}{L_R}} = 0.88A$$

Magnetics Design

Magnetics design also plays a crucial role in achieving high efficiency and density. In the Quarter Brick DC/DC Converter design, planar magnetics are used to gain high efficiency and density.

DESIGN OF PLANAR MAGNETICS

Planar magnetics are becoming popular in the high density power supply designs where the winding height is the thickness of the PCB. Planar magnetics design can be constructed stand-alone with a stacked layer design or as a small multi-layer PCB or integrated into a multi-layer board of the power supply.

The advantages of planar magnetics are:

- Low leakage inductance
- Very low profile
- Excellent repeatability of performance
- Economical assembly
- Mechanical integrity
- Superior thermal characteristics

Planar E cores offer excellent thermal resistance. Under normal operating conditions, it is less than 50% as compared to the conventional wire wound magnetics with the same effective core volume, VE. This is caused by the improved surface to the volume ratio. This results in better cooling capability and can handle higher power densities, while the temperature is within the acceptable limits.

The magnetic cross section area must be large to minimize the number of turns that are required for the given application. Ensure that the core covers the winding that is laid on the PCB. Such design types reduce the EMI, heat dissipation and allow small height cores. Copper losses can be reduced by selecting the round center leg core because this reduces the length of turns.

The Planar Magnetics design procedure is the same as that of the wire wound magnetics design:

1. Select the optimum core cross-section.
2. Select the optimum core window height.
3. Iterate turns versus duty cycle.
4. Iterate the core loss.
5. Iterate the copper loss (Cu).
6. Evaluate the thermal methods.
7. Estimate the temperature rise.
8. What is the cost trade-off versus the number of layers.
9. Does the mechanical design fit the envelope and pad layout?
10. Fit within core window height.
11. Is the size sufficient for power loss and thermal solution?

Full-Bridge Planar Transformer Design

The two considerations for secondary rectifications are Full Wave Center Tapped (FWCT) rectifier configuration and Full Wave Current Doubler rectifier configurations. It is observed that the FWCT rectifier makes optimum use of board space and efficiency goals. Preliminary testing has validated this conclusion.

A further optimization goal is to offer a broad operating frequency from 125 kHz to 200 kHz to provide wide latitude for customers to optimize efficiency.

The input voltage range is 36 VDC-76 VDC nominal with extended VINMIN OF 32.5 VDC.

Analysis of the transformer design begins with the given input parameters:

- VIN = 36V
- Frequency = 150 kHz
- TP = 6.667 x 10^{-6}

The intended output voltage was meant to supply a typical bus voltage for distributed power applications and the output voltage. VO = 12.00V and the maximum output load current, IO = 25A

No substitute exists for the necessary work to perform calculations sufficient to evaluate a particular core size, turns, and core and copper losses. These must be iterated for each design. One of the design considerations is to maximize the duty cycle, but the limitation of resolution offered by integer turns will quickly lead to the turn ratio of NP = 5 and NS = 2.

In the design of the magnetics, users must select the minimum number of turns. There is a cost or penalty to placing real-world turns on a magnetic structure such as, resistance, voltage drop and power loss. Therefore, use the least number of integer turns possible.

Thereafter, a reasonable assessment for turn ratio, duty cycle, peak flux density, and core loss can be done until a satisfactory point is reached for the designer.

The duty cycle (more than each half-period) to produce the desired output is as follows:

- T_{ON} = 2.89 µs
- D = T_{ON}/T_P = 0.434

Over a full period, the duty cycle is 86.8% at a V_{IN} of 36 V_{DC}.

In this design, the following regulation drops are used:

- Secondary MOSFET drop, $V_{FET\ SEC}$ = 0.1V
- Total trace drops, V_{DROP} = 0.2V
- Primary MOSFET drop, $V_{FET\ PRI}$ = 0.6V

EQUATION 17:

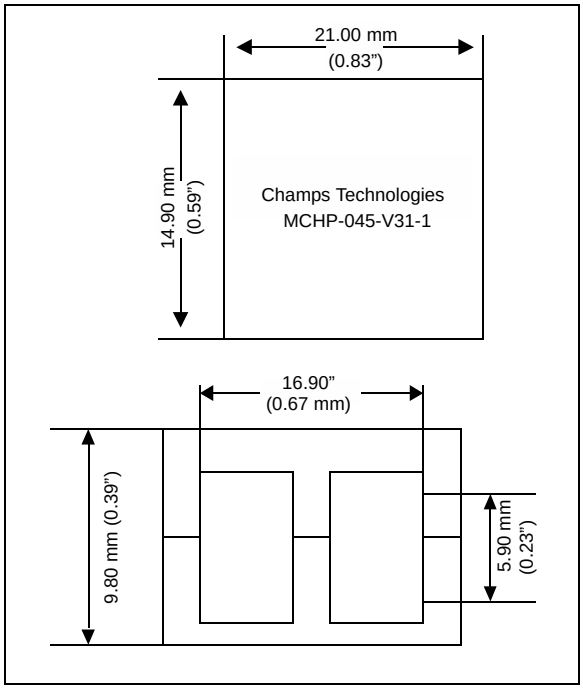
$$V_O = \left[(V_{IN} - V_{FETPRI}) \times \frac{N_S}{N_P} - V_{FETSEC} - V_{DROP} \right] \times 2D$$
$$= 12.03V$$

The iteration method is followed again to select the core size from the available cores.

The selected core has the following magnetic parameters:

- A_C = 0.45 cm^2
- L_E = 3.09 cm
- V_E = 1.57 cm^3

FIGURE 16: PLANAR TRANSFORMER



This core shape is a tooled core and is available from the Champs Technologies. In general, a power material in the frequency range of interest must be considered. Materials such as 2M, 3H from Nicera™, the PC95 from TDK™, or the 3C96, 3C95 from Ferroxcube™ are the most recommended options. The peak-to-peak and rms flux densities arising from this core choice are shown in Equation 18.

EQUATION 18:

$$B_{PKPK} = \frac{(V_{IN} \times t_{ON}) \times 10^8}{N_P \times A_C}$$

$$B_{PKPK} = 4.624 \times 10^3 Gauss$$

$$B_{RMS} = \sqrt{\frac{2}{T_P} \times \int_O^{t_{ON}} \left[\frac{(V_{IN} \times t_{ON}) \times 10^8}{2 \times N_P \times A_C} \right]^2 dT}$$

$$B_{RMS} = 2.153 \times 10^3 Gauss$$

The power loss density is calculated using the parameters shown in Table 4.

TABLE 4: FIT PARAMETERS TO CALCULATE THE POWER LOSS DENSITY

Material	f (kHz)	Cm	x	y	Ct2	Ct1	Ct0
3C92	20-100	26.500	1.19	2.65	2.68E-04	5.43E-02	3.75
	100-200	0.349	1.59	2.67	1.51E-04	3.05E-02	2.55
	200-400	1.19E-04	2.24	2.66	2.08E-04	4.37E-02	3.29
3C96	20-100	5.120	1.34	2.66	5.48E-04	1.10E-01	6.56
	100-200	8.27E-02	1.72	2.80	1.83E-04	3.66E-02	2.83
	200-400	9.17E-05	2.22	2.46	2.33E-04	4.72E-02	3.39
3F35	400-1000	1.23E-08	2.95	2.94	1.38E-04	2.41E-02	2.03

Note: Source – New ER Cores for Planar Converters, Ferroxcube™ Publication 939828800911, Sept. 2002.

Core loss density can be approximated by the formula shown in Equation 19. The core constants are made available by Ferroxcube™. In this design:

- Temp = 50°C
- Frequency = 150000 Hz
- B = B_{RMS} * 10^{-4} = 0.2153 Tesla
- x =1.72
- y = 2.80
- Ct2 = 1.83 * 10^{-4}
- Ct1 = 3.66 * 10^{-2}
- Ct0 = 2.83
- Cm = 8.27 * 10^{-2}

EQUATION 19: CORE LOSS DENSITY

$$\text{Core Loss Density } Pcore = \frac{C_m \times Freq^x \times B^y \times \left(C_{t0} - C_{t1} \times Temp + C_{t2} \times Temp^2\right)}{1000}$$

$$P = 1.307 \times 10^3\ mW/Cm^3$$

$$CoreLoss = P \times V_E \times 10^{-3}$$

$$CoreLoss = 2.052W$$

One of the benefits of using planar construction is the opportunity to utilize 2 oz., 3 oz., and 4 oz. copper weight, which results in very thin copper. The impact is that skin depth and proximity loss factors are usually considerably reduced versus using wire wound magnetic structures. The copper losses are calculated using DC Resistance (DCR).

The secondary rms current in each half of the center tapped winding is shown in Equation 20.

EQUATION 20: SECONDARY RMS CURRENT

$$I_{SEC} = I_O \times \sqrt{D}$$

$$I_{SEC} = 16.47A$$

Primary rms current is calculated as shown in Equation 21:

EQUATION 21: PRIMARY RMS CURRENT

$$I_{PRI} = I_O \times \sqrt{2D} \times \frac{N_S}{N_P}$$

$$I_{PRI} = 9.317A$$

The DCR values are computed from the CAD drawings:

- Secondary DCR: *SecDCR* = 0.0023E
- Primary DCR: *PriDCR* = 0.025E

Secondary copper loss is multiplied by two because it is a center tapped winding.

EQUATION 22:

$$Sec\_Loss = 2 * I^2_{SEC} * Sec\_DCR = 1.248W$$

$$Pri\_Loss = I^2_{PRI} * Pri\_DCR = 2.17W$$

$$Total\_Loss = Sec\_Loss + Pri\_Loss + Core\ Loss$$

$$Total\_Loss = 5.466W$$

The stacking of the main transformer layers arrangement is shown in Table 5.

TABLE 5: STACKING LAYERS FOR PLANAR TRANSFORMER

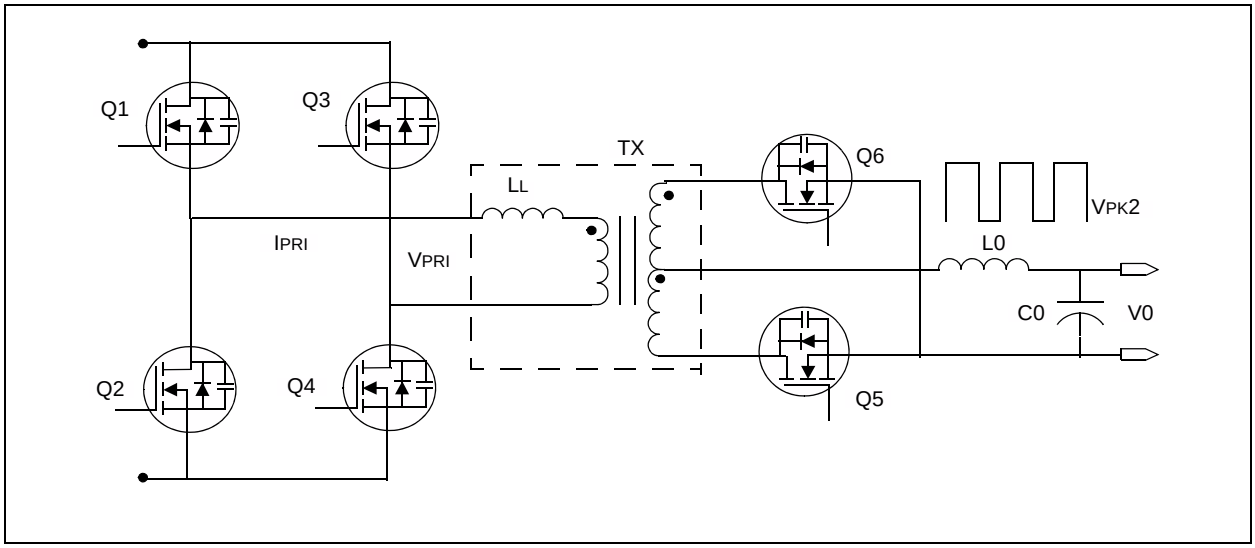
Layers	Winding			Cu Weight (Oz.)
	Primary	Sec1	Sec2	
Layer 1			Sec2	2
Layer 2				2
Layer 3		Sec1		2
Layer 4				2
Layer 5	Primary			4
Layer 6				4
Layer 7		Sec1		2
Layer 8				2
Layer 9	Primary			2
Layer 10				3
Layer 11			Sec2	3
Layer 12				2
Layer 13	Primary			4
Layer 14				4
Layer 15		Sec1		2
Layer 16				2
Layer 17			Sec2	2
Layer 18				2
Turns	5	2	2	

Planar Output Inductor Design

The output inductor serves the following functions:

- Stores the energy during the OFF period to keep the output current flowing continuously to the load.
- Smooths out and average the output voltage ripple to an acceptable level.

FIGURE 17: FULL-BRIDGE CONVERTER WITH CENTER TAPPED FULL WAVE SYNCHRONOUS RECTIFIER



The duty cycle (more than each half-period) to produce the desired output is as follows:

- Switch turn ON time, TON = 2.89 µs
- Total Switching period, TP = 6.667µs
- Duty cycle, D = TON/TP = 0.434

Over a full period the duty cycle is 86.8% at VINMIN 36 VDC.

EQUATION 23:

$$V_O = \left[(V_{IN} - V_{FETPRI}) \times \frac{N_S}{N_P} - V_{FETSEC} - V_{DROP} \right] \times 2D$$

$$V_O = 12.03V$$

In the case of output inductor, consider the choice of inductance value at the maximum off time. This occurs in PWM regulated DC-DC converters at the maximum input voltage, VIN MAX = 76V, and the feedback loop adjusts the switch ON time accordingly.

TONMIN = 1.415 µs

The duty cycle is as follows:

D_MIN = TONMIN/TP = 1.3689 µs

The peak voltage at the transformer secondary is as shown in Equation 24.

EQUATION 24:

$$V_{PK2} = (V_{INMAX} - V_{FETPRI}) \times \frac{N_S}{N_P} - V_{FETSEC} - V_{DROP}$$

$$V_{PK2} = 28.26V$$

Maximum output load current, IO = 25A. A ripple current of 25% of the total output current is considered in this design.

EQUATION 25:

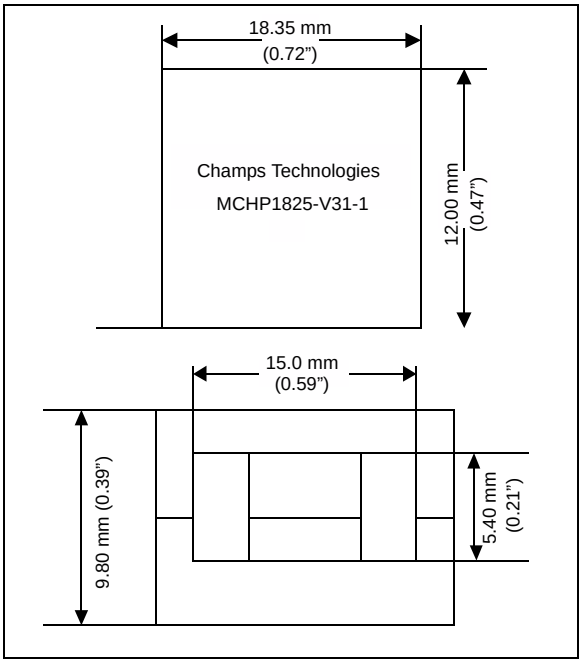
$$I_{MIN} = I_O \times 0.25 = 6.5A$$

EQUATION 26: OUTPUT INDUCTANCE (LOMIN)

$$L_{OMIN} = \frac{(V_{PK2} - V_O) \times T_{ONMIN}}{I_{MIN}} = 3.54\mu H$$

In this design, the core window height and its adequacy in terms of accommodating the 18 layer PCB stack is to be assessed since the windings/turns for the inductor are also embedded.

FIGURE 18: PLANAR OUTPUT INDUCTOR



This core is also a tooled core as the main transformer, TX1. It is available from Champs Technologies as PN MCHP1825-V31-1. Materials such as 7H from Nicera™, the PC95 from TDK™, or the 3C94, 3C92 from Ferroxcube™ are the recommended choices.

- Core cross section, AC = 0.4 cm^2
- Core path length, LCORE = 3.09 cm
- Rated output current: IRATED = 17A
- Defined saturation current: ISAT = 20A

The process of inductor design involves iterating the number of turns possible and solving for a core air gap. The air gap is checked for operating the flux below maximum rated flux in the core material at the two operating current values that is rated current and saturation current.

In this design, if the 18 layers are available, these layers can be split into balanced integer turns. This is a practical method and the number of turns Nt = 6.

In this design, a fringing flux factor assumption of 15% is done that is FFF = 1.15.

The iterative process begins by calculating the air gap equation. The air gap is calculated using Equation 27.

EQUATION 27:

$$L_{GAP} = \left(\frac{0.4 \times \pi \times Nt^2 \times A_C \times 10^{-8}}{L_{OMIN}} \right) \times FFF$$

$$= 0.058cm$$

$$L_{GAPIN} = \frac{L_{GAP}}{2.54} = 0.023inch$$

EQUATION 28: OPERATING FLUX DENSITY AT DEFINED SATURATION CURRENT

$$B_{DC} = \frac{0.4 \times \pi \times Nt \times I_{SAT}}{L_{GAP}}$$

$$B_{DC} = 2.598 \times 10^{3} Gauss$$

EQUATION 29: OPERATING FLUX DENSITY AT RATED CURRENT

$$B_{RATED} = \frac{0.4 \times \pi \times Nt \times I_{RATED}}{L_{GAP}}$$

$$B_{RATED} = 2.208 \times 10^{3} Gauss$$

The BDC and BRATED values are conservative compared to the commercially rated devices. Typical BMAX values are 3000 Gauss at 100ºC.

The required AL value is calculated, as shown in Equation 30.

EQUATION 30: A_L VALUE

$$A_L = \frac{L_{OMIN} \times 10^{9}}{Nt^{2}} = 98.32 mH$$

This is helpful for instructing the core manufacturer for gapping instructions. The inductor traces are designed using a CAD package and are integrated into the PCB layout package. The CAD package facilitates the calculation of trace resistance for each layer. The calculated DCR values $DCR_{RATED} = 3.5 * 10^{-3E}$.

Copper loss is computed at the DC values of rated and saturation-defined currents, as shown in Equation 31.

EQUATION 31:

$$Cu_{LossSAT} = (I_{SAT})^{2} \times DCR_{RATED}$$

$$Cu_{LossSAT} = 1.4W$$

EQUATION 32:

$$Cu_{LossRATED} = (I_{RATED})^{2} \times DCR_{RATED}$$

$$Cu_{LossRATED} = 1.012W$$

One of the design goals is to make it universal for other lower and higher power implementations of the digital converter and to keep the overall efficiency high. It fits comfortably with its footprint in the PCB. However, we consider that a smaller core and footprint optimization is quite possible.

Planar Drive Transformer Design

To drive each leg (high side and low side) of the gates, the high side/low side driver, or low side driver with isolated drive transformer is required. A minimum of 500 VDC isolation is required in the drive transformer from the high side to low side winding. Because the gate drive is derived from secondary side controller, primary to secondary 2500 VDC isolation is required.

The following critical parameters must be controlled while designing the gate drive transformer:

- Leakage inductance
- Winding capacitance

A high leakage inductance and capacitance causes an undesirable gate signal in the secondary, such as phase shift, timing error, overshoot and noise. Winding capacitance results when the design has a higher number of turns. Leakage inductance results when the turns are not laid uniformly. Because planar magnetics are used in this application, these parameters may not be a problem. Since the absolute number of turns required is low and the primary and secondary side high/low drive windings can be interleaved to minimize leakage without increasing the overall capacitance.

Typical gate drive transformers are designed with ferrite cores to reduce cost and to operate them at high frequencies. Ferrite is a special material that comprises high electrical resistivity and can be magnetized quickly with minor hysteresis losses. Because of its high resistance, eddy currents are also minimal at high frequency.

Selection of Core Materials and Core

Selection of core material depends on the frequency of the operation. 3F3 from Ferroxcube™ is one of the best options for the operating frequencies below 500 kHz. The power loss levels of gate drive transformers is usually not a problem and thus Ferroxcube RM4/ILP is selected. The magnetic parameters of Ferroxcube RM4/ILP are as follows:

- AC = 0.113 cm^2
- Lm = 1.73 cm
- AL =1200 nH
- µEFF = 1140

One of the primary goals of the design is to embed all the magnetics as part of the overall PCB design of the main power stage. A small size core geometry is selected, that has sufficient window height to accommodate the overall PCB thickness and also gives reasonable window width to accommodate the PCB trace width that comprises the turns. The resulting “footprint” or core cut-out required of the RM4/ILP was found to be acceptable.

We will iterate the primary turns to arrive at a suitable peak flux density and magnetizing current using the formula shown in Equation 33.

EQUATION 33:

$$N_P = \frac{(V_{IN} \times T_{ON}) \times 10^8}{B_{PKPK} \times A_C}$$

In the application, VIN = 12V as set by the bias supply. The operating frequency for main power processing is selected as 150 kHz. The result is the gate drive transformer operates at the same frequency.

The duty cycle is also determined by the power stage. The basic input parameters, TP and TON are set.

Iterating for primary turns, NP = 10.

The peak-to-peak flux density can be achieved as shown in Equation 34:

EQUATION 34: PEAK-TO-PEAK FLUX DENSITY

$$B_{PKPK} = \frac{(V_{IN} \times T_{ON}) \times 10^8}{N_P \times A_C}$$

$$B_{PKPK} = 3.069 \times 10^3 Gauss$$

The peak flux density is shown in Equation 35, which yields a volt-µs rating of (VIN * TON) = 37.7. This is well below the typical saturation curves for 3F3 of 3000 Gauss at 85ºC operational ambient temperature. However, potential saturation is not a design concern.

EQUATION 35: PEAK FLUX DENSITY

$$B_{PK} = \frac{(V_{IN} \times T_{ON}) \times 10^8}{2 \times N_P \times A_C}$$

$$B_{PK} = 1.534 \times 10^3 Gauss$$

The RMS flux density is calculated as shown in Equation 36.

EQUATION 36: RMS FLUX DENSITY

$$B_{RMS} = \sqrt{\frac{2}{T_P} \times \int_O^{T_{ON}} \left[\frac{(V_{IN} \times T_{ON}) \times 10^8}{2 \times N_P \times A_C} \right]^2 \times DT}$$

$$B_{RMS} = 1.363 \times 10^3 Gauss$$

results in mW of core loss.

The peak and RMS flux densities can be pushed higher. However, a reasonably low value of magnetizing current has been maintained such that the driver is not loaded much.

EQUATION 37: CALCULATION OF MAGNETIZING INDUCTANCE

$$LA_L = {N_P}^2 \times A_L \times 10^{-9}$$

$$LA_L = 1.2 \times 10^{-4} Henry$$

Or,

$$L_M = \frac{0.4 \times \pi \times \mu_{EFF} \times (N_P)^2 \times A_C \times 10^{-8}}{L_m}$$

$$L_M = 9.57 \times 10^{-5} Henry$$

Conversely, the inductance minimum will be between ~70 µH.

$$L_{MIN} = 0.75 L_M Henry$$

$$L_{MIN} = 6.699 \times 10^{-5} Henry$$

The magnetizing current is thus reasonable for this application, and is shown in Equation 38:

EQUATION 38:

$$di = \frac{V_{IN} \times T_{ON}}{L_M}$$

$$di = 0.362A$$

Assuming the worst case, the distributed capacitance is shown as follows:

$$C_D = 50 \times 10^{-12} Farad$$

Any ringing on the gate drive waveforms due to the transformer will possess a frequency of 2.3 MHz.

EQUATION 39:

$$F_R = \frac{1}{2 \times \pi \times (\sqrt{L_M \times C_D})}$$

$$F_R = 2.3MHz$$

In this design, the selection of track width or trace width was fairly conservative. Given the RM4/ILP core window width of 2.03 mm (80 mils), and an allowable PCB width accommodated inside this core of 1.63 mm (64 mils), and a further conservative assumption of trace-to-trace clearance of 0.3 mm (12 mils), we can either place 2T/layer of 0.39 mm (15 mil) width or 3T/layer of 0.18 mm (7 mils) width. If 4 oz. copper was used per layer the 0.18mm trace width would result in too much “under-etch” in the fabrication. We had ~14 layers dictated by the power stage and the resulting PCB thickness of 3.5-3.8 mm could be easily accommodated by the RM4/ILP core window height. Hence, it is easier to select 2T/layer. This selection also allowed three opportunities for an interleave to occur between the primary and each secondary drive winding. A choice of 3T/layer may have resulted in an imbalance and with less opportunity for interleave.

Current Sense Transformer Design

The current sense transformer selected is a conventional stand-alone magnetic device. The decision was made earlier to have a 1:100 current transformation ratio. Therefore, it is difficult to implement this device as an embedded structure.

We repeat some aspects of the TX1 main transformer design such as switching frequency.

EQUATION 40:

$$F_{SW} = 150 \times 10^{3} HZ$$

$$T_p = \frac{1}{F_{SW}}$$

$$T_P = 6.667 \times 10^{-6} Sec$$

The transformation ratio, $N_C = N_S/N_P = 100$

Maximum rated current, $I_{MAX} = 10A$

Therefore, secondary RMS current is computed as shown in Equation 41:

EQUATION 41: SECONDARY RMS CURRENT

$$I_{RMSSECY} = \frac{I_{RMSPRIM}}{N_C}$$

$$I_{RMSSECY} = 0.093A$$

EQUATION 42:

$$T_{ON} = 2.89 \times 10^{-6} Sec$$

$$T_{OFF} = \frac{T_P}{2} - T_{ON}$$

$$T_{OFF} = 4.433 \times 10^{-7} Sec$$

The core used on this part = E5.3/2.7/2-3C96

The core parameters are as follows:

- $L_M = 1.25$ cm
- $A_C = 0.0263$ cm^2
- $V_E = 0.0333$ cm^3

The nominal current sense termination resistor value: $R_B = 10.0E$.

EQUATION 43:

$$V_{PKSECY} = \frac{I_{MAX}}{N_S} \times R_B$$

$$V_{PKSECY} = 1V$$

Therefore, the rating is 0.1 V/amp.

EQUATION 44:

$$B_{PK} = \frac{(V_{PKSECY} \times T_{ON}) \times 10^{8}}{N_S \times A_C}$$

$$B_{PK} = 109.886 Gauss$$

It is considered that the peak flux density is very low and it is fine. Usually, the current to voltage gain is this low in most switched mode converters. The current ramp signal at the current sense (CS) input for most analog controllers is <1V so always select a low value termination resistor. In this case, the voltage gain is conditioned with differential op amps prior to sending it to the input ADC of the dsPIC® DSC.

It is helpful to know that higher current to voltage gains are possible simply by selecting higher value termination resistors. The only limitation will be a ceiling imposed by the saturation of the ferrite core.

The volt-µs rating of the CH-1005 Champs Technologies is 58V-µs. In this design, if a termination impedance of 100Ω is selected, a 10V signal amplitude is gained. The current transformer reproduces the current wave shape until it is not saturated, that is as long as it is performing as a transformer. In this design, a maximum ON time of 5.8 µs can be permitted.

The rated maximum flux is shown in Equation 45.

EQUATION 45:

$$B_{RATED} = \frac{(58 \times 10^{-6}) \times 10^{8}}{N_S \times A_C}$$

$$B_{RATED} = 2.205 \times 10^{3} Gauss$$

The B_{PK} is rated as 2200 Gauss peak for 100ºC operation unipolar excursion. The RMS flux density is calculated as shown in Equation 46.

EQUATION 46: RMS FLUX DENSITY

$$B_{RMS} = \sqrt{\frac{2}{T_P} \times \int_{O}^{t_{ON}} \left[\frac{(V_{PKSECY} \times T_{ON}) \times 10^{8}}{2 \times N_S \times A_C} \right]^2 dTp}$$

$$B_{RMS} = 51.159 Gauss$$

EQUATION 47:

$$CoreLossDensity, P = \frac{C_m \times F^x \times (B_{RMS})^y \times (C_{t0} - C_{t1} \times Temp + C_{t2} \times Temp^2)}{1000}$$

$$P = 0.048 \ mW/cm^3$$

where setting up core loss coefficients:

Cm = 8.27 * 10-2

x = 1.72

y = 2.80

Temp = 30

Ct1 = 3.66 * 10-2

Ct2 = 1.83 *10-4

Ct0 = 2.83

F = 1.5 * 10^5

$$CoreLoss = P \times V_E \times 10^{-3}$$

$$CoreLoss = 1.592 \times 10^{-6} W$$

Core loss is about zero or negligible.

Secondary *SecDCR* = 6.6E.

EQUATION 48:

$$Secloss = (I_{RMSSECY})^2 \times SecDCR$$
$$= 0.057W$$
$$Priloss = (I_{RMSPRIM})^2 \times PriDCR$$
$$= 0.173W$$
$$TotalLoss = Secloss + Priloss + Coreloss$$
$$= 0.23W$$

where:

Secloss = Secondary copper losses

Priloss = Primary copper losses

PriDCR = 0.002E

SecDCR = 6.6E

Total loss for this device at maximum ratings is less than 1/4W.

Calculate the inductance value for the selected 3C96 material.

EQUATION 49:

$$L_{AL} = (N_S)^2 \times A_L \times 10^{-9}$$
$$L_{AL} = 3 \times 10^{-3} \quad \sim 3mH$$

where:

Ns = 100

AL = 300 nH

EQUATION 50:

$$L_{MIN} = L_{AL} \times 0.75$$
$$= 2.25mH$$

Minimum secondary inductance = 2.25 mH.

$$X_L = 2 \times \pi \times f \times L_{MIN}$$
$$= 2.12 \times 10^3 E$$

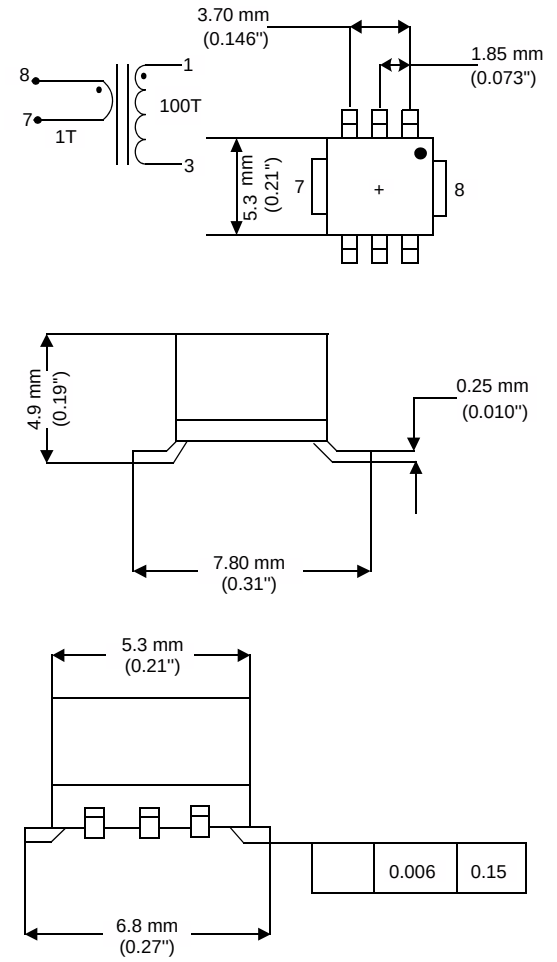
Effective termination impedance is as shown in Equation 51:

EQUATION 51:

$$X_{EFF} = \frac{X_L \times Rb}{X_L + Rb}$$
$$X_{EFF} = 9.953E$$

Deviation from ideal is < 0.1%.

FIGURE 19: CURRENT TRANSFORMER



Planar Auxiliary Power Supply Transformer Design

The digital DC/DC converter requires auxiliary power supply. The dsPIC DSC requires 3.3V and the gate drivers require 12V.

The dsPIC DSC must have power supplied to it prior to start-up of the power converter. The scheme to accomplish this is to utilize an analog converter for start-up and also for continuous operation. This avoids possible glitches or uncontrolled operation events during abnormal operation or unanticipated transient conditions. The analog controller requires a boot strap supply once it has gone through soft-start.

The dsPIC DSC requires 3.3V. A linear regulator is inserted prior to 3.3V so that the headroom required at one output is 4V. The 3.3V output voltage before regulator V01 = 4V.

- Load current, $I_{3.3V}$ = 0.3A
- 12V output voltage before regulator, V02 = 12V
- Load current, I_{12V} = 0.4A
- Total output power = 6W
- Consider an overall efficiency of 80%
- Input power = 7.5W

Consider minimum input voltage, VINMIN = 32V. The converter is designed to operate at a maximum duty cycle, D = 40%. The nominal operating frequency, FSW of the IC is 250 kHz.

EQUATION 52:

$$F_{SW} = 250 \times 10^{3} Hz$$

Total period, TP = 4 µs

On period, TON = 1.6 µs

EQUATION 53:

$$AverageCurrent, I_{AVE} = \frac{InputPower}{MinimumInputVoltage} = \frac{7.5W}{32V} = 0.234A$$

Peak current of a Discontinuous mode Flyback Converter, IPPK is shown in Equation 54.

EQUATION 54:

$$I_{PPK} = 2 \times \frac{I_{AVE}}{D} = 1.17A$$

Primary rms current, IRMSPRIM is shown in Equation 55:

EQUATION 55:

$$I_{RMSPRI} = I_{PPK} \times \sqrt{\frac{T_{ON}}{3 \times T_P}} = 0.427A$$

EQUATION 56:

$$PrimaryInductanceL_P = \frac{V_{INMIN} \times D}{F_{SW} \times I_{PPK}} = \frac{32 \times 0.4}{250000 \times 1.17} = 43.6\mu H$$

EQUATION 57:

$$PeakSecondaryCurrent, I_{SCPK} = \frac{2 \times I_{SCDC}}{D_S}$$

$$\frac{2 \times 0.1}{0.6} = 3.33A$$

$$SecondaryRMSCurrent, I_{SRMS} = \sqrt{\frac{D_S}{3} \times I_{SCPK}} = 1.489A$$

where:
Short circuit current: I_{SCDC} = 1A
Secondary duty cycle: D_S = 0.6

The turns ratio for 12V and 3.3V output is shown in Equation 58.

EQUATION 58:

$$\frac{N_P}{N_S} \geq \frac{[V_{IN} - (I_{PPK} \times R_{DS(ON)})] \times D}{(V_{OUT} + V_{fD1}) \times (0.8 - D)}$$

$$\frac{N_P}{N_{S12}} = 2.60$$

$$\frac{N_P}{N_S 3.3} = 7.828$$

where:
Voltage drop on the diode, V_{FD1} = 0.7V
$R_{DS(ON)}$ = 4E

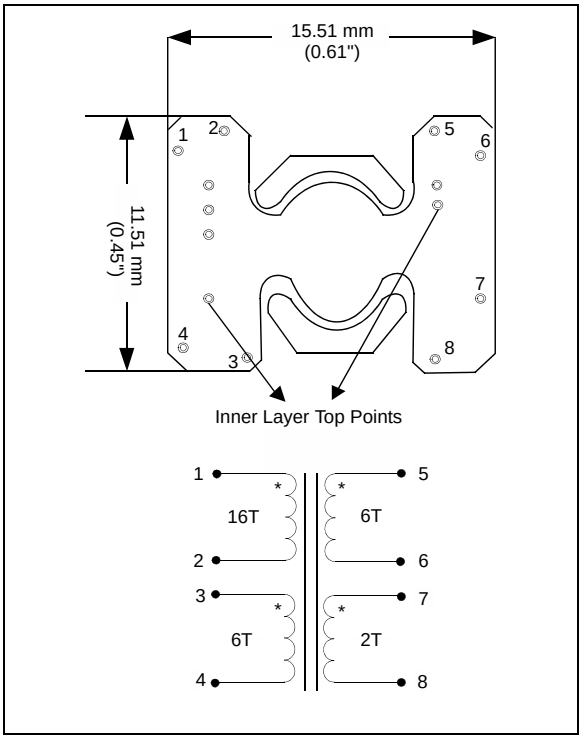
A quick check of the available standard core structures indicates that there was a distinct possibility to use a standard size RM-4 core.

An important feature of this core for this design is, it consists of a core window with nominal 4.3 mm that clears the 4.0 mm PCB thickness. The overall height of this core is 7.8 mm so it is <10 mm height of the DC/DC Converter mechanical height.

The RM-4 core parameters are:

- AE = 0.145 cm^2
- ICORE = 1.73 cm
- µ = 2000
- VE = 0.25 cm^3

FIGURE 20: AUXILIARY PLANAR TRANSFORMER



The footprint (length x width) of the device is not greater than that of a stand-alone magnetic device. The footprint shown above has been further reduced in the final implementation and the entire bias converter has been implemented as part of the embedded design.

EQUATION 59:

$$N_{PRI} = \frac{V_{INMIN} \times T_{ON} \times 10^8}{B_{MAX} \times A_E} = 16T$$

where:

B_{MAX} = 2200Gauss

The required center post air gap based on the formula is shown in Equation 60:

EQUATION 60:

$$L_{GAP} = \frac{0.4 \times \pi \times (N_{PRI})^2 \times A_E \times 10^{-8}}{L_P} \times FFF$$

$$L_{GAP} = 0.012cm$$

$$L_{GAPIN} = \frac{L_{GAP}}{2.54}$$

$$L_{GAPIN} = 4.591 \times 10^{-3} in$$

The A_L value is calculated as shown in Equation 61.

EQUATION 61:

$$A_L = \frac{L_P \times 10^9}{(N_{PRI})^2}$$

$$A_L = 164.063nH$$

The flux density is calculated as shown in Equation 62.

EQUATION 62:

$$B_{PK} = \frac{0.4 \times \pi \times N_{PRI} \times I_{PPK}}{L_{GAP}}$$

$$B_{PK} = 1.959 \times 10^3 Gauss$$

B_{PK} is lesser than B_{SAT} limitation of 3000 Gauss at 85ºC. The required maximum output power for DCM operation, factoring in efficiency is shown in Equation 63.

EQUATION 63:

$$P_O = \frac{1}{2} \times L_P \times (I_{PPK})^2 \times F_{SW}$$

$$P_O = 7.46W$$

The peak AC flux density is calculated as shown in Equation 64:

EQUATION 64:

$$B_{PKAC} = \frac{(V_{IN} \times T_{ON}) \times 10^8}{N_{PRI} \times A_E}$$

$$B_{PKAC} = 2.48 \times 10^3 Gauss$$

The RMS flux density is calculated as shown in Equation 65.

EQUATION 65:

$$B_{RMS} = \sqrt{\frac{1}{T_P} \times \int_O^{T_{ON}} \left[\frac{(V_{IN} \times T_{ON}) \times 10^8}{2 \times N_{PRI} \times A_E}\right]^2 dTp}$$

$$B_{RMS} = 771.454Gauss$$

The core loss equation parameters are used for Ferroxcube “3C92” material at 40ºC rise in temperature.

EQUATION 66:

$$B = \frac{B_{RMS}}{10000}$$

$$f = \frac{1}{T_P}$$

$$f = 2.5 \times 10^5 Hz$$

$$Temp = 40^{\circ} C$$

The operating coefficients are:

$C_M = 9.17 \times 10^{-5}$

EQUATION 67: CORE LOSS DENSITY FORMULA

$$P = C_M \times f^x \times B^y \times \frac{(C_{t0} - C_{t1}) \times Temp + C_{t2} \times Temp^2}{1000}$$

$$P = 303.063\ mW/cm^3$$

where:

$Ct2 = 2.33 * 10^{-4}$

$Ct1 = 4.72 * 10^{-2}$

$Ct0 = 3.39$

$x = 2.22$

$y = 2.46$

$$CoreLoss = P \times V_{OL} \times 10^{-3}$$

$$CoreLoss = 0.076W$$

A calculated core loss value of 76 mW is acceptable and a good reason to use ferrite for the core material.

The CAD package is used in the PCB trace design to calculate the trace DCR for the primary and secondary DC resistance.

- $DCR_{SEC} = 0.023E$
- $DCR_{PRI} = 0.088E$

EQUATION 68:

$$opperLoss = \left(I^2_{RMSPRI} \times DCR_{PRI}\right) + \left(I^2_{RMSSEC} \times DCR_{SEC}\right.$$

$$CopperLoss = 0.067W$$

The overall loss is shown in Equation 69.

EQUATION 69:

$$TotalLoss = CuLoss + CoreLoss$$

$$TotalLoss = 0.142$$

The only efficiency penalty in using a digital controller is the bias supply converted efficiency of 80%. All converters will share approximately the same FET driver loss.

The only further penalty is the footprint or space occupied by the bias supply within the available outline package of the converter itself. The main advantage as discussed at the outset is that the controller is “always on”, that is, it supplies power in a controlled fashion and rides out abnormalities and transients that might at the least require a hiccup start-up for an analog controller.

DESIGNING A DIGITAL QUARTER BRICK CONVERTER

The Quarter Brick DC/DC Converter was designed using the dsPIC33FJ16GS502. The design analysis is described in the following sections.

What is a Digitally Controlled Power Supply?

A digital power supply can be broadly divided into power control and power management. Power control is relatively a new trend when compared to power management.

Power management is data communication, monitoring, data logging, power supply protection, and sequencing of the outputs. This is not real time because the switching frequencies of the converters are higher than the power management functions.

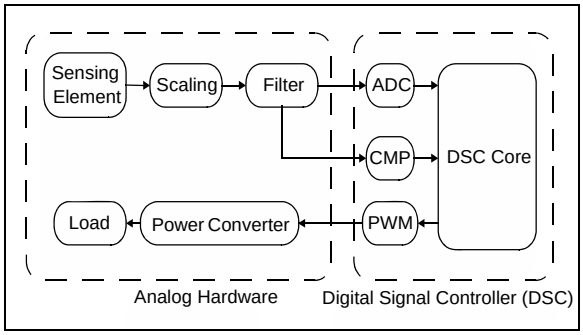
Power control is defined as the flow of power in the converter and it is controlled from one PWM cycle to another PWM cycle. Power control is performed with both the DSCs and analog controllers without much variation in the design.

Advantages of DSC

In modern SMPS applications, power conversion is only part of the total system solution. In addition, many other requirements and features are required to make the system more reliable. These features can be realized using a DSC and are as follows:

- Improved level of portability to other converter topologies
- Adaptive and predictive control mechanism to achieve high efficiency and improved dynamic response
- Software implementation of the protections to reduce the component count
- Improved scalability
- Active load balancing in the parallel connected systems
- Improved overall system reliability and stability
- System performance monitoring capability
- Real time algorithms for the regulation of power converters
- Less susceptibility to parameter variations from thermal effects and aging

FIGURE 21: REAL WORLD SIGNAL CHAIN: DIGITAL POWER SUPPLY



DIGITAL PHASE-SHIFTED FULL-BRIDGE (PSFB) DESIGN

In the digital power supply design, the power train is same as the analog power converter design. The difference exists in the way it is controlled in the digital domain. The analog signals such as voltage and current are digitized by using the ADC, and fed to the DSC. These feedback signals are processed with the digital compensator and modulate the PWM gate drive to get the desired control on the output.

Few critical peripherals that are used in digital power supply are listed below:

- PWM generator
- ADC
- Analog comparator

PWM Generator

The PWM generator must have the ability to generate high operating frequencies with good resolution, dynamically control PWM parameters such as duty cycle, period, and phase, and to synchronously control all PWMs, fault handling capability, and CPU load staggering to execute multiple control loops.

The PWM resolution determines the smallest correction to be done on the PWM time base.

EQUATION 70:

$$PWMResolution = \frac{PWMClockFrequency}{DesiredPWMFrequency}$$

EQUATION 71:

$$BitResolution = \log 2\left(\frac{PWMClockFrequency}{DesiredPWMFrequency}\right)$$

EXAMPLE 1:

PWM Clock Frequency = 60 MHz

Desired PWM Frequency = 500 kHz

PWM Resolution = 120 = One part in 120

Bit Resolution = log_2 (120) ~ 7 bits

EXAMPLE 2:

PWM Clock Frequency = 1000 MHz

Desired PWM Frequency = 500 kHz

PWM Resolution = 2000 = One part in 2000

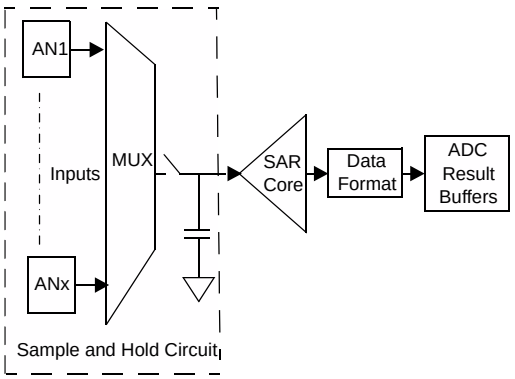
Bit Resolution = log_2 (2000) ~ 11 bits

A resolution of 11 bits indicates that the user can have 2048 different steps from zero to full power of the converter. This gives finer granularity in control of the duty cycle when compared to the seven bits resolution where only 128 steps are available for control.

Analog-to-Digital Converter (ADC)

All the real world feedback signals are continuous signals, and should be digitized to process in the DSC. A built-in ADC performs this process. ADC requires a voltage signal that is to be provided as an input. The input signals are scaled down to the ADC reference voltage. These voltages are typically 3.3V and 5V.

FIGURE 22: ANALOG-TO-DIGITAL CONVERTER (ADC)



In digital SMPS applications, higher bit resolutions and higher speed are the two characteristics that determine the ADC selection.

The ADC resolution indicates the number of discrete values it can produce over the range of analog values, hence the resolution is expressed in bits.

EQUATION 72:

$$ADCResolution = \frac{FullScaleVoltage}{2^n}$$

where:

n = Number of bits in the ADC

EXAMPLE 3: CALCULATING THE ADC RESOLUTION

Example A:

ADC full voltage = 3.3V

Number of bits in an ADC = 10

Therefore, ADC resolution = 3.22mV

Another parameter to be considered is the sample and conversion time (time taken by ADC to sample an analog signal and to deliver the equivalent digital value). Usually, the conversion time is specified in million samples per second (Msps). For example, if the conversion time is specified as 2 Msps, the ADC can convert two million samples in one second. Hence, the sample and conversion time is 0.5 µs.

The conversion speed plays an important role to replicate the sampled signal. As per Nyquist criterion, the sampling frequency must be greater than twice the bandwidth of the input signal (Nyquist frequency). As a guideline in SMPS applications, sampling of the analog signal at a frequency greater than 10x of the signal bandwidth is required to maintain fidelity.

Analog Comparator

Most of the DSCs consists of an analog comparator as a built-in peripheral which enhances the performance of SMPS applications. Analog comparator can be used in cycle-by-cycle control method to improve the response time of the converter and also in the fault protection applications.

ADC and PWM Resolution in SMPS Applications

Usually, analog controllers provide fine resolution to position the output voltage. The output voltage can be adjusted to any arbitrary value, and is only limited by loop gain and noise levels. However, a DSC consists of a finite set of discrete levels, because the quantizing elements, ADC and PWM generator exist in the digital control loop. Therefore, the quantization of ADC and PWM generator is critical to both static and dynamic performance of switched mode power supplies.

The ADC resolution must be lower than the permitted output voltage variation to achieve the specified output voltage regulation. The required ADC resolution is shown in Equation 73.

EQUATION 73:

$$N_{A/D} = Int\left[\log 2\left(\frac{V_{MAX_{A/D}}}{V_{REF}} \times \frac{V_o}{\Delta V_o}\right)\right]$$

where:

$V_{MAX\ A/D}$ = ADC full range voltage in this application

V_{REF} = Reference voltage

$N_{A/D}$ = Number of bits in ADC

V_O = Signal to be measured (output voltage)

ΔV_O = Allowed output voltage variation

Int [ ] = Denotes taking the upper rounded integer

EXAMPLE 4: ADC Resolution

$V_{MAX\ A/D}$ = 3.3V

V_O = 12V

ΔV_O = 1% of 12V = 120 mV

V_{REF} = 2.6V which is 80% of the ADC full range voltage

$N_{A/D}$ = 7, (therefore, a 7-bit ADC can be used)

ADC resolution can also be expressed as follows:

$$ADC\ LSB << (V_{REF}/V_O) * \Delta V_O$$

The digital PWM produces an integer number of duty values (it produces a discrete set of output voltage values). If the desired output value does not belong to any of these discrete values, the feedback controller switches among two or more discrete values of the duty ratio. In digital control system, this is called as limit cycle and it is not desirable.

Limit cycling can be avoided by selecting the change in output voltage caused by one LSB change in the duty ratio has to be smaller than the analog equivalent of the LSB of ADC. For a buck type forward regulator, N_{PWM} is shown in Equation 74.

EQUATION 74:

$$N_{PWM} >= N_{A/D} + log_2\left[\frac{V_{ref}}{V_{MAX\ A/D} * D}\right]$$

where:

N_{PWM} = Number of bits in a PWM controller

D = Duty ratio

To generalize, N_{PWM} must be minimum of one bit more than $N_{A/D}$.

Note: To have a stable output, that is without limit cycling, the down stream quantizer of the ADC should have higher resolution.

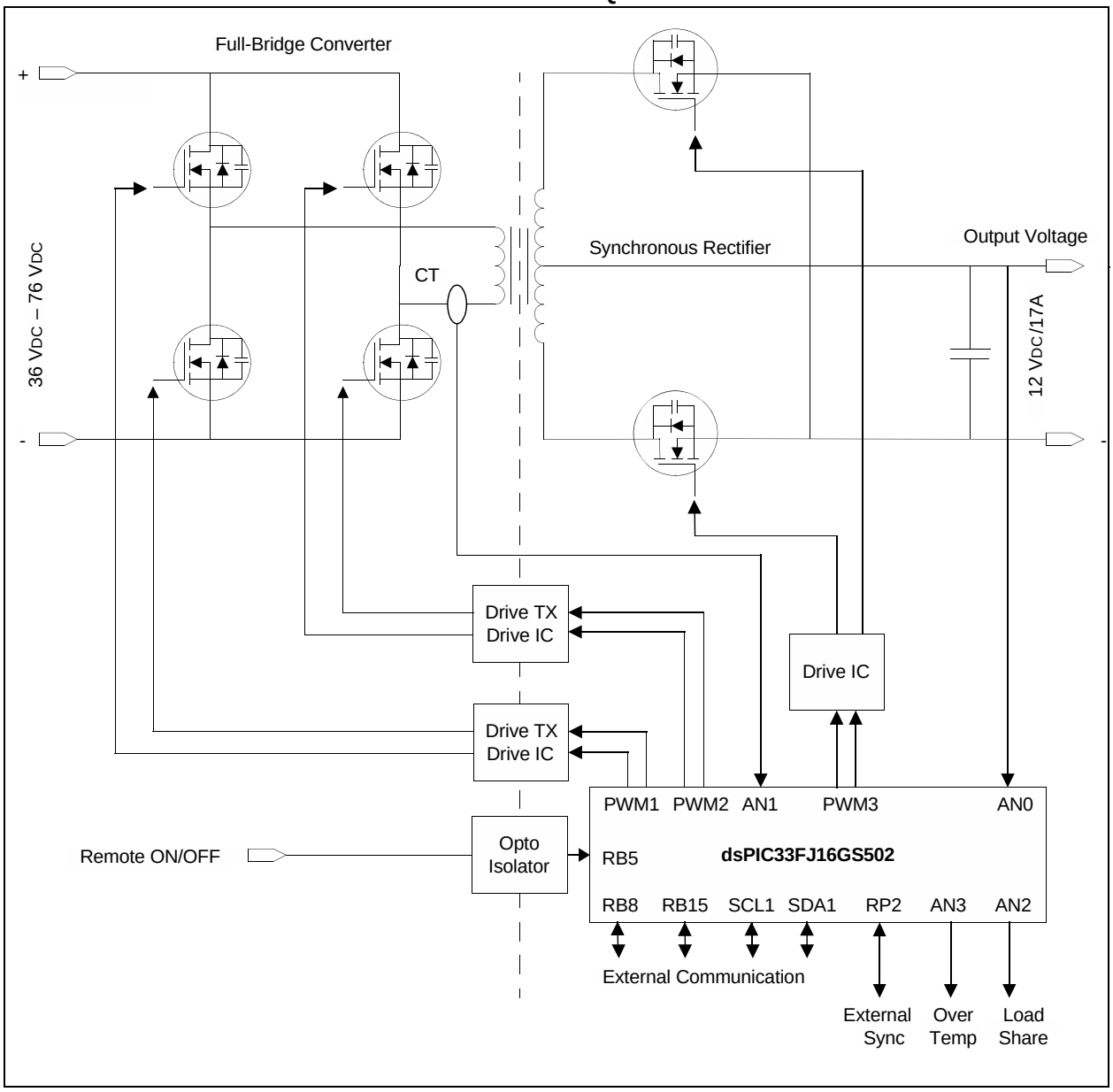
TABLE 6: SWITCHING FREQUENCIES OF THE CONVERTER

Signal Name	Description	Type of Signal	dsPIC® DSC Resource	Frequency of Operation
PWM1H,PWM1L	Left Leg Gate Drive	PWM Output	PWM1H,PWM1L	150 kHz
PWM2H,PWM2L	Right Leg Gate Drive	PWM Output	PWM2H,PWM2L	150 kHz
PWM3H,PWM3L	Synchronous Rectifier Gate Drive	PWM Output	PWM3H,PWM3L	150 kHz
—	Control Loop Frequency	—	—	75 kHz

TABLE 7: DSC PERIPHERALS MAPPED TO PSFB CONVERTER

Pin	Peripheral	Description
1	AN2	Load share
2	AN3	Temp
3	CMP2C	Output overvoltage
4	RP10	TX secondary voltage
5	VSS	Ground
6	CMP4A	TX overcurrent
7	RP2	EXT SYNCI1
8	PGD2	Programming
9	PGC2	Programming
10	VDD	Bias supply +ve
11	RB8	COM1
12	RB15	COM2
13	RB5	Remote ON/OFF
14	SCL1	COM4
15	SDA1	COM3
16	VSS	Ground
17	VDDcore	VDD core
18	PWM3H	Sync gate drive
19	PWM3L	Sync gate drive
20	PWM2H	PSFB gate drive
21	PWM2L	PSFB gate drive
22	PWM1H	PSFB gate drive
23	PWM1L	PSFB gate drive
24	AVSS	Ground
25	AVDD	Bias supply +ve
26	$\overline{\text{MCLR}}$	Master clear
27	AN0	TX current
28	AN1	12V output

FIGURE 23: dsPIC® DSC RESOURCES FOR THE QUARTER BRICK CONVERTER



DIGITAL CONTROL SYSTEM DESIGN

Digital control system design is a process of selecting the difference equation or Z-domain transfer function for the controller to achieve good closed loop response. Parameters such as settling time, output overshoot, rise time, control loop frequency and bandwidth must be considered to achieve acceptable performance.

The denominator polynomial of transfer function provides the roots of the equation. These roots are the poles of the transfer function. This equation is called the characteristic equation.

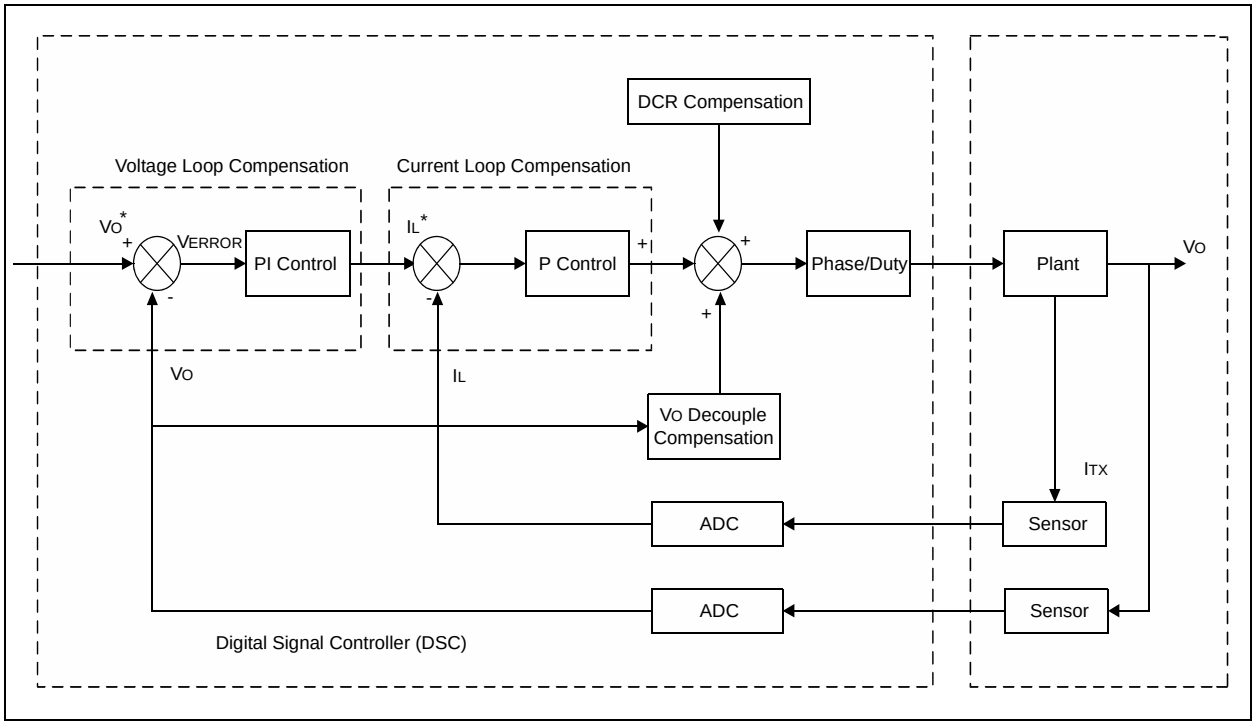
The nature of roots of the characteristic equation provides an indication of the time response. The system stability can be determined by finding the roots of the characteristic equation and its location. The system is considered to be stable if the roots of the characteristic equation are located in left half of the 'S' plane. This causes the output response due to bounded input to decrease to zero as the time approaches infinity.

In the quarter brick converter design, the controller is designed in the continuous time domain and then converted to an equivalent digital controller. This approach is called digital re-design approach or digital design through emulation.

Digital Average Current Mode Control Technique

Digital current mode control is a new approach for improving the dynamic performance of high frequency switched mode PWM converters, and is used in this design. In this method, DSC performs the entire control strategy in software. The current mode control (CMC) strategy consists of two control loops. The inner current loop subtracts a scaled version of the inductor current from the current reference. The current error is further processed with the PID or PI compensator and the result is appropriately converted into duty or phase. Any dynamic changes in the output load current directly modifies the duty or phase of the converter. The outer loop subtracts the scaled output voltage from a reference and the error is processed using the PID or PI compensator. The output of the voltage loop compensator provides the current reference for the inner loop. Current and voltage compensators allow tuning of the inner and outer loops to ensure converter stability and to achieve the desired transient response.

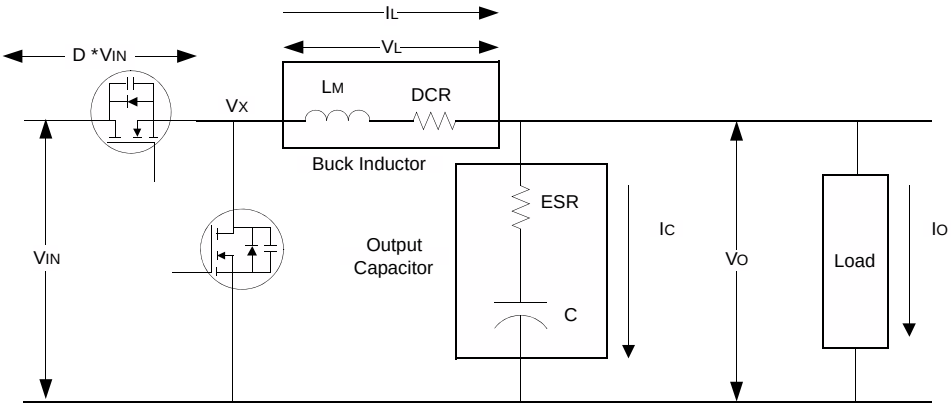
FIGURE 24: AVERAGE CURRENT MODE CONTROL



Deriving the Characteristic Equation for the Current Mode Control (CMC)

Let us take a simple buck converter to derive the characteristic equation.

FIGURE 25: BUCK CONVERTER



Based on Figure 25, and applying Kirchhoff's laws results in the expressions and equations shown in Equation 75.

EQUATION 75:

(A) $I_C = I_L - I_O$

(B) $V_O = D \times V_{IN} - V_L$

(C) $I_L = \frac{V_L}{X_L} = \frac{V_L}{2\pi fL} = \frac{V_L}{J\omega L} = \frac{V_L}{sL}$

(D) $V_O = I_C \times X_c = \frac{I_c}{2\pi fC} = \frac{I_C}{J\omega C} = \frac{I_C}{sC}$

The current compensator proportional gain is denoted as RA, and it has a dimension of resistance. The value of RA can be determined from the system characteristic equation. Higher value of RA implies higher current loop bandwidth. With the current mode control, the 'D' term performance in the voltage PID can be achieved.

EQUATION 76:

$$V_X = V_O + V_L$$

$$V_X = V_O + sLI_L = R_A \times [(I_L^*) - I_L] + [V_X - sLI_L]$$

(E) $$I_L = \frac{[R_A \times (I_L^*)]}{R_A + sL}$$

The current reference (IL*) is generated using the outer voltage loop.

[IL* = (VO* - VO) * G] (because current loop performs the function of differential gain in the voltage loop, the outer voltage loop will have only proportional and integral gain).

From the physical capacitor system, IC = IL - IO. In the equation, IO is made as constant and analyzed the relation between VO and VO*. Therefore, IL = sCVO.

EQUATION 77:

(F) $$(I_L)^* = (V_O^* - V_O) \times \left(K_P + \frac{K_I}{s}\right)$$

$$I_L \times \frac{(Ra + sL)}{Ra} = [(V_O^*) - V_O] \times \left[K_P + \left(\frac{K_I}{s}\right)\right]$$

The Equation 77 is rearranged to find VO*/VO and is shown in Equation 78.

EQUATION 78:

$$\frac{V_O^*}{V_O} = \frac{\left[K_P \times R_A + \left(\frac{K_I}{S}\right)\right]}{s^2LC + (sC \times R_A) + (K_P \times R_A) + \left(\frac{K_I}{s}\right) \times R_A}$$

The denominator $[s^2LC + sCRa + K_PRa + (K_I/s)Ra]$ denotes the characteristic equation. The denominator should have three roots known as three poles or three bandwidths, f1 > f2 > f3 (units of Hz) of the controller. These roots correspond to current loop bandwidth (f1), proportional voltage loop bandwidth (f2) and integral voltage loop bandwidth (f3). These roots should be selected based on the system specifications. f1, f2 and f3 should be separated with a factor minimum of three between them. This ensures that any parameter variation (L and C) due to manufacturing tolerance or inductor saturation will not affect the stability of the system.

The f3 determines the settling time (T_S), that is the output voltage of the converter takes to settle within 98% of V_O* for a step change in load. Ts should be selected less than the specification settling time.

$T_S = 4/2\pi f3$

The f2 determines the ability of the controller to track changes in V_O*. If V_O* varies, V_O can track V_O* variations up to a frequency f2 Hz.

The f1 exists only to make the system non-oscillatory or resonant at frequencies greater than f2.

The gains K_P, K_I and R_A can be determined once f1, f2 and f3 are selected. The characteristic equation:

$s^3LC + s^2CRa + s\,K_P\,Ra + K_I\,Ra = 0$ is a cubic equation.

Because 's' is $-2\pi f1(\omega 1)$, $-2\pi f2$ ($\omega 2$) and $-2\pi f3$ ($\omega 3$), which are the roots of the characteristic equation and should make the equation equal to zero after substituting for 's'. The three unknown coefficients K_P, K_I and R_A can be obtained by solving the following three equations shown in Equation 79:

EQUATION 79:

$$\omega_1^2 CR_A + \omega_1 K_P R_A + K_I R_A = -\omega_1^3 LC$$

$$\omega_2^2 CR_A + \omega_2 K_P R_A + K_I R_A = -\omega_2^3 LC$$

$$\omega_3^2 CR_A + \omega_3 K_P R_A + K_I R_A = -\omega_3^3 LC$$

This can be solved by using the matrix method shown in Equation 80.

EQUATION 80:

$$\begin{bmatrix} \omega_1^2 & \omega_1 & 1 \\ \omega_2^2 & \omega_2 & 1 \\ \omega_3^2 & \omega_3 & 1 \end{bmatrix} \times \begin{bmatrix} CRa \\ K_P R_A \\ K_I R_A \end{bmatrix} = \begin{bmatrix} -\omega_1^3 LC \\ -\omega_2^3 LC \\ -\omega_3^3 LC \end{bmatrix}$$

The matrix shown in Equation 80 is made equivalent to A * Y = B for simplicity purpose.

EQUATION 81:

$$Y = \begin{bmatrix} Y1 \\ Y2 \\ Y3 \end{bmatrix} = A^{-1} \times B$$

$Y1 = C\,R_A$ and $R_A = Y1/C$

$Y2 = K_P\,R_A$ and $K_P = Y2/R_A$

$Y3 = K_I\,R_A$ and $K_I = Y3/R_A$

Finding the Gains

Substituting the actual design parameters used in the PSFB converter to have the K_P, K_I, R_A gains.

- Transformer turns ratio = 5:2
- Primary input voltage, V_{IN} = 76V
- Nominal primary input voltage, V_{NOM} = 48V

The maximum primary input current is selected as 9.75A and is reflected to the secondary because the controller exists on the secondary side of the isolation barrier.

The base value of the current IN_{BASE} is 24.38A and the base value of the voltage VN_{BASE} is 14.2V. All the voltage and current quantities are referenced with the base values IN_{BASE} and VN_{BASE}.

Transformer secondary voltage is:

- V_{INS} = V_{IN}/turns ratio = 30.4V
- Output inductor L = $3.4e^{-6}$ Henry
- DC resistance of the inductor and tracks is considered as DCR = 0.05E
- Output capacitance, C = $4576e^{-6}$F (4400 µF external to converter)
- Equivalent series resistance of the capacitor, ESR = 0.0012E
- Switching frequency of the converter, F_{SW} = 150000 Hz
- Control loop frequency T_S is 1/2 of the F_{SW} that is:

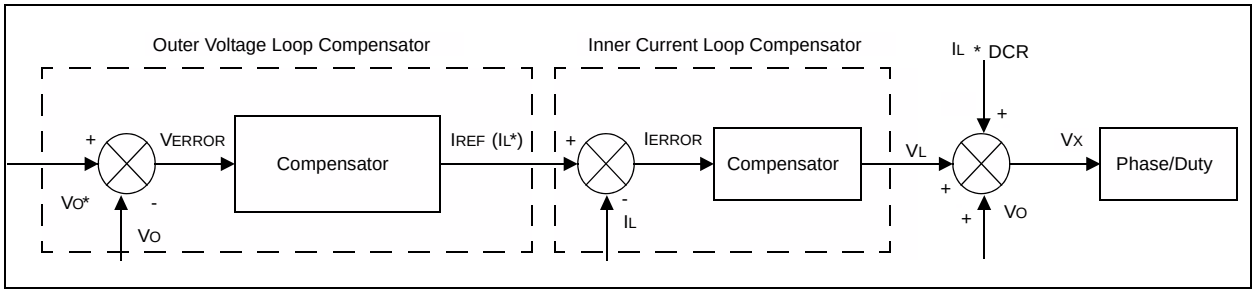
$$T_S = \frac{1}{F_{SW}/2}$$

- Integral voltage BW, f3 = -1000 * 2 * π
- Proportional voltage BW, f2 = -2000 * 2 * π
- Proportional current loop BW, f1 = -4000 * 2 * π

The characteristic equation is solved using the above three bandwidths.

- R_A = 0.1495
- K_P = 57.5037
- K_I = 2.0646e + 005

FIGURE 26: CONTROL LOOP COMPENSATOR DESIGN BLOCK DIAGRAM



Scaling

The gains calculated previously are based on real units (volts, amps, and so on). The dsPIC DSC consists of a fixed point processor and the values in the processor comprise linear relationship with the actual physical quantities they represent.

The gains calculated are in real units, and cannot be directly applied to these scaled values (representation of physical quantities). Therefore, for the consistency these gains must be scaled.

The scaling feedback section and the prescalar section provide general concepts of scaling.

The basic idea behind scaling is the quantities that are to be added or subtracted should have the same scale. Scaling does not affect the structure of the control system block diagram. Scaling only affects the software representation of various quantities used in the software.

Scaling Feedback

To properly scale the PID gains, it is imperative to understand the feedback gain calculation. The feedback can be represented in various formats. Fractional format (Q15) is a very convenient representation.

Fractional format allows easy migration of code from one design to another with different ratings where most of the changes that exist only in the coefficients and are defined in the header file.

To use the available 16 bits in the processor, the Q15 format is most convenient as it allows signed operations and full utilization of the available bits (maximum resolution). Other formats can also be used, but resolution is lost in the process. Q15 allows using the fractional multiply `MAC` and `MPY` operation of the dsPIC DSC effectively.

The feedback signal (typically voltage or current) is usually from a 10-bit ADC. Based on the potential divider or amplifier in the feedback circuitry, actual voltage and current is scaled.

Typically, the feedback 10-bit value (0 -1023) is brought to ±32767 range by multiplying with 32. This format is also known as Q15 format: Q15(m) where -1<m<1 and is defined as (int) (m * 32767).

These formulae will have some error as 2^{15} = 32768 is required, but due to finite resolution of 15 bits, only ±32767 is used. From a control perspective, for most systems these hardly introduce any significant error. In this format, +32767 correspond to +3.3V and 0 corresponds to 0V.

Prescalar

As most physical quantities are represented as Q15 format for easy multiplication with gains, the gains must also be represented in fractional format. If the value of gain (G * VNBASE/INBASE) is between -1 and +1, it can be easily represented as fractional format.

Multiplication can then be performed using fractional multiply functions such as `MAC` or using `builtin_mul` functions and shifting appropriately. For example, z = `(__builtin_mulss(x,y)` >> 15) results in z = Q15(fx,fy), where all x, y, and z are in Q15 format (fx and fy are the fractions that are represented by x and y).

In many cases, the gain terms are greater than unity. Because 16-bit fixed point is a limitation, a prescalar may be used to bring the gain term within the ± range.

In this application, voltage loop proportional gain KP value is higher than one. Therefore, it is normalized using the defined current, voltage base values with the pre scalar 32. For simplifying the calculations, the voltage integral gain (KI) is also scaled with 32, that means if a prescalar is used for P term in a control block, it must also be used for the 'I' and 'D' term in the control block since all the terms are added together.

To prevent the number overflows, PID output and 'I' output must be saturated to ±32767.

The saturation limits for the PID output must be set at 1/32 of the original ±32767 to account for the prescalar. Therefore, saturation limits are set at ±1023. Finally, after saturation, the output must be post scaled by five to bring it to proper scale again.

Gain Scaling

The voltage compensator input is in voltage dimensions and the output is in current dimensions, the voltage loop coefficients dimensions will be in mho (Siemens).

New value voltage loop proportional gain K_P after normalizing and scaling will be (K_P * VN_{BASE})/(IN_{BASE} * prescalar) that is 1.04.

New value voltage loop integral gain, K_I after normalizing and scaling will be K_I * T_S * VN_{BASE}/(IN_{BASE} * prescalar) = 0.0501.

The current compensator input is in current dimensions and the output is in voltage dimensions, the current loop coefficients dimensions will be in Ω.

New value current loop Integral gain, R_A after normalizing is [(R_A/V_{INS}) * IN_{BASE}] = 0.1495.

A few more contributors for the Phase/Duty control, are voltage decouple term and DCR compensation term. These are discussed below.

Because at steady state (V_L = 0), the average output of switching action will be equal to V_O. A contribution of V_O can be applied towards V_X (the desired voltage at primary of the transformer).

V_O information is available in the software, so the voltage decouple term can be easily calculated. This will improve the dynamic performance and make the design of control system easier. PI output performs only small changes to correct for load and line variations and most of the variation in PHASE/DUTY is contributed by V_O.

The voltage decouple term after scaling will be VN_{BASE}/V_{INS}.

The other parameters that need to be addressed are the resistance drops in the traces and magnetic winding resistance drop which may cause the current loop to function less than ideal. The dimension of gain of the current loop is in ohms. The physical resistance may interfere with the control action. If this resistance is known and measured during the design stage, then this resistance drop in the software can be compensated.

The DC resistance compensation term after scaling will be (DCR/V_{INS}) * IN_{BASE}.

The input quantity should be in fractional format (this must be ensured in code). Then, the output current quantity will automatically be in the correct fractional quantity. This essentially solves the objective of scaling. The same logic applies to any control block.

By considering the input and output units and scale of each block to be implemented in software, the proper scaled values can be arrived.

LOAD SHARING

In the traditional analog controller, regulation of the converter is achieved by a simple PWM controller, and load sharing of the converter is achieved by an additional load sharing controller/equivalent amplifier circuit. Recently, high end systems are calling for logging of converter parameters, which requires a microcontroller to communicate to the external world. Therefore, each converter needs a PWM controller, a load sharing controller, and a Microcontroller to meet the desired specifications.

In the recent past, cost of the DSCs has reduced drastically and are highly attractive for use by power supply designers in their applications. Digital controllers are immune to component variations and have the ability to execute sophisticated nonlinear control algorithms, which are not common or unknown in analog controlled power systems.

Apart from closing the control loop digitally, the DSC can perform fault management and communicate with the external applications which is becoming more and more significant in server applications. Digitally controlled power systems also offer advantages where very high precision, flexibility and intelligence are required.

For the overcurrent protection or short circuit protection of the converters, load current or load equivalent current will be measured and the same will be used for the load sharing between the converters. Therefore, an additional circuitry/additional controller is not required in the case of a digitally controlled power supply compared to its analog counterpart for load sharing. This reduces overall cost as the component count is lower and easier to implement by adding a few lines of code to the stand-alone converter design.

Digital Load Sharing Implementation

Basic operation of the analog and digital load sharing concept is the same; however, implementation is completely different. In the digital implementation, the ADC will sample the continuous signals of output voltage and output current. The sampling frequency of the output voltage and output current signal is user configurable. The PID compensator design calculations are performed in the Interrupt Service Routine (ISR) and are updated based on the control loop frequency.

In the dual load sharing implementation, for additional current, error information is added and this combined data will be given to the PWM module to generate appropriate phase/duty cycle. The PID compensator design will be same as the standalone individual converter. The load sharing compensator depends on the expected dynamic performance and this depends on the bandwidth of the current feedback. The current loop compensator forces the steady state error, (δI_L) between individual converter currents I_{L1}, I_{L2} and average current (I_{AVE}) to zero.

Typically, temperature is a criteria for stress on the components and the junction temperature bandwidth is around 5 ms (about 30 Hz). Therefore, it is sufficient to use ~500 Hz bandwidth current data and the current share loop can have a bandwidth of ~100 Hz. Here, the DSC allows output voltage regulation by designing the voltage/current loop compensator and load current sharing by load current loop compensator design. Effectively, both the output voltage regulation and the load sharing will be done with the single controller and this results in fewer components, less complexity and increased reliability. Poor noise immunity is a disadvantage of this design.

Load sharing loop proportional gain, IK_P will be $2\pi fL = 0.0021$

Load sharing loop integral gain, IK_I will be $2\pi f_5$ $IK_I = 0.3356$, where f5 (25 Hz) is the zero of the PI.

New value voltage loop proportional gain, IK_I after normalizing and scaling w ill be as shown below:

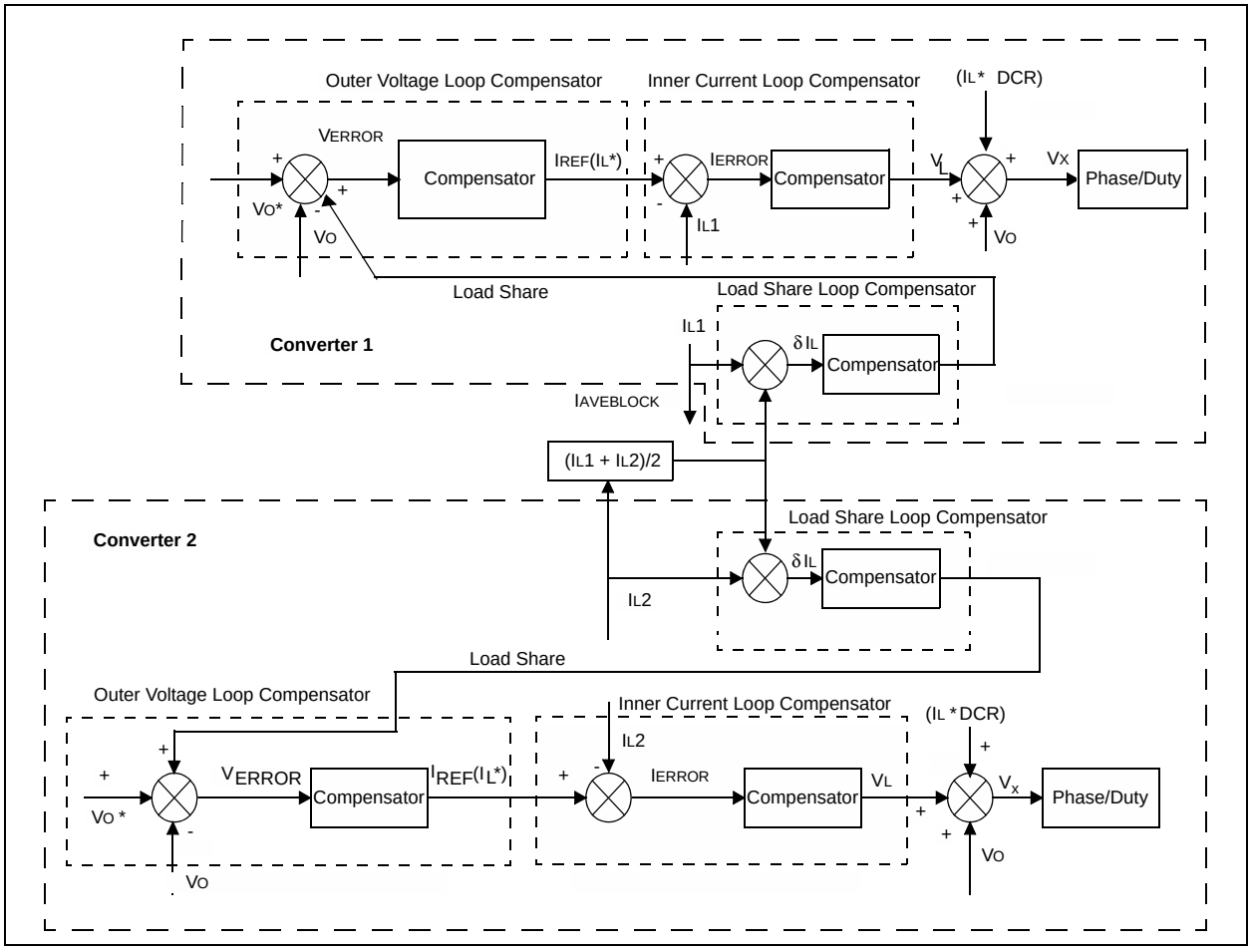
$IK_P * IN_{BASE}/VN_{BASE} * prescaler2 * 1.25 = 0.0734$

New value voltage loop proportional gain, IK_I after normalizing and scaling will be as follows:

$IK_I * IN_{BASE}/VN_{BASE} * prescaler2 * T_{SLOADSHARE} = 0.0092$

In this application, the load sharing sampling time ($T_{S\ LOADSHARE}$) is selected as 1 kHz.

FIGURE 27: SINGLE WIRE LOAD SHARE COMPENSATOR DESIGN BLOCK DIAGRAM



MATLAB MODELING

The .m file is used to generate the coefficients that are used in the MATLAB model (.mdl). This file also generates the scaled values to be used in the software. The generated values are in fractional format. In software, the coefficients must be represented as Q15(x), where 'x' is a fractional value.

For more detailed calculations, refer to the MATLAB (.m) file in the PSFB_MATLAB file. For the MATLAB Simulink block diagram, refer to the MATLAB (.mdl) file.

The following Bode plots (Figure 29 through Figure 31) are generated from the MATLAB (.m) file. Each plot is used to describe the behavior of the system.

The disturbance rejection plot is defined as: $I(s)/V_O(s)$.

The transfer function $I_O(s)/V_O(s)$ (with $V_O^*(s) = 0$) is called as dynamic stiffness or disturbance rejection. This plot explains us for a unit amplitude distortion in V_O, the amount of load needed as a function of frequency. The system needs to be as robust as possible so that the output does not change under load.

The higher this absolute figure of merit, the stiffer (better) the power supply output will be. The minimum is 35 db in this application, which will correlate to 56A (20logI = 35 dB) at approximately 1300 Hz of load producing 1.0V ripple on the output voltage.

FIGURE 28: MATLAB® DIGITAL IMPLEMENTATION FOR THE PSFB CONVERTER (FROM MATLAB FILE)

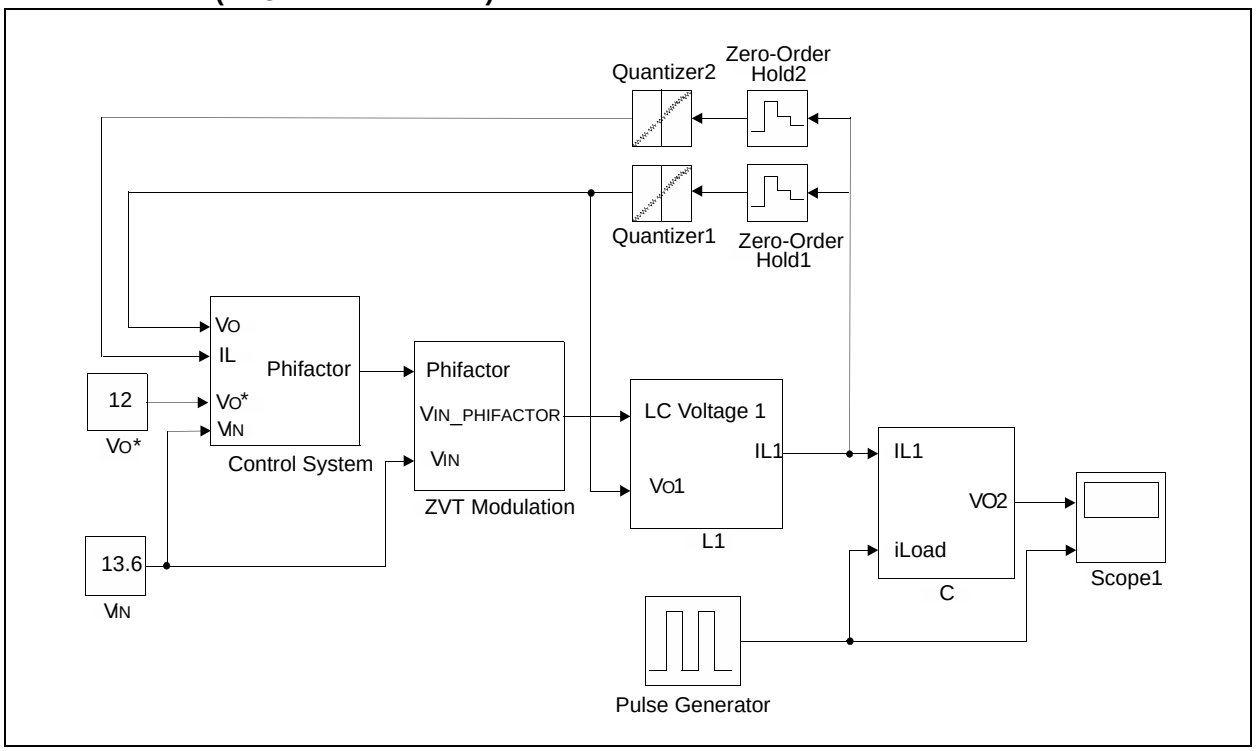
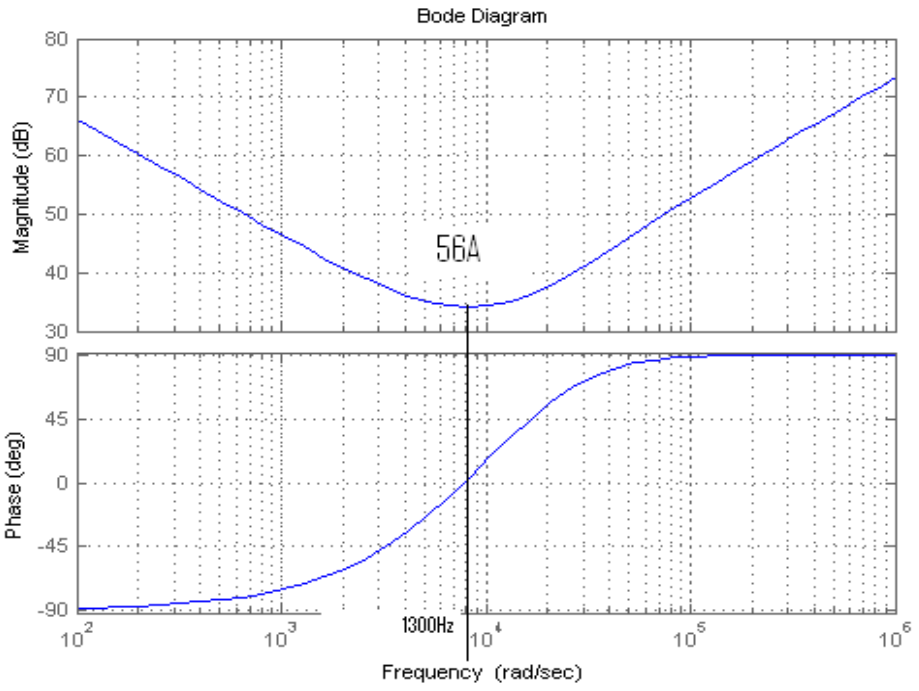


FIGURE 29: DISTURBANCE REJECTION PLOT



The loop gain voltage plot illustrated in Figure 30 is used to calculate the phase and gain margin. In the plot, the phase margin (difference between 180º and the phase angle where the gain curve crosses 0 db) is 50º. To prevent the system from being conditionally unstable, it is imperative that the gain plot drops below 0 db when the phase reaches 180º.

The blue curve is for the analog implementation and the green curve is for the digital implementation.

It is generally recommended to have a phase margin of at least 40º to allow for parameter variations. The gain margin is the difference between gain curve at 0 db and where the phase curve hits 180º. The gain margin (where the green line on the phase plot reaches 180º) is -20 db.

FIGURE 30: LOOP GAIN PLOT

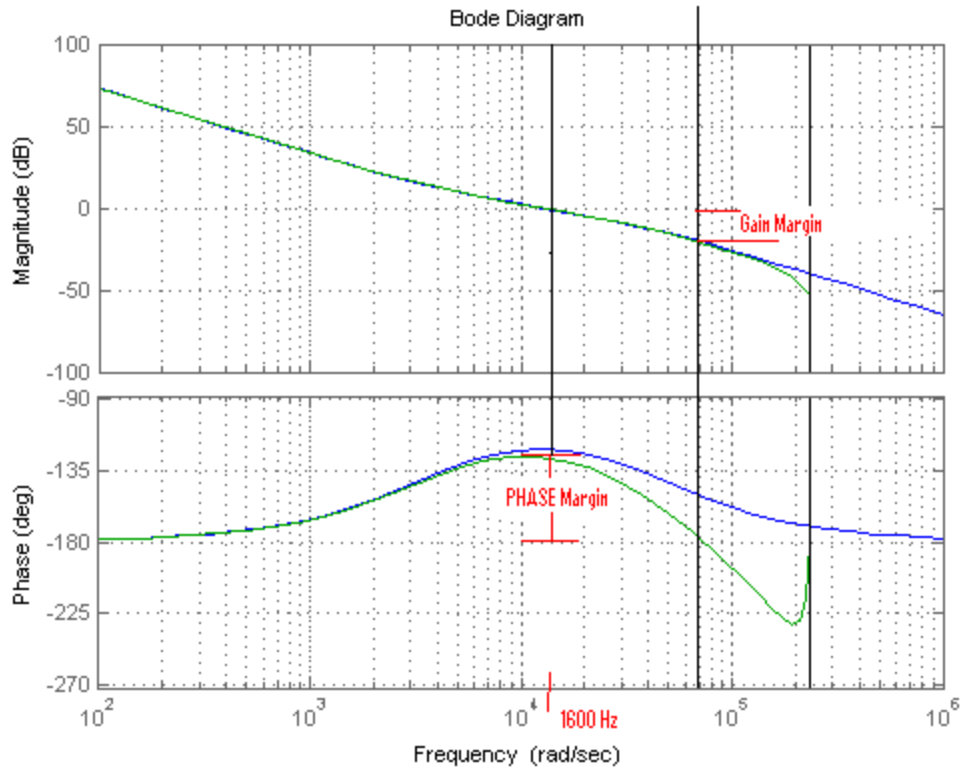
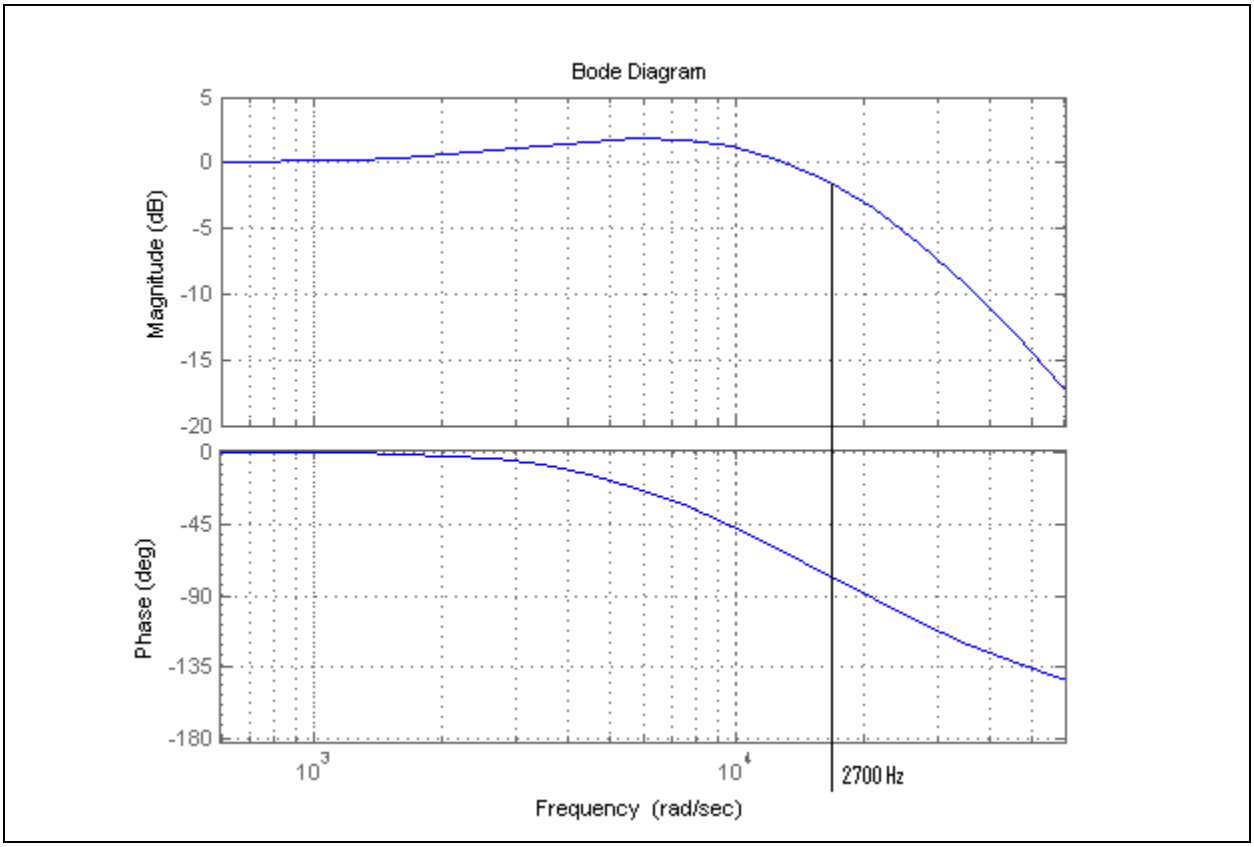


Figure 31 illustrates the closed loop Bode plot. The point where the gain crosses -3 db or -45º in phase is usually denoted as the bandwidth. In this system, the bandwidth of the voltage loop is approximately 2700 Hz (17000 rad/s), which is closely matched by the Bode plot.

FIGURE 31: CLOSED LOOP PLOT



SOFTWARE IMPLEMENTATION

The Quarter Brick DC/DC Converter is controlled using the dsPIC33FJ16GS502 device. This device controls the power flow in the converter, fault protection, soft start, remote ON/OFF functionality, external communication, adaptive control for the synchronous MOSFET's and single wire load sharing.

Note:	For more information on this device, refer to the *"dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet"* (DS70318). For information on the peripherals, refer to **Section 43. "High-Speed PWM"** (DS70323), **Section 44. "High-Speed 10-Bit Analog-to-Digital Converter (ADC)"** (DS70321), and **Section 45. "High-Speed Analog Comparator"** (DS70296) in the *"dsPIC33F/PIC24H Family Reference Manual"*. These documents are available from the MIcrochip website (www.microchip.com).

Description of Software Functional Blocks

The source files and header files describe the functions used in the software.

Source Files

Main_CMC.c

Functions present in this file are:

main()

Configures the operating frequency of the device.

Configures the auxiliary clock module.

Calls functions for configuring GPIO, ADC and PWM modules.

Checks for fault status.

ADCP1Interrupt()

Read values of currents and voltages.

Check for any fault condition.

If fault does not exist, execute the control loop.

If fault exists, disable PWM outputs.

INT1Interrupt()

Remote ON/OFF functionality.

T1Interrupt()

Averaging the PID output.

Over current limit selection.

Over temperature fault.

Init_CMC.c

Functions present in this file are:

init_PSFBDrive ()

Configure the primary MOSFET's PWM module.

init_SYNCRECTDrive ()

Configure the synchronous MOSFET's PWM module.

init_ADC()

Configure the ADC module.

InitRemoteON_OFF()

Configure the System state for remote ON/OFF functionality.

init_Timer1()

Configure Timer1.

Variables_CMC.c

Declarations and Initialization of all the global variables.

Compensator_CMC.c

DigitalCompensator(void)

Function to execute the voltage PI compensator and current P compensator.

LoadshareCompensator(void)

Function to execute the load share PI compensator.

delay.s

`_Delay` to get ms delay.

`_Delay_Us` to get µs delay.

Header Files

Define_CMC.h

This file has all the global function prototype definitions and global parameter definitions.

This is the file where all the modifications must be done based on the requirements of hardware components, power level, control loop bandwidth and other parameters. They are given below for reference.

Variables_CMC.h

Supporting file for `Variables_CMC.c` and contains all the external global definitions.

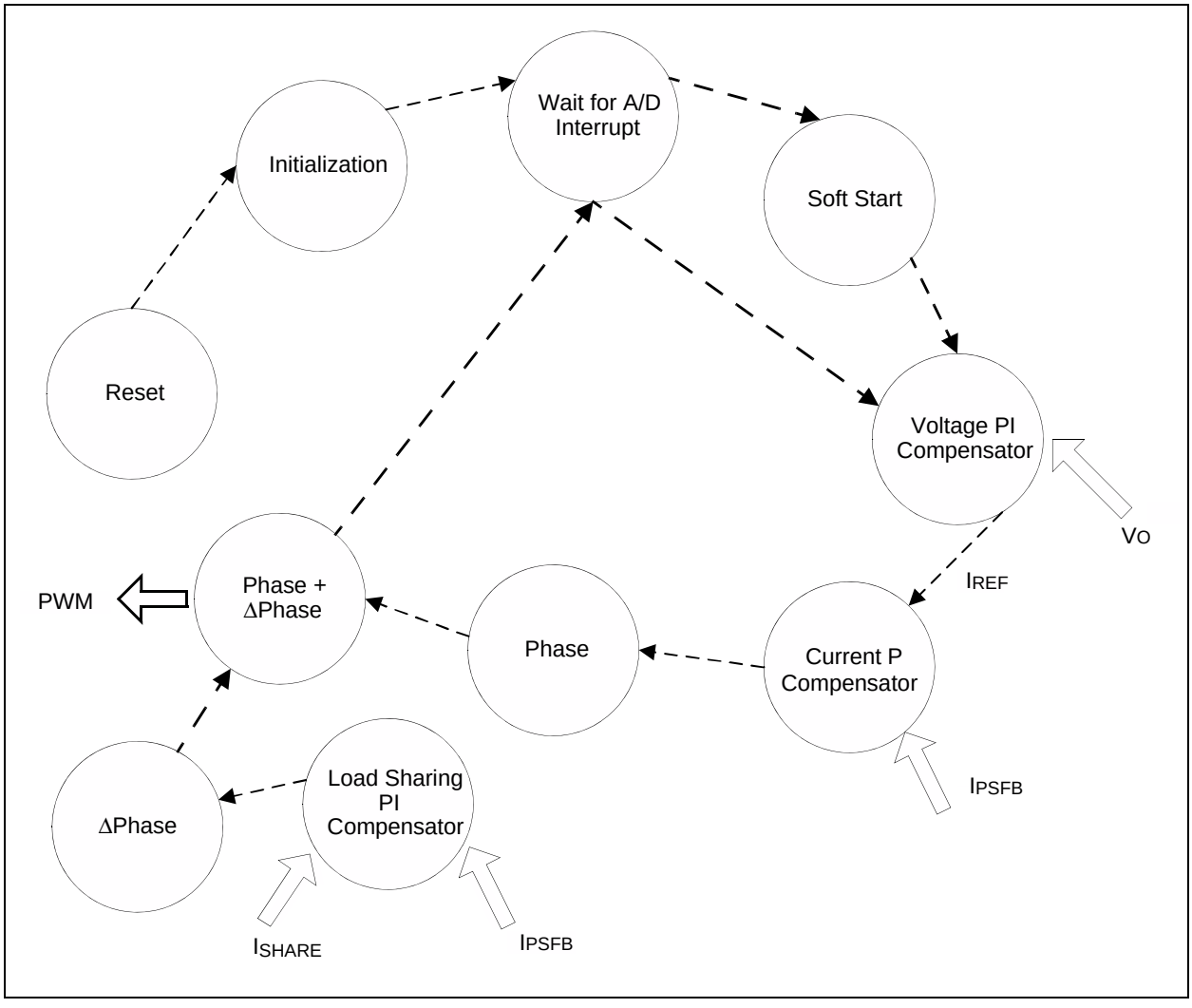
dsp.h

Standard library file for all DSP related operations.

delay.h

Presentable delay definition in ms and µs.

FIGURE 32: SOFTWARE FLOW CONTROL CMC WITH LOAD SHARING



Digital Nonlinear Implementations

DSCs allow implementing customized configurations to gain performance improvements of the SMPS.

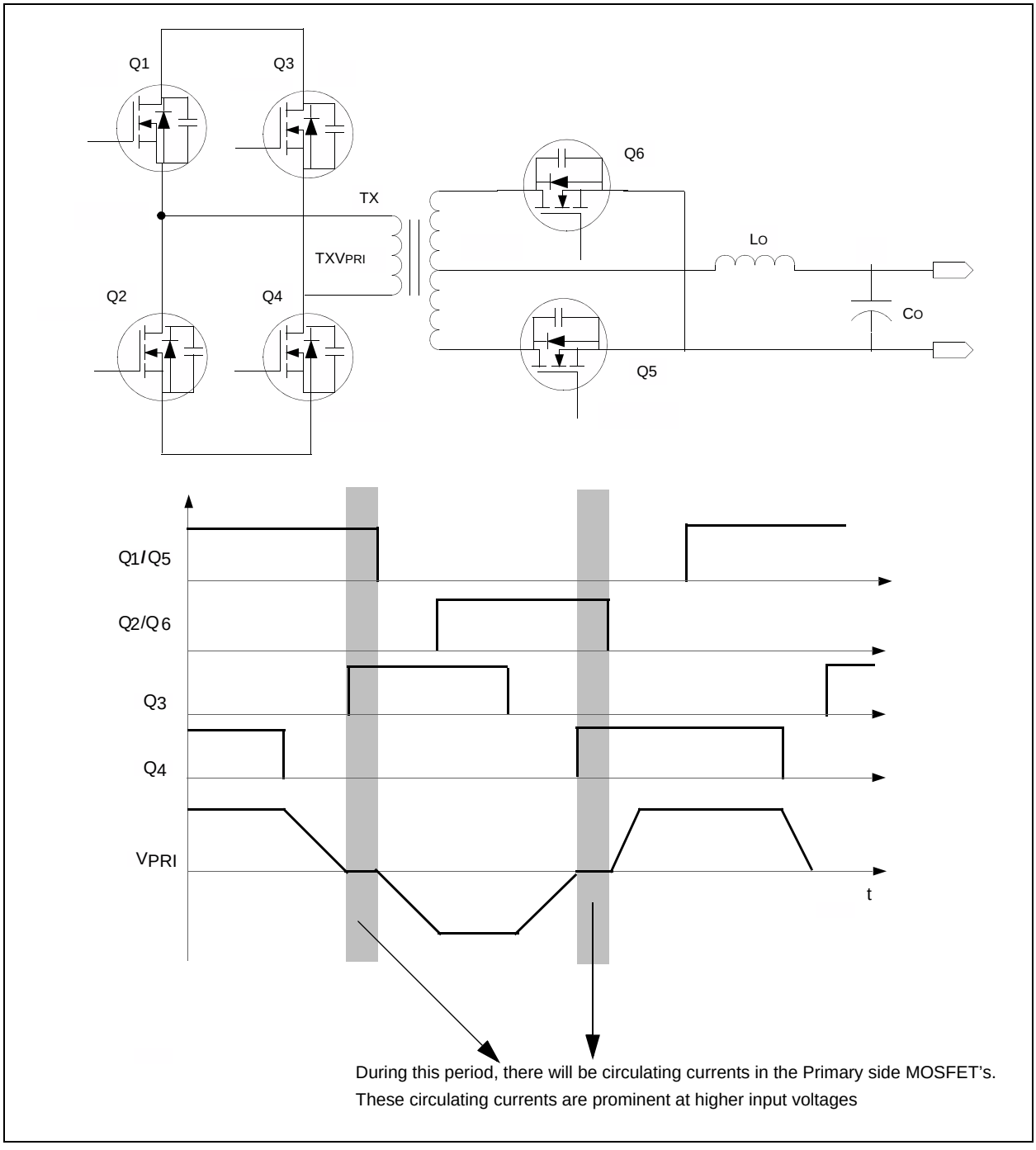
Adaptive Control to Improve the Efficiency

Achieving ultra high efficiency specifications in power supply designs require unique configuration of PWM. This can be achieved by using external hardware or with software in digital controllers. In the PSFB converter, the software is designed to get the efficiency benefit at higher specified input voltages.

Most of the DC/DC converters (part of AC/DC converter/Brick DC/DC converter) are designed using the isolation transformer for user safety and is also imposed by regulatory bodies. These power supplies are designed primary with push-pull, half-bridge, full-bridge and PSFB, in the secondary with synchronous MOSFET configurations to gain high efficiency.

To avoid cross conduction, there will be a defined dead band and during this period neither of the synchronous MOSFET's conduct so, the current will take the path of MOSFET body diode. These MOSFET body diodes has high forward drop compared to the $R_{DS}(ON)$ of the MOSFET, that is, $V_F * I >> I_{RMS}^2 * R_{DS}(ON)$. Therefore, the losses are higher and the efficiency is less.

FIGURE 33: FULL-BRIDGE CONVERTER WITH CONVENTIONAL SYNCHRONOUS MOSFET GATE DRIVES

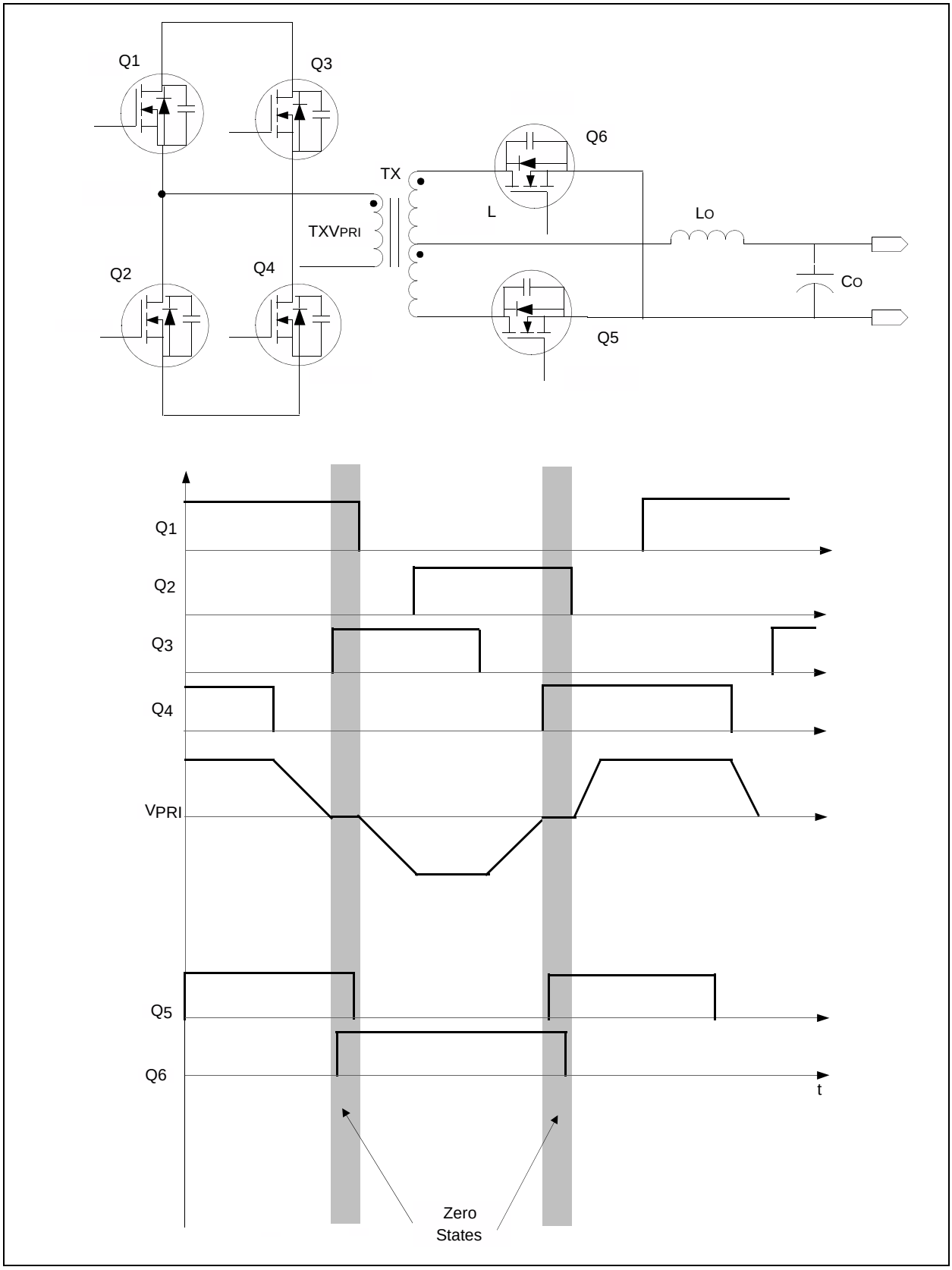


These problems can be overcome by unique configuration of PWM gate drive of the synchronous MOSFETs.

To control the output voltage of the converter with variation of input voltage, the duty cycle/phase is controlled. At high input voltages, the energy transfer from primary side to secondary side will be in small portions of the total period (zero states will exist). Due to the presence of inductors in secondary side of the converter, current continues to flow through the transformer coils through the MOSFET's channel or through MOSFET body diodes. Due to reflection of current from secondary to primary, there will be a circulating current during the zero states in the primary and particularly this will be predominant at higher input voltage than the nominal input voltages of the input voltage range.

Losses occurring during zero state of the primary side of the transformer can be avoided by overlapping the PWM gate drive of the synchronous MOSFETs. This method solves the problems which cause losses during zero states of the transformer.

FIGURE 34: FULL-BRIDGE CONVERTER WITH OVERLAP OF SYNCHRONOUS MOSFET GATE DRIVES



MOSFET body diode conduction in the primary side of the transformer is stopped so there are no reflected currents from the secondary side. The secondary side coils conduct in a way that there are no circulating currents in the primary side, effectively cancellation of currents. If a center tapped configuration is used in the secondary side of the transformer, the two coils cancel the flux and no flux is linked to the primary side because of the cancellation of currents. In case of “synchronous current doubler configuration” in the secondary side, both the synchronous MOSFETS are ON and the current does not pass in secondary side coil of the transformer, and therefore there is no reflected current in the primary side of the converter. This drastically reduces the circulating current losses in primary side body diodes of the MOSFETs.

- In the case of center tapped transformer secondary configuration, instead of one synchronous MOSFET and one coil of the center tapped transformer, two synchronous MOSFETS and two transformer coils conduct simultaneously. Therefore, the secondary current will have only half the effective resistance, and the losses are reduced by half compared to when only one synchronous MOSFET is ON.
- In the conventional switching methodology, intentional dead time is introduced between the two synchronous MOSFETS and typically this may be 10% of switching period based on the designs. During this dead time, the high secondary current flows through the high forward drop body MOSFET and cause losses. By configuring the overlap of the PWM gate drive of the synchronous MOSFET, the high secondary currents flow through the channel of the MOSFET. In this instance there will be only R_{DS}(ON) losses that are very less compared to the losses incurred by the MOSFET body diodes in the dead time.

Overcurrent Protection Implementation

A current transformer is located in the primary side of the converter and the output of the current transformer also varies with the line conditions. To have the specific current limit across the line voltages, the compensator final output is averaged over a period of 10 ms. The compensator final output provides the line voltage variation data. This data is used as a modifier to change the current limit setting.

PRINTED CIRCUIT BOARD (PCB)

In the Quarter Brick DC/DC Converter design, an 18-layer PCB is used to achieve the standard quarter brick dimensions. The PCB tracks routing is a challenging task in the quarter brick converter design. The PCB layers are described in Table 8.

TABLE 8: Stacking of PCB Layers

PCB Layer	PCB Layer Description
1	Top layer traces, magnetic winding and component assembly.
2	Analog GND, magnetics and primary, and secondary side Cu pours.
3	
4	
5	
6	Analog GND, +3.3V, magnetics and primary, and secondary side Cu pours.
7	Analog GND, gate drive traces, magnetics and primary, and secondary side Cu pours.
8	Analog GND, magnetics and primary, and secondary side Cu pours.
9	
10	
11	Analog GND, DIG GND, magnetics and primary, and secondary side Cu pours.
12	Analog GND, DIG GND, gate drive traces, magnetics and primary, and secondary side Cu pours.
13	Analog GND, DIG GND, magnetics and primary, and secondary side Cu pours.
14	Analog GND, DIG GND, gate drive traces, magnetics and primary, and secondary side Cu pours.
15	Analog GND, DIG GND, magnetics and primary, and secondary side Cu pours.
16	Analog GND, DIG GND, magnetics and primary, and secondary side Cu pours.
17	Digital GND and signal traces, magnetics and primary, and secondary side Cu pours.
18	Bottom layer traces, magnetic winding and component assembly.

LABORATORY TEST RESULTS AND CIRCUIT SCHEMATICS

The Laboratory test results provide an overview of the quarter brick PSFB electrical specifications as well as the scope plots from initial test results. The test results are illustrated in Figure 35 to Figure 65.

FIGURE 35: OUTPUT VOLTAGE RIPPLE: 8.5A AT 75V

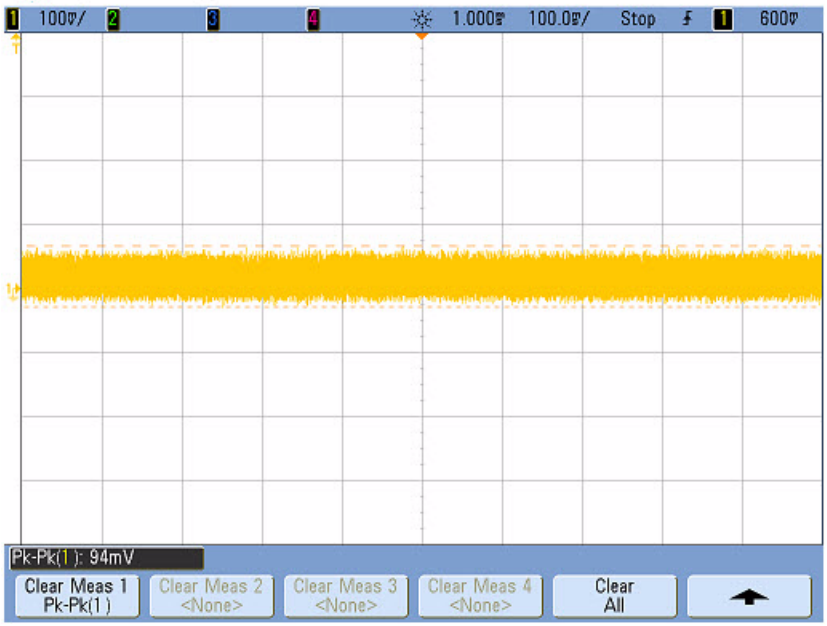


FIGURE 36: OUTPUT VOLTAGE RIPPLE: 17A AT 75V

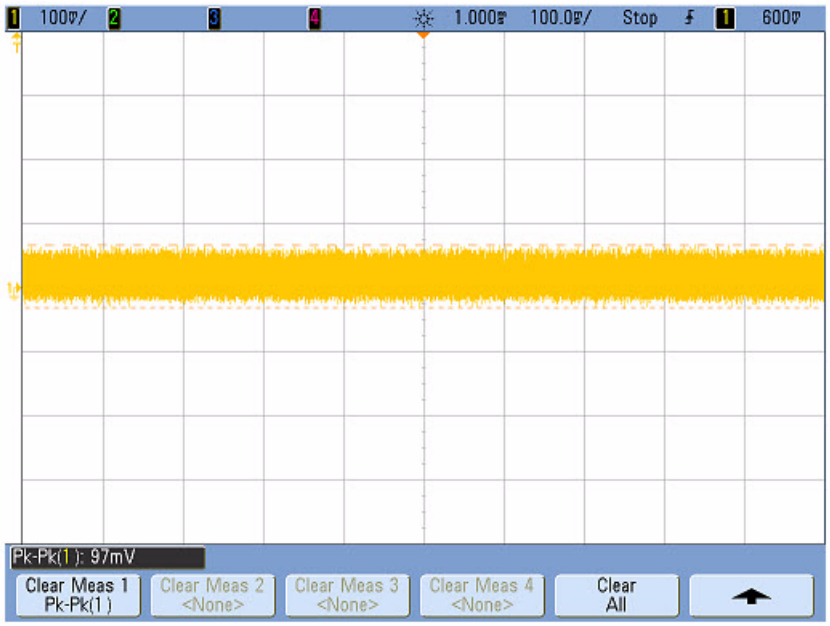


FIGURE 37: OUTPUT VOLTAGE RIPPLE: 0A AT 75V

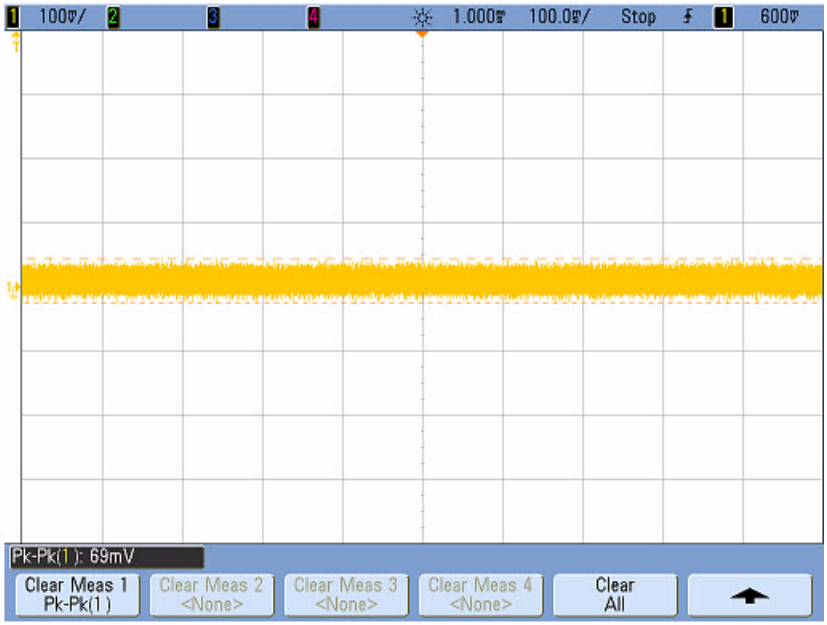


FIGURE 38: OUTPUT VOLTAGE RIPPLE: 8.5A AT 48V

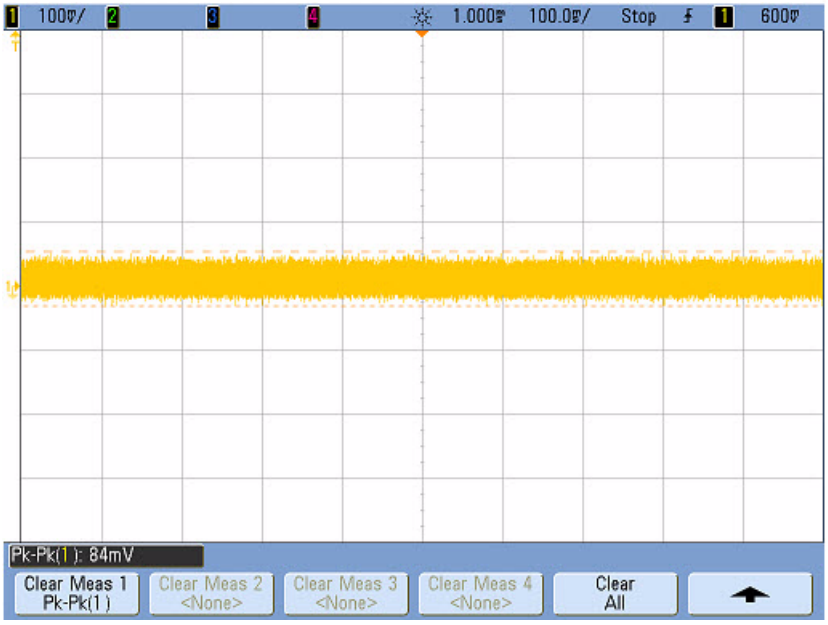


FIGURE 39: OUTPUT VOLTAGE RIPPLE: 17A AT 48V

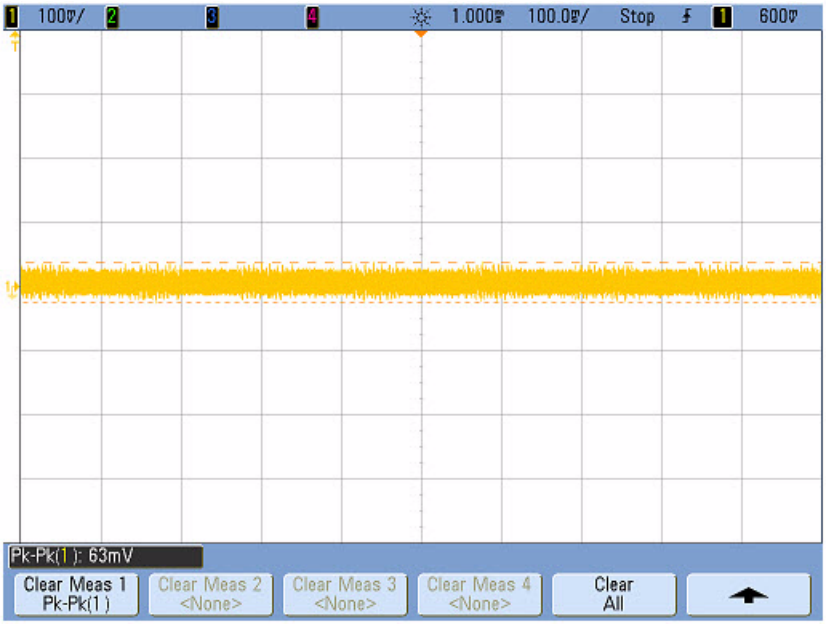


FIGURE 40: OUTPUT VOLTAGE RIPPLE: 0A AT 75V

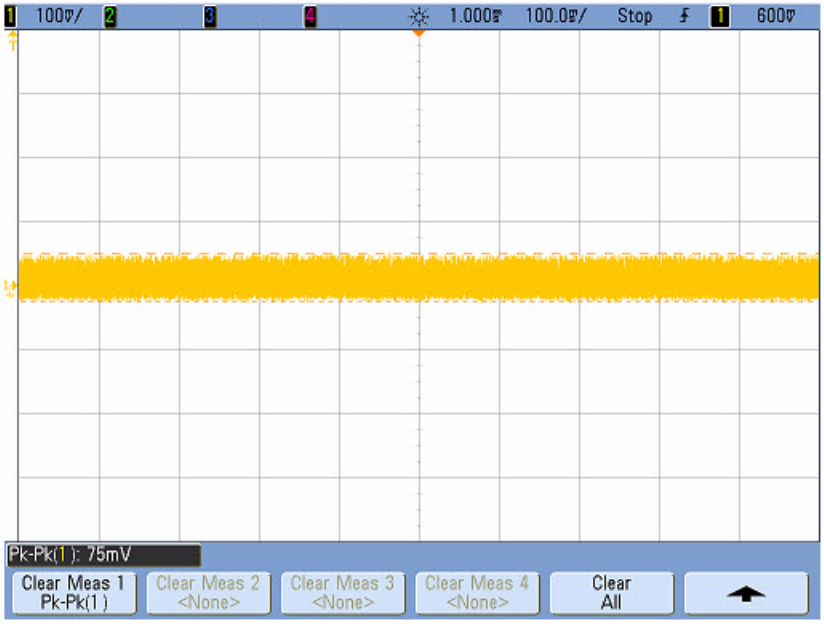


FIGURE 41: OUTPUT VOLTAGE RIPPLE: 8.5A AT 36V

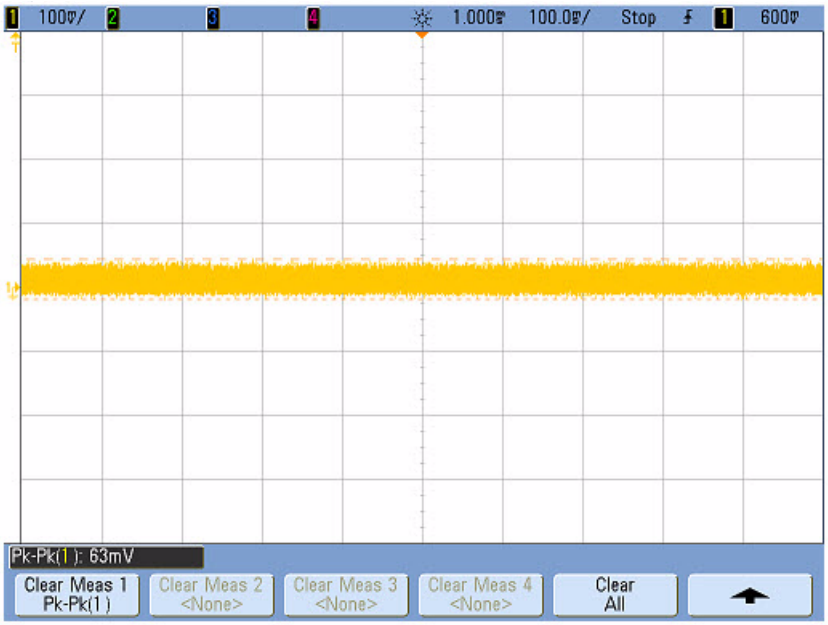


FIGURE 42: OUTPUT VOLTAGE RIPPLE: 17A AT 36V

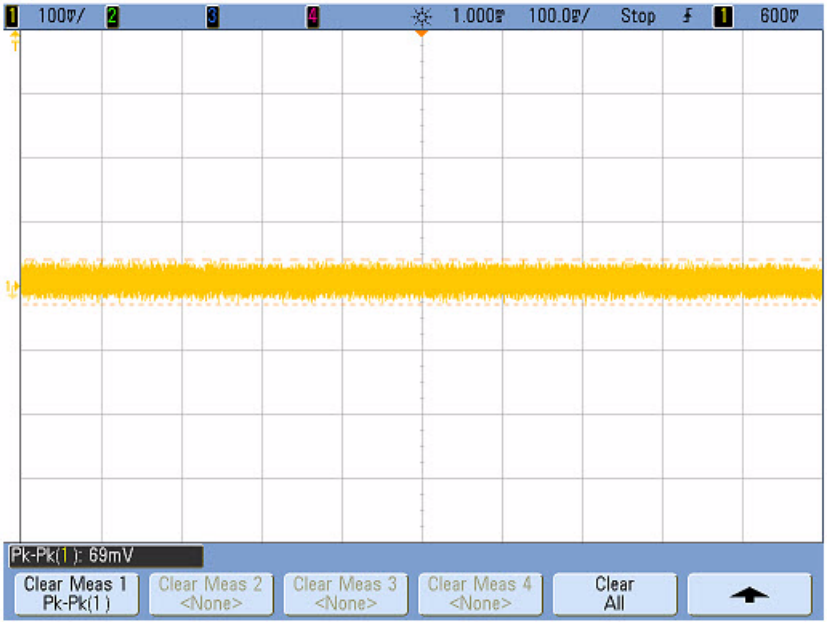


FIGURE 43: OUTPUT VOLTAGE TRANSIENT: 4.25A, 12.75A AT 48V

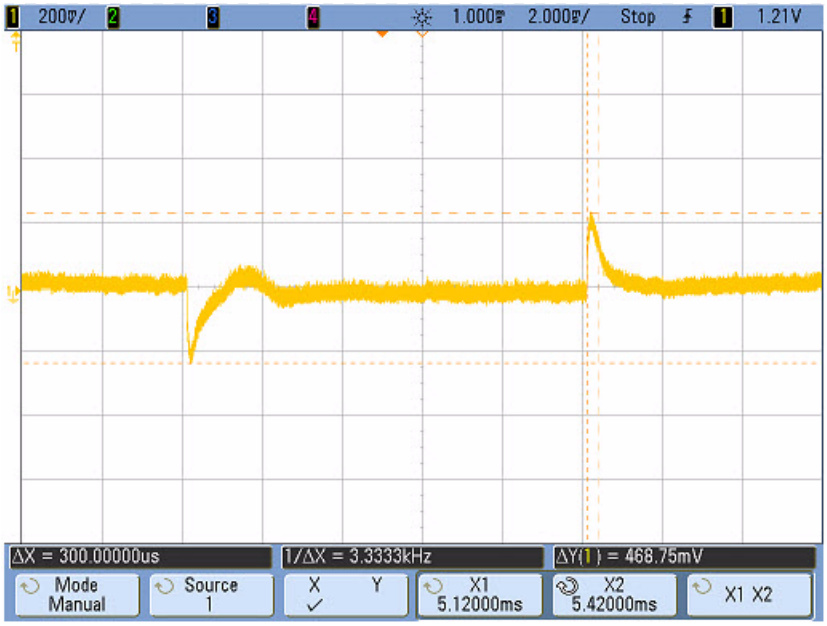


FIGURE 44: OUTPUT VOLTAGE TRANSIENT: 4.25A, 12.75A AT 75V

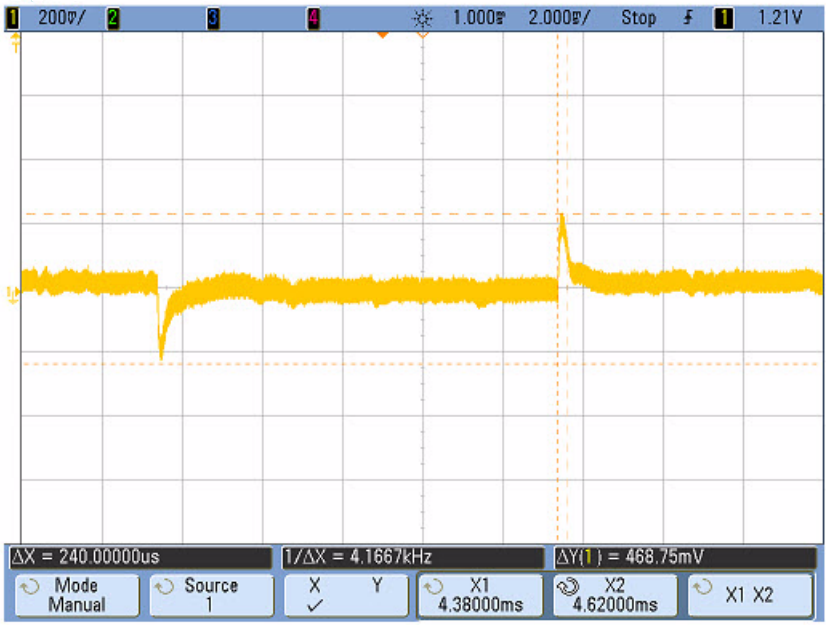


FIGURE 45: OUTPUT VOLTAGE TRANSIENT: 4.25A, 12.75A AT 36V

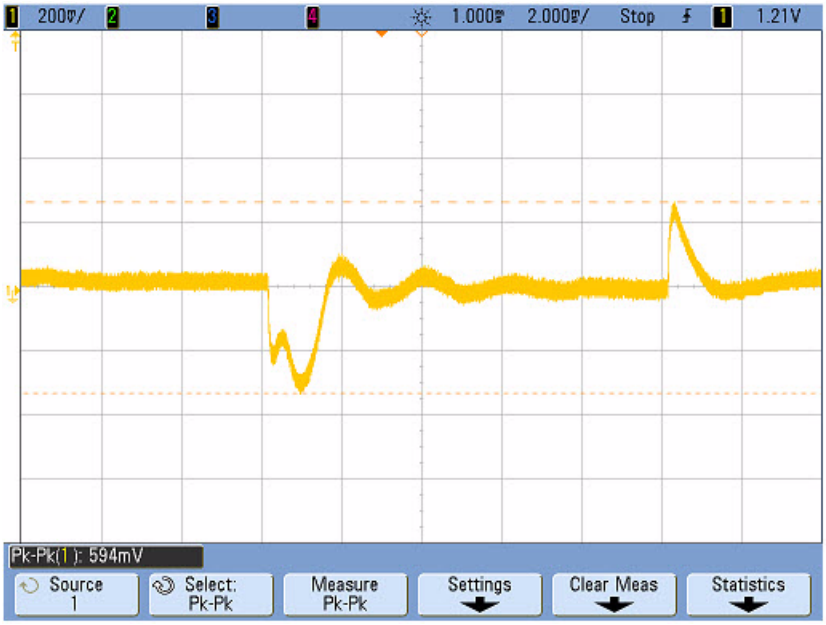
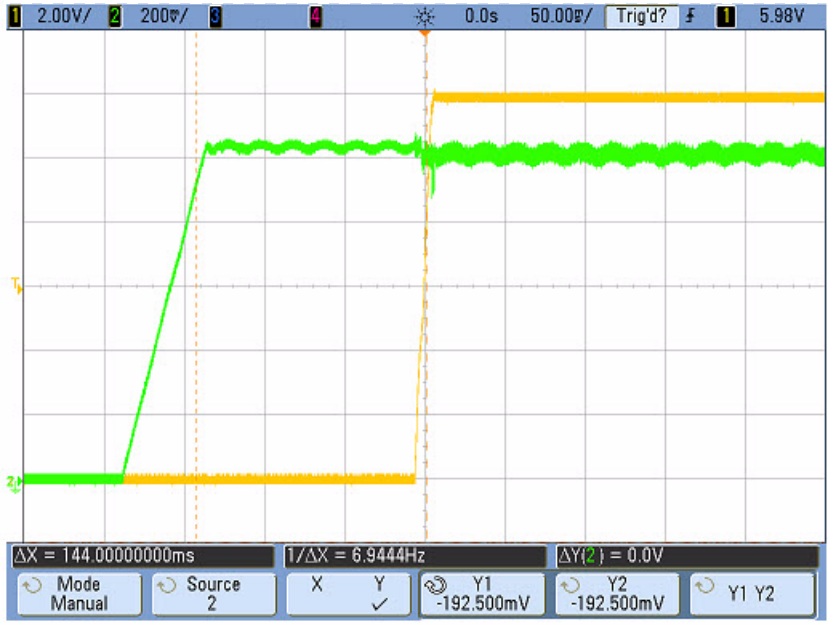


FIGURE 46: START-UP TIME: 8.5A AT 53V



Green Input Voltage

Yellow Output Voltage

FIGURE 47: OUTPUT VOLTAGE RAMP UP TIME: 17A AT 53V

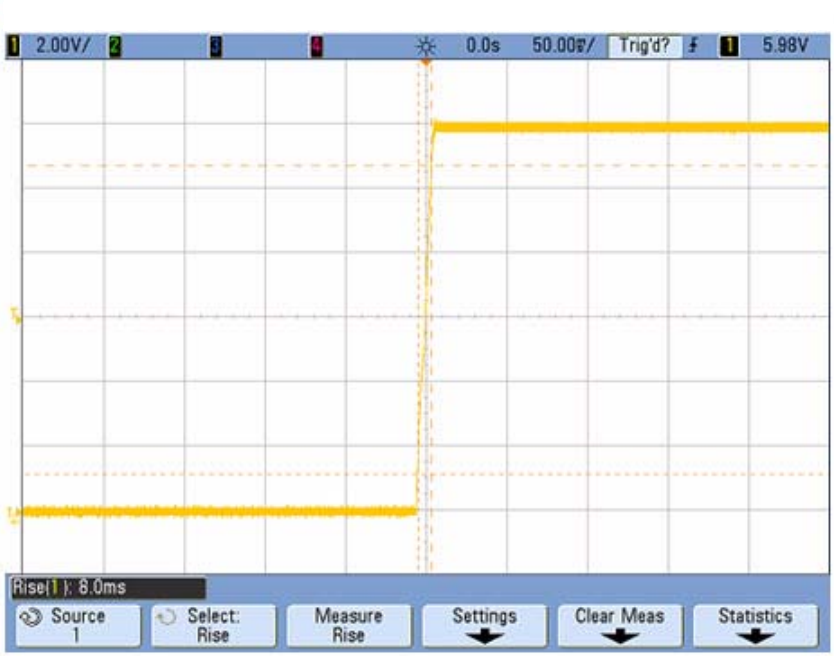


FIGURE 48: OUTPUT VOLTAGE RIPPLE: 8.5A AT 53V

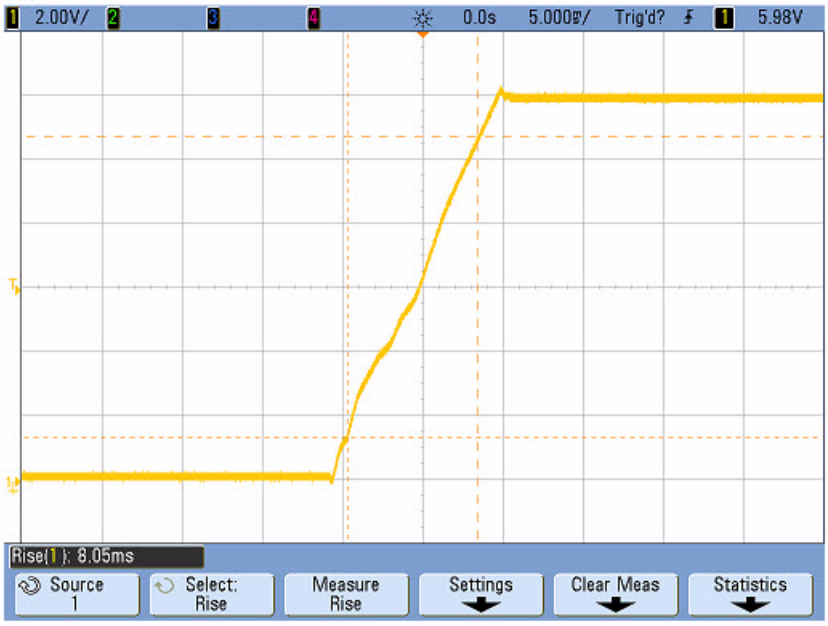


FIGURE 49: OUTPUT VOLTAGE OVERSHOOT: 8.5A AT 53V

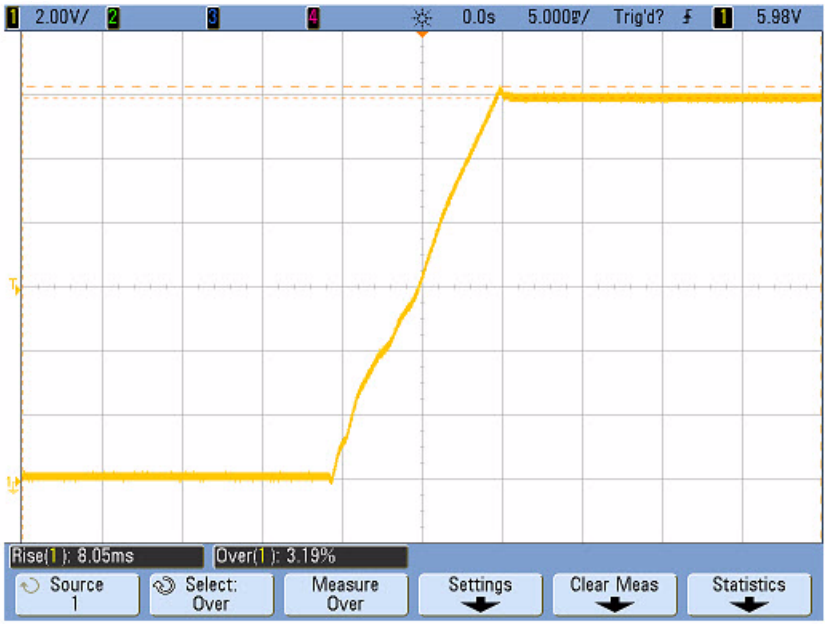
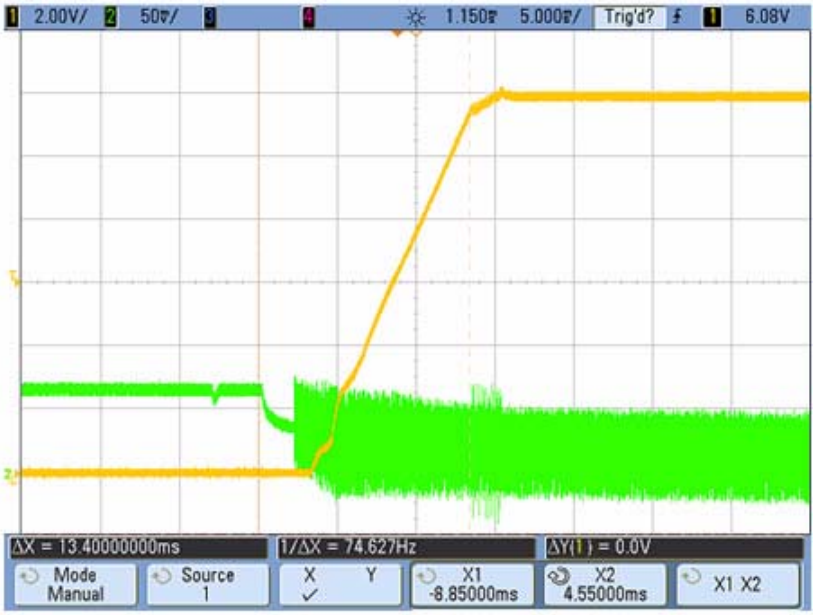


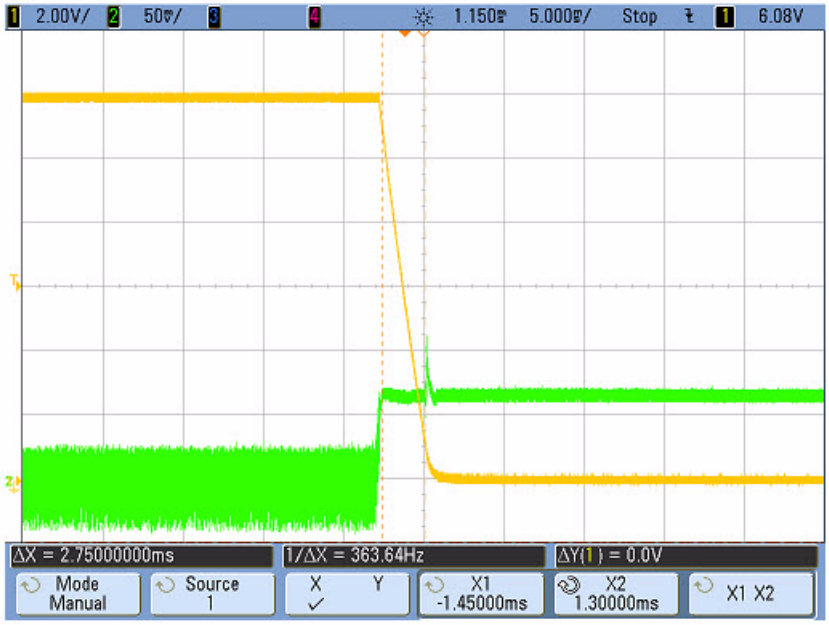
FIGURE 50: REMOTE ON/OFF, OUTPUT VOLTAGE RISE TIME: 17A AT 53V



Yellow Output Voltage

Green Remote Signal

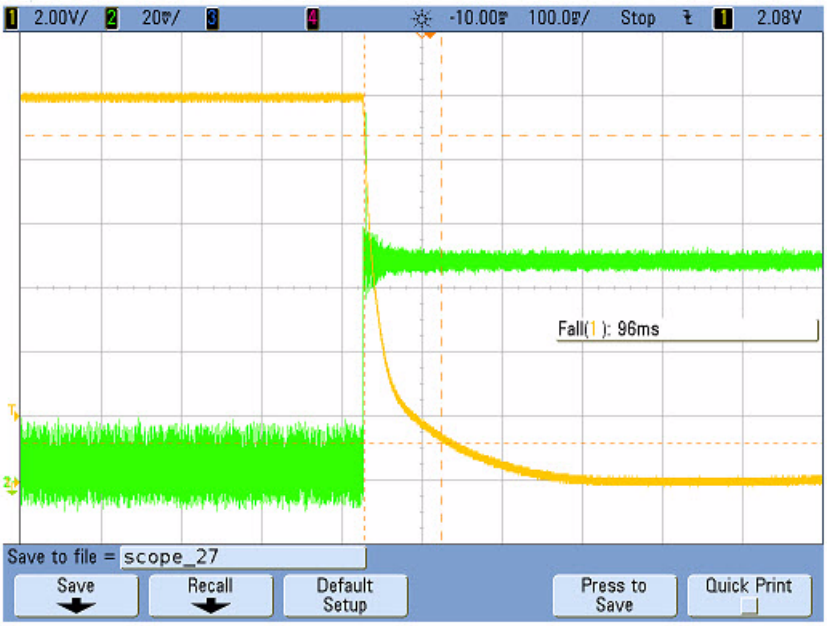
FIGURE 51: REMOTE ON/OFF, OUTPUT VOLTAGE FALL TIME: 17A AT 53V



Yellow Output Voltage

Green Remote Signal

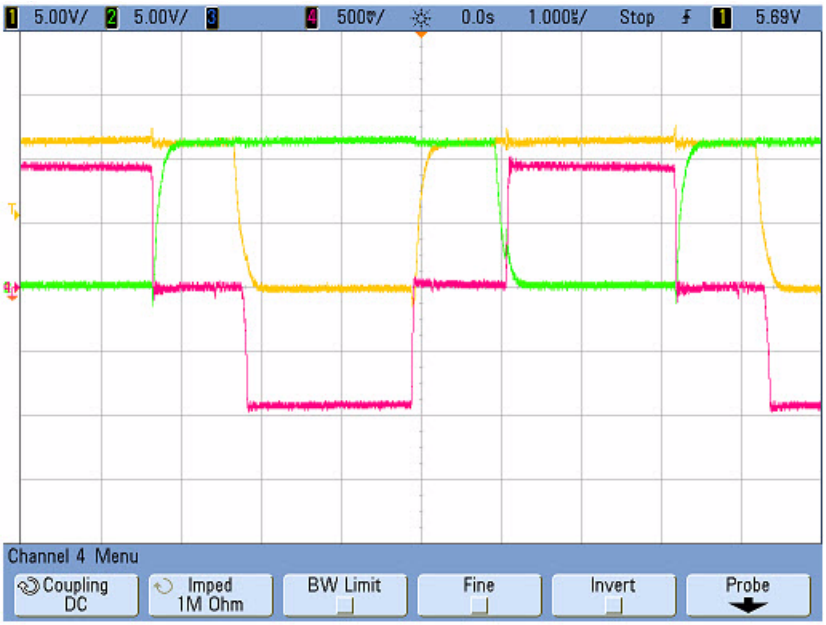
FIGURE 52: REMOTE ON/OFF, OUTPUT VOLTAGE FALL TIME: 0A AT 53V



Yellow Output Voltage

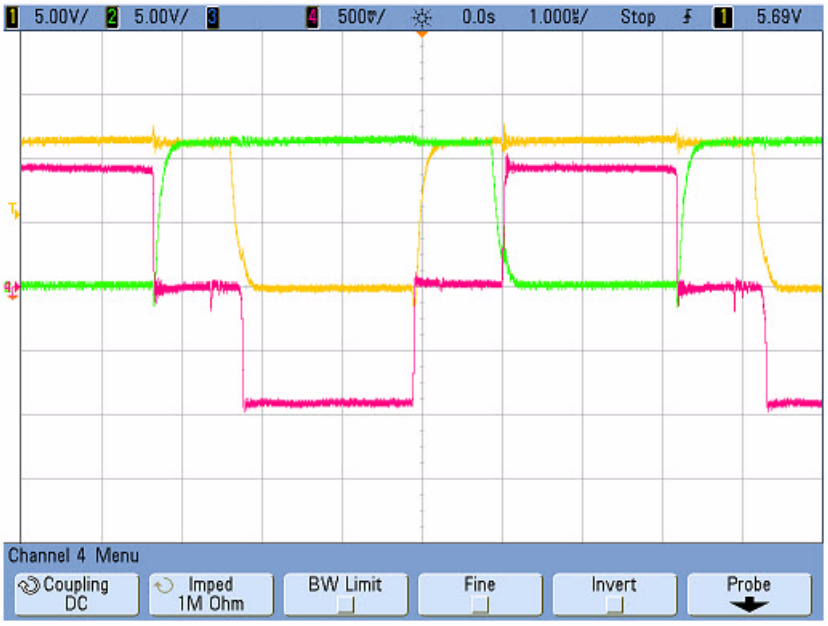
Green Remote Signal

FIGURE 53: PRIMARY TX AND SYNCHRONOUS FET GATE WAVEFORMS: 48V/8.5A



Yellow Q14 gate
Green Q13 gate
Pink Tx

FIGURE 54: PRIMARY TX AND SYNCHRONOUS FET GATE WAVEFORMS: 48V/17A



Yellow Q14 gate
Green Q13 gate
Pink Tx

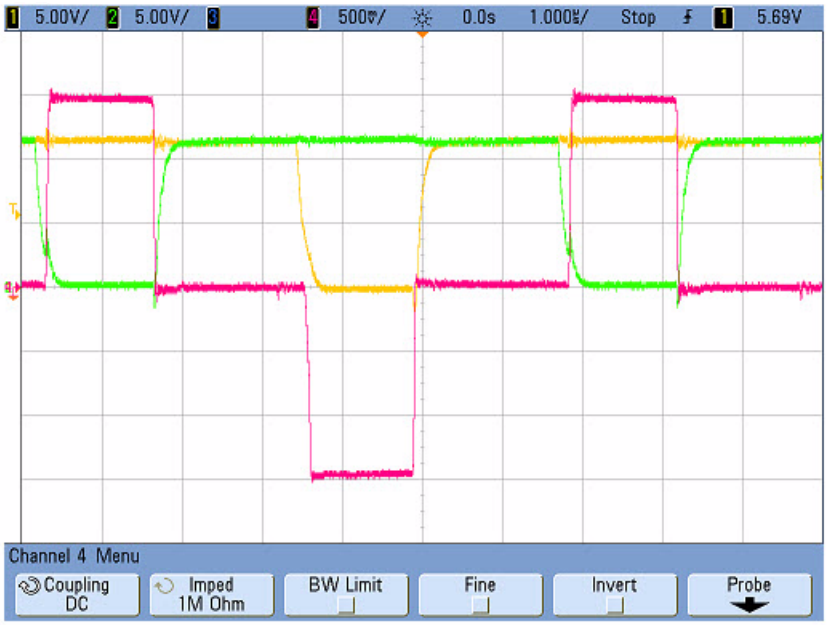
FIGURE 55: PRIMARY TX AND SYNCHRONOUS FET GATE WAVEFORMS: 48V/0A

Yellow Q14 gate

Green Q13 gate

Pink Tx

FIGURE 56: PRIMARY TX AND SYNCHRONOUS FET GATE WAVEFORMS: 76V/8.5A

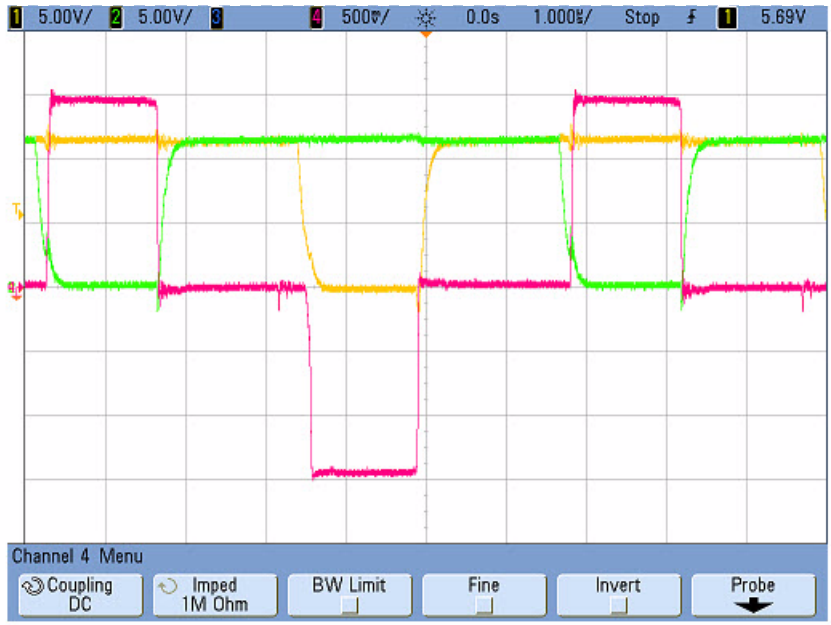


Yellow Q14 gate

Green Q13 gate

Pink Tx

FIGURE 57: PRIMARY TX AND SYNCHRONOUS FET GATE WAVEFORMS: 76V/17A



Yellow Q14 gate

Green Q13 gate

Pink Tx

FIGURE 58: PRIMARY TX AND SYNCHRONOUS FET GATE WAVEFORMS: 76V/0A

Yellow Q14 gate

Green Q13 gate

Pink Tx

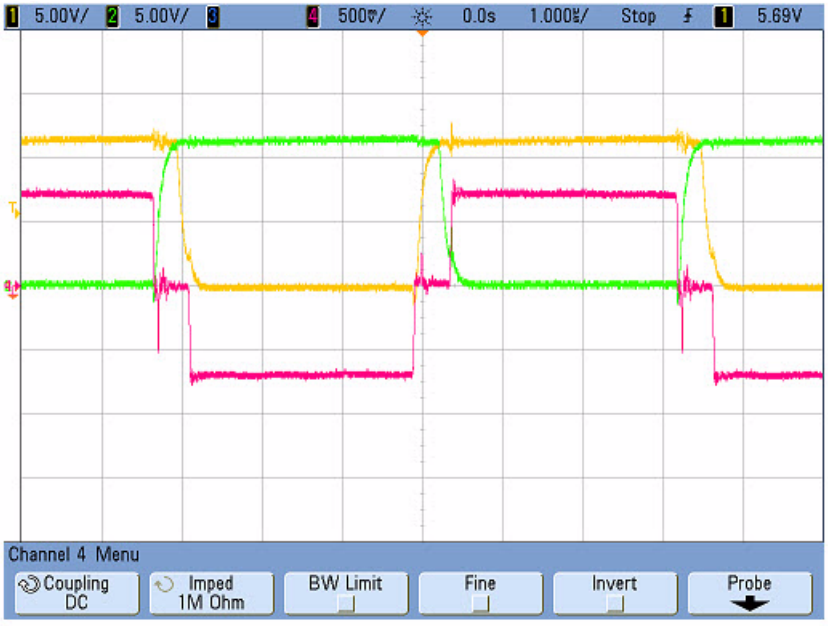
FIGURE 59: PRIMARY TX AND SYNCHRONOUS FET GATE WAVEFORMS: 36V/8.5A

Yellow Q14 gate

Green Q13 gate

Pink Tx

FIGURE 60: PRIMARY TX AND SYNCHRONOUS FET GATE WAVEFORMS: 36V/17A

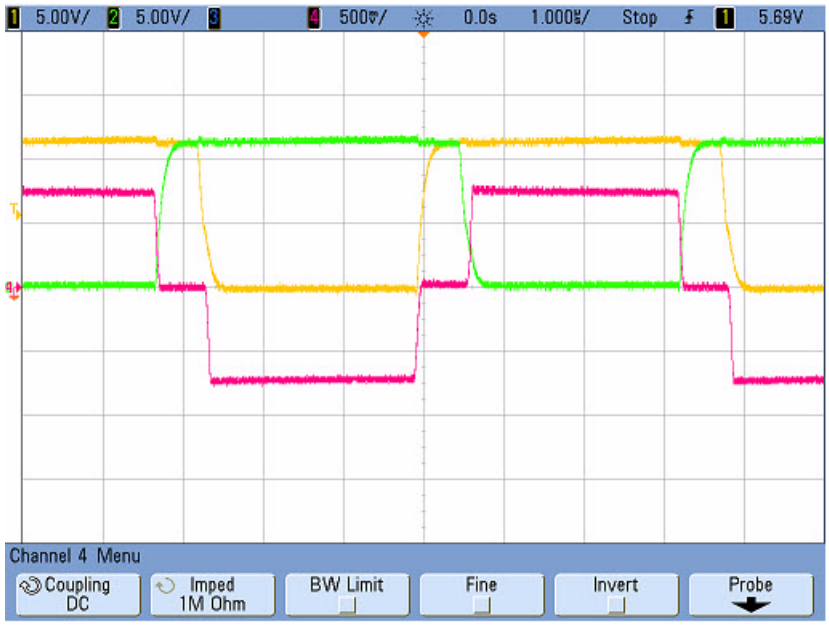


Yellow Q14 gate

Green Q13 gate

Pink Tx

FIGURE 61: PRIMARY TX AND SYNCHRONOUS FET GATE WAVEFORMS: 36V/0A

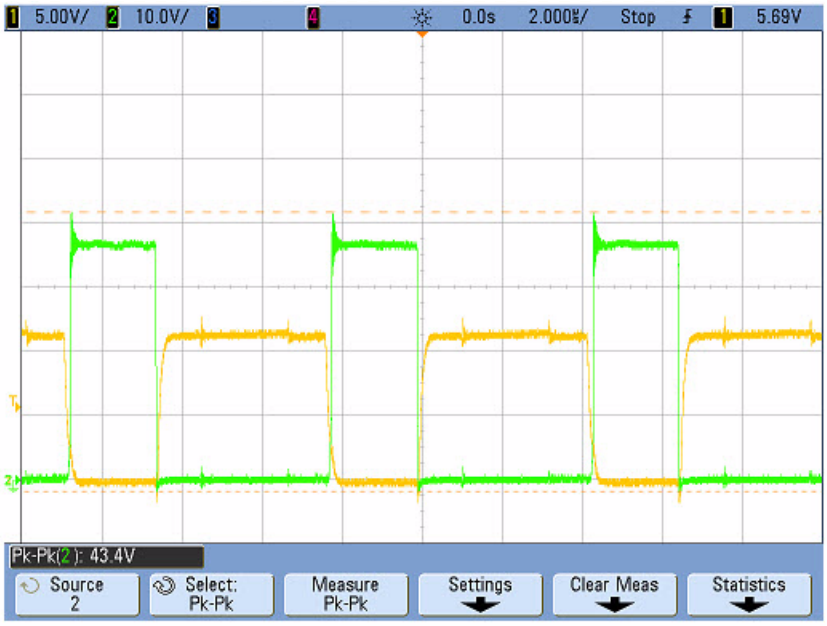


Yellow Q14 gate

Green Q13 gate

Pink Tx

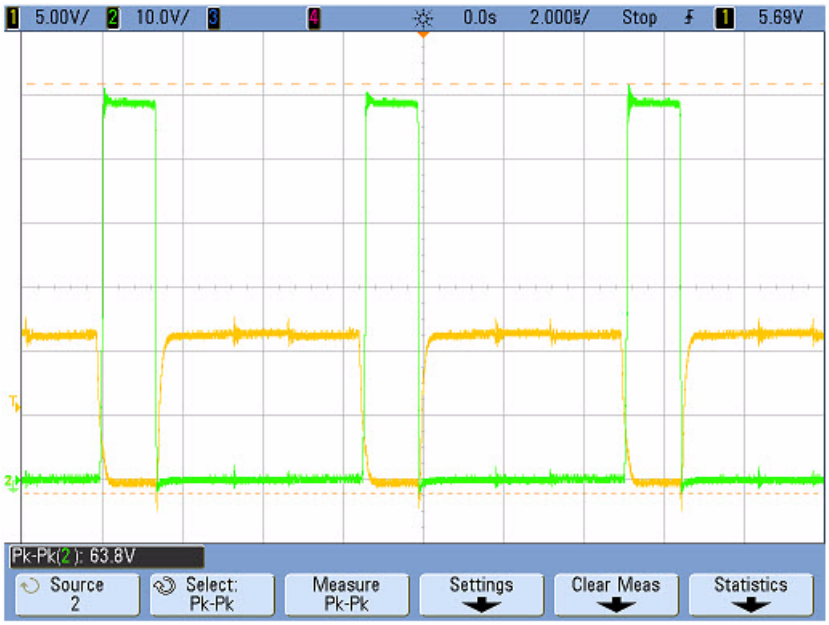
FIGURE 62: SYNCHRONOUS MOSFET GATE AND DRAIN WAVEFORM: 48V/17A



Yellow Q14 gate

Green Q14 drain

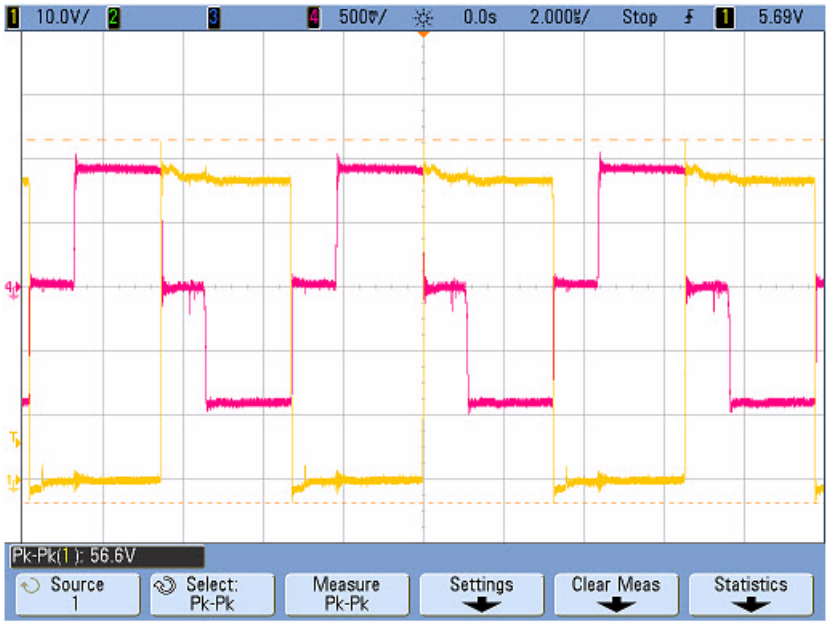
FIGURE 63: SYNCHRONOUS MOSFET GATE AND DRAIN WAVEFORM: 76V/17A



Yellow Q14 gate

Green Q14 drain

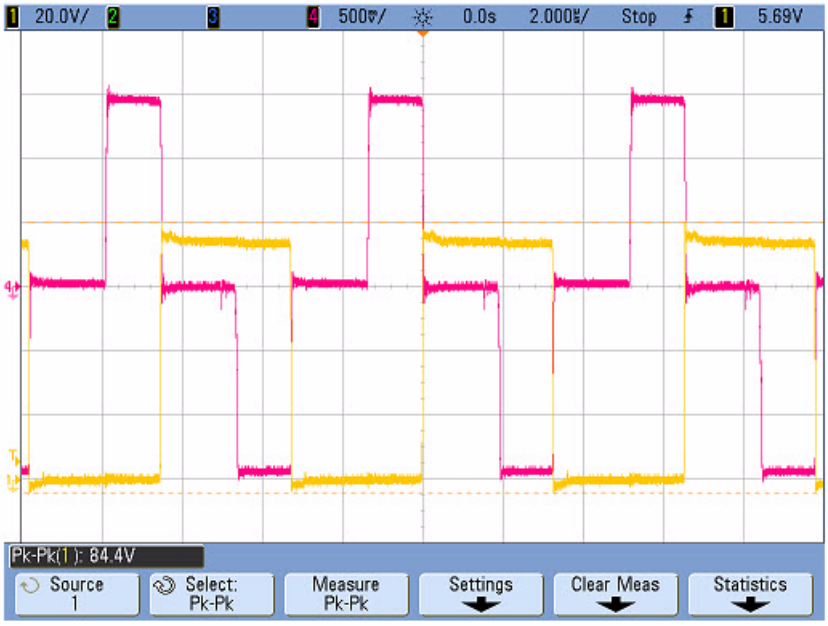
FIGURE 64: PRIMARY MOSFET GATE AND DRAIN WAVEFORM: 48V/17A



Yellow Q4 drain

Pink Tx

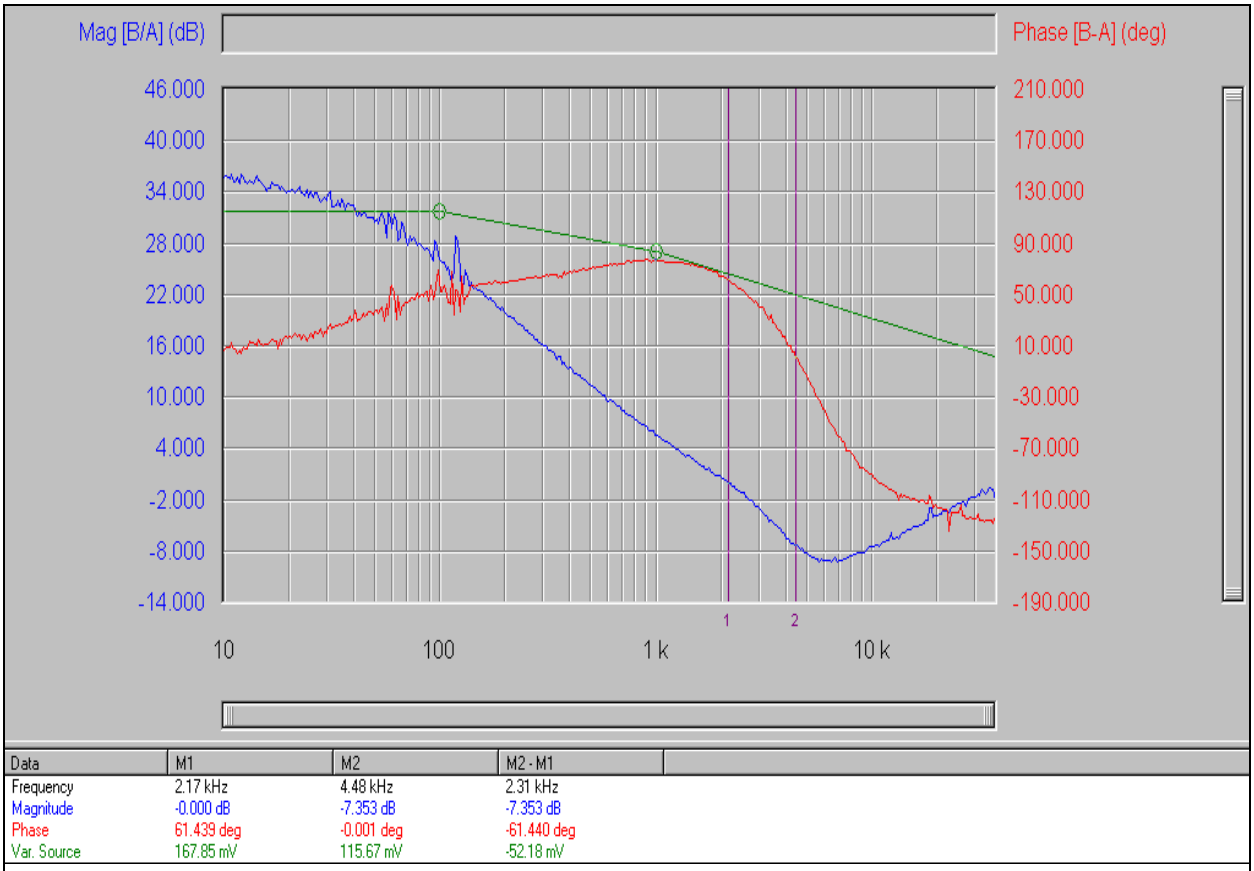
FIGURE 65: PRIMARY MOSFET GATE AND DRAIN WAVEFORM: 76V/17A



Yellow Q4 drain

Pink Tx

FIGURE 66: LOOP GAIN PLOT: 36V AND 12V/9A



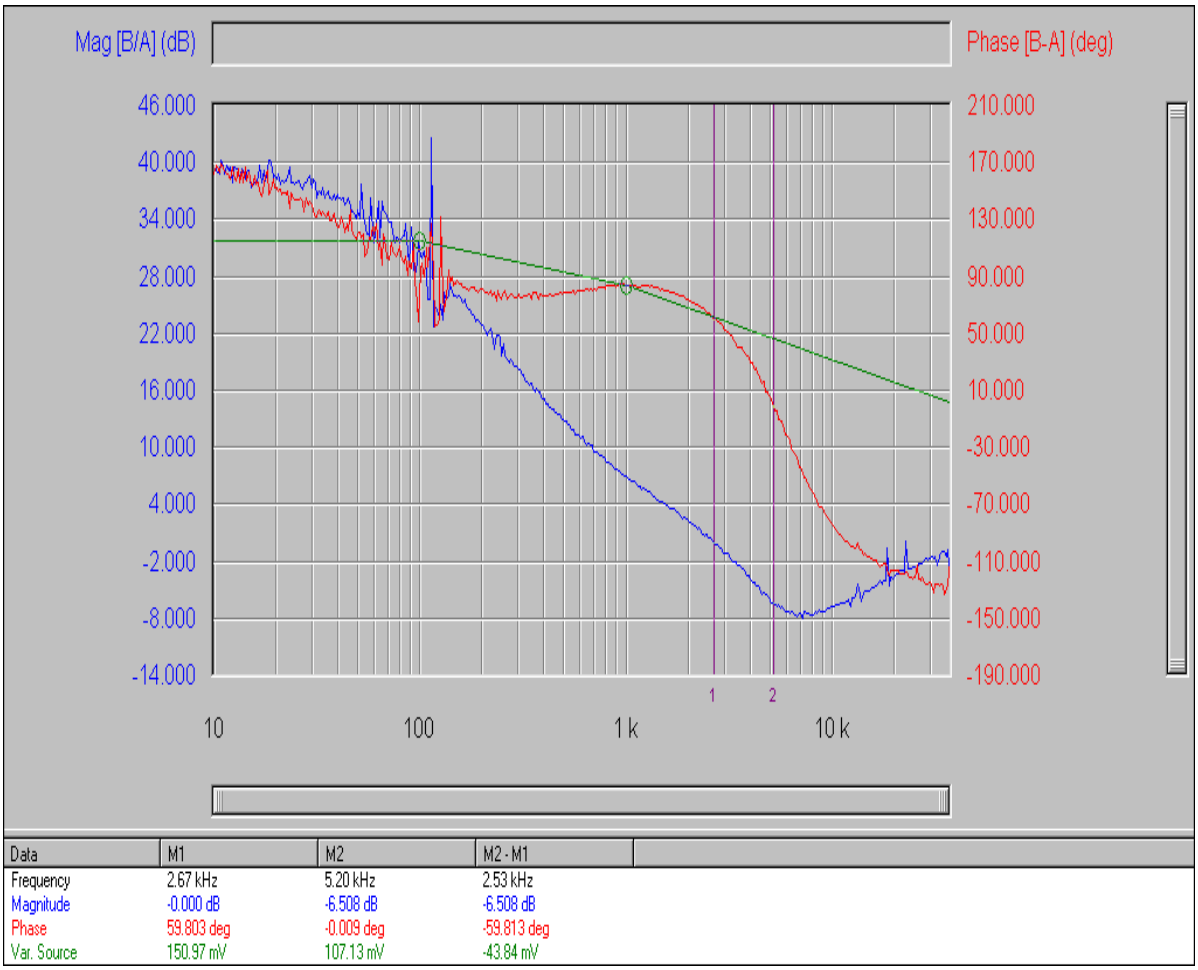
Data	M1	M2	M2 - M1
Frequency	2.17 kHz	4.48 kHz	2.31 kHz
Magnitude	-0.000 dB	-7.353 dB	-7.353 dB
Phase	61.439 deg	-0.001 deg	-61.440 deg
Var. Source	167.85 mV	115.67 mV	-52.18 mV

Phase Margin: 61.43^0

Gain Margin:-7.53 dB

Crossover frequency: 2.17 kHz

FIGURE 67: LOOP GAIN PLOT: 48V AND 12V/9A

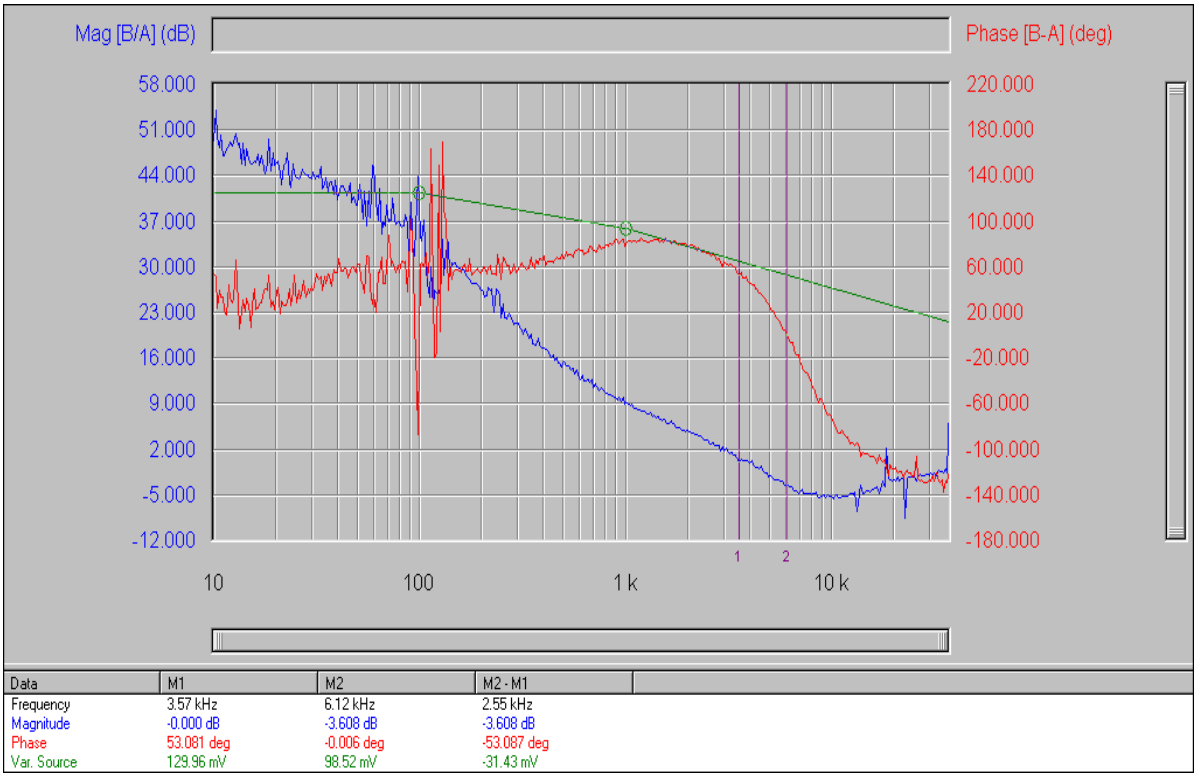


Phase Margin: 59.80^0

Gain Margin:-6.508 dB

Crossover frequency: 2.67 kHz

FIGURE 68: LOOP GAIN PLOT: 76V AND 12V/9A



Phase Margin: 53.08^0

Gain Margin:-3.60 dB

Crossover frequency: 3.57 kHz

CONCLUSION

This application note presents the design of a PSFB Quarter Brick DC/DC Converter through the average current mode control using a Microchip dsPIC “GS” family Digital Signal Controller (DSC). Various nonlinear techniques implemented in this design explore the benefits of DSCs in Switched Mode Power Converter applications.

Microchip has various resources to assist you in developing this integrated application. For more details on the PSFB Quarter Brick DC/DC Converter Reference Design using a dsPIC DSC, please contact your local Microchip sales office.

REFERENCES

The following resources are available from Microchip Technology Inc., and describe the use of dsPIC DSC devices for power conversion applications:

- *“dsPIC33FJ06GS101/X02 and dsPIC33FJ16GSX02/X04 Data Sheet”* (DS70318)
- Dedicated Switch Mode Power Supply (SMPS) Web site: http://www.microchip.com/SMPS

In addition, the following resource was used in the development of this application note:

“Design and Implementation of a Digital PWM Controller for a High-Frequency Switching DC-DC Power Converter”. Aleksandar Prodic, Dragan Maksimovic and Robert W. Erickson

APPENDIX A: SOURCE CODE

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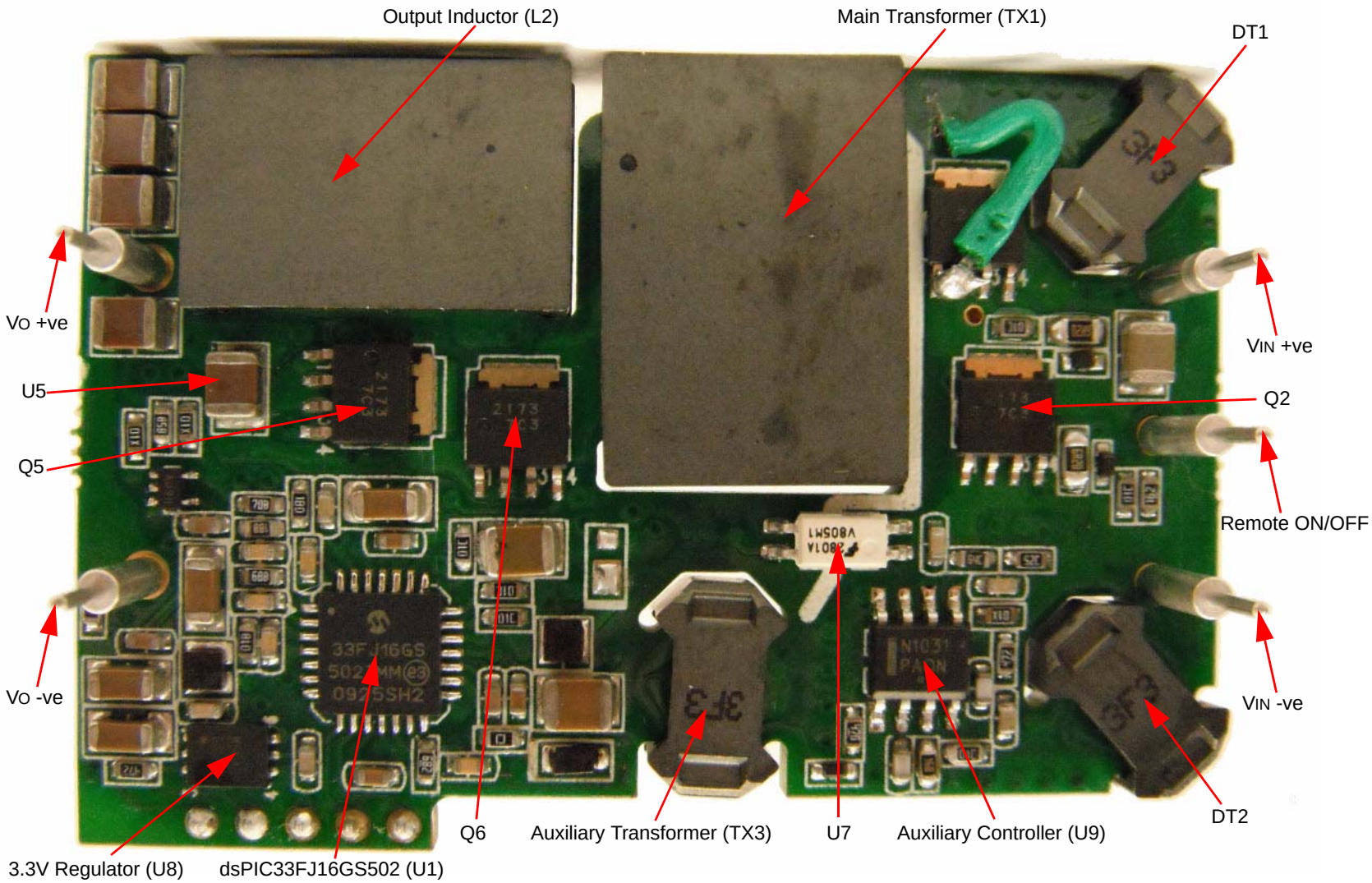
APPENDIX B: PSFB QUARTER BRICK DC/DC CONVERTER BOARD LAYOUT AND SCHEMATICS

FIGURE B-1: PSFB Quarter Brick DC/DC Converter Board Layout (Bottom View)



Note: This view lists a few key components. Refer to the Bottom Silk drawing in Figure B-2, which lists all board components.

FIGURE B-2: PSFB Quarter Brick DC/DC Converter Board Layout (Bottom Silk)

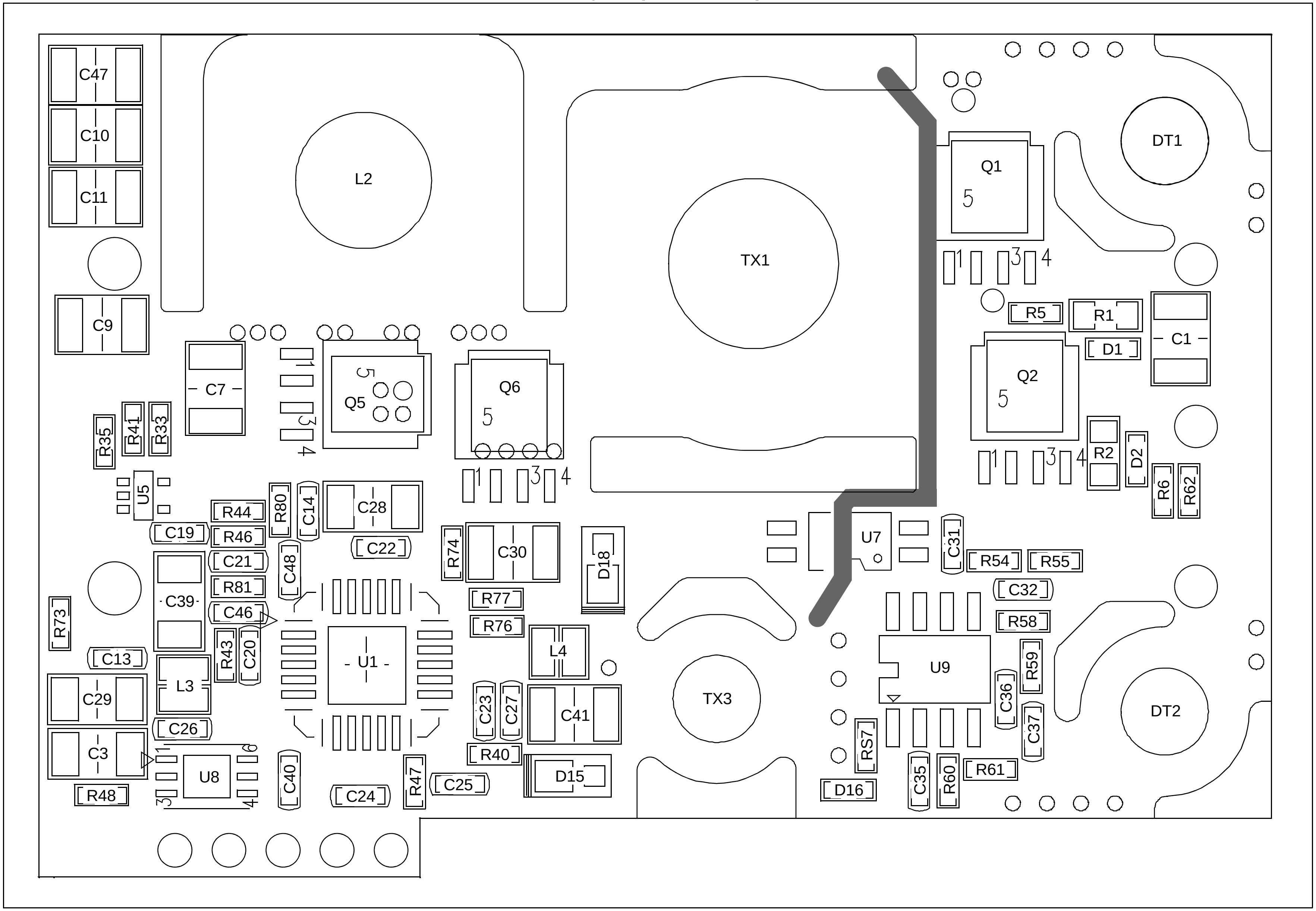
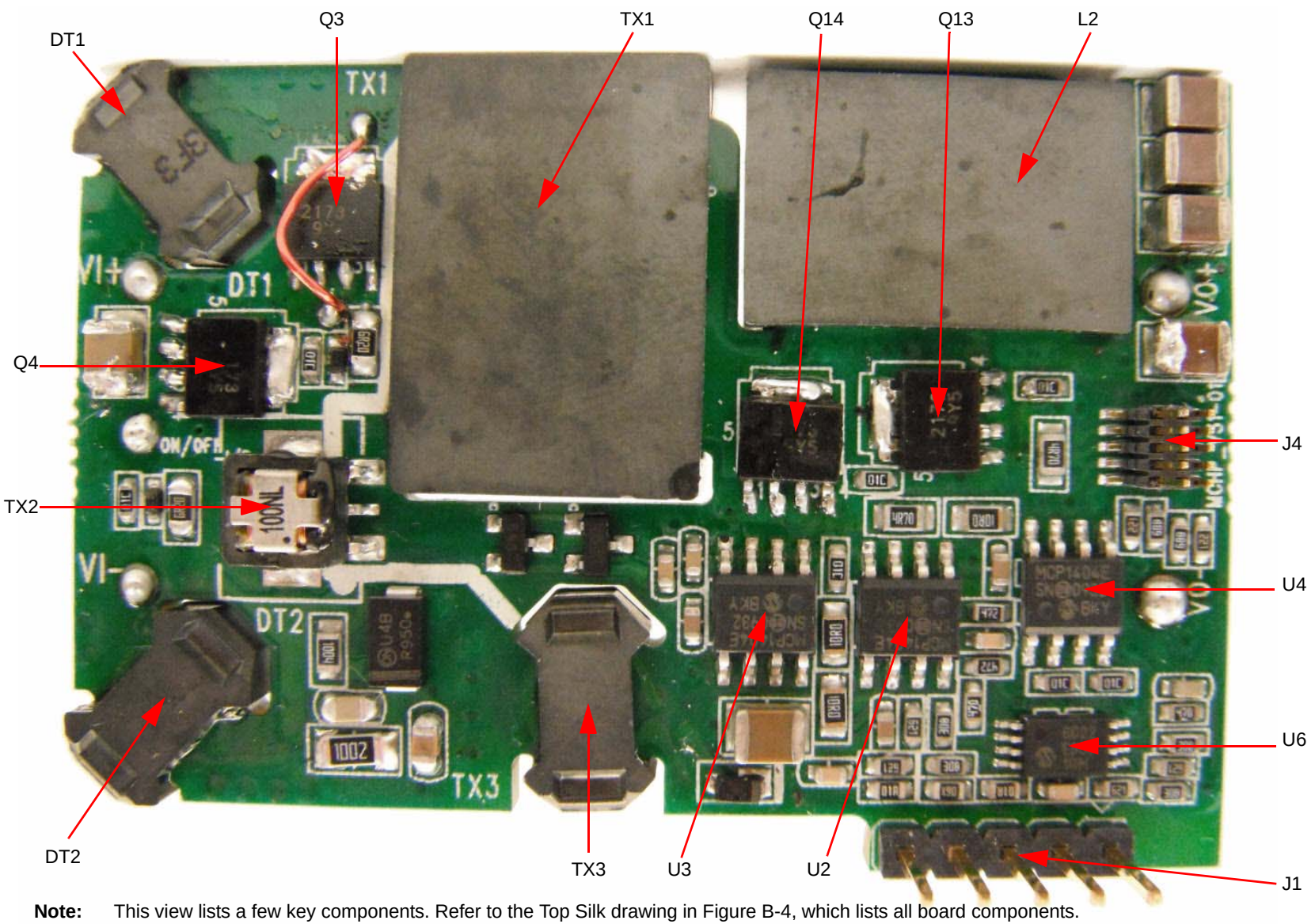


FIGURE B-3: PSFB Quarter Brick DC/DC Converter Board Layout (Top View)



Note: This view lists a few key components. Refer to the Top Silk drawing in Figure B-4, which lists all board components.

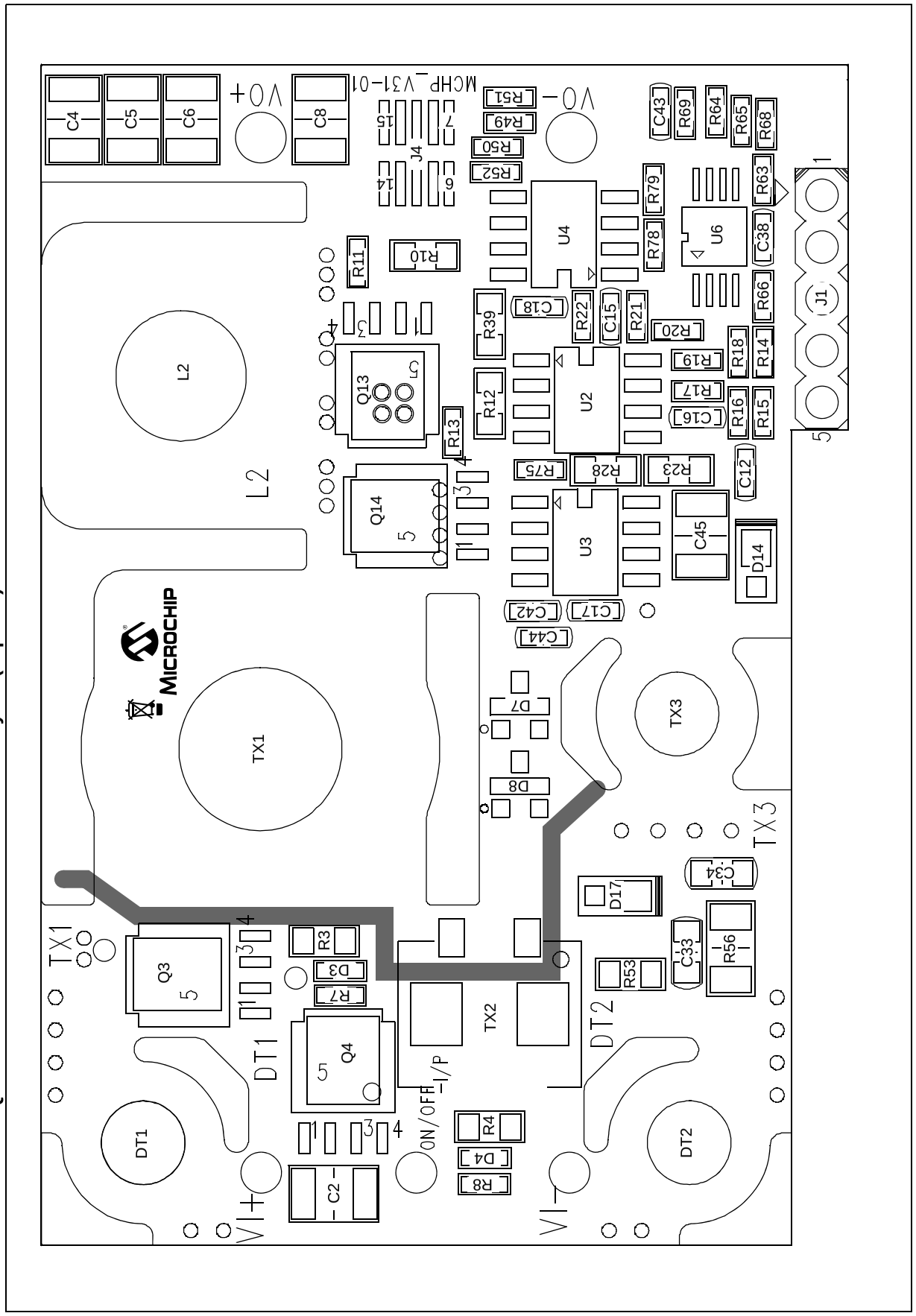


FIGURE B-4: PSFB Quarter Brick DC/DC Converter Board Layout (Top Silk)

FIGURE B-5: PSFB Quarter Brick DC/DC Converter Board Dimensions

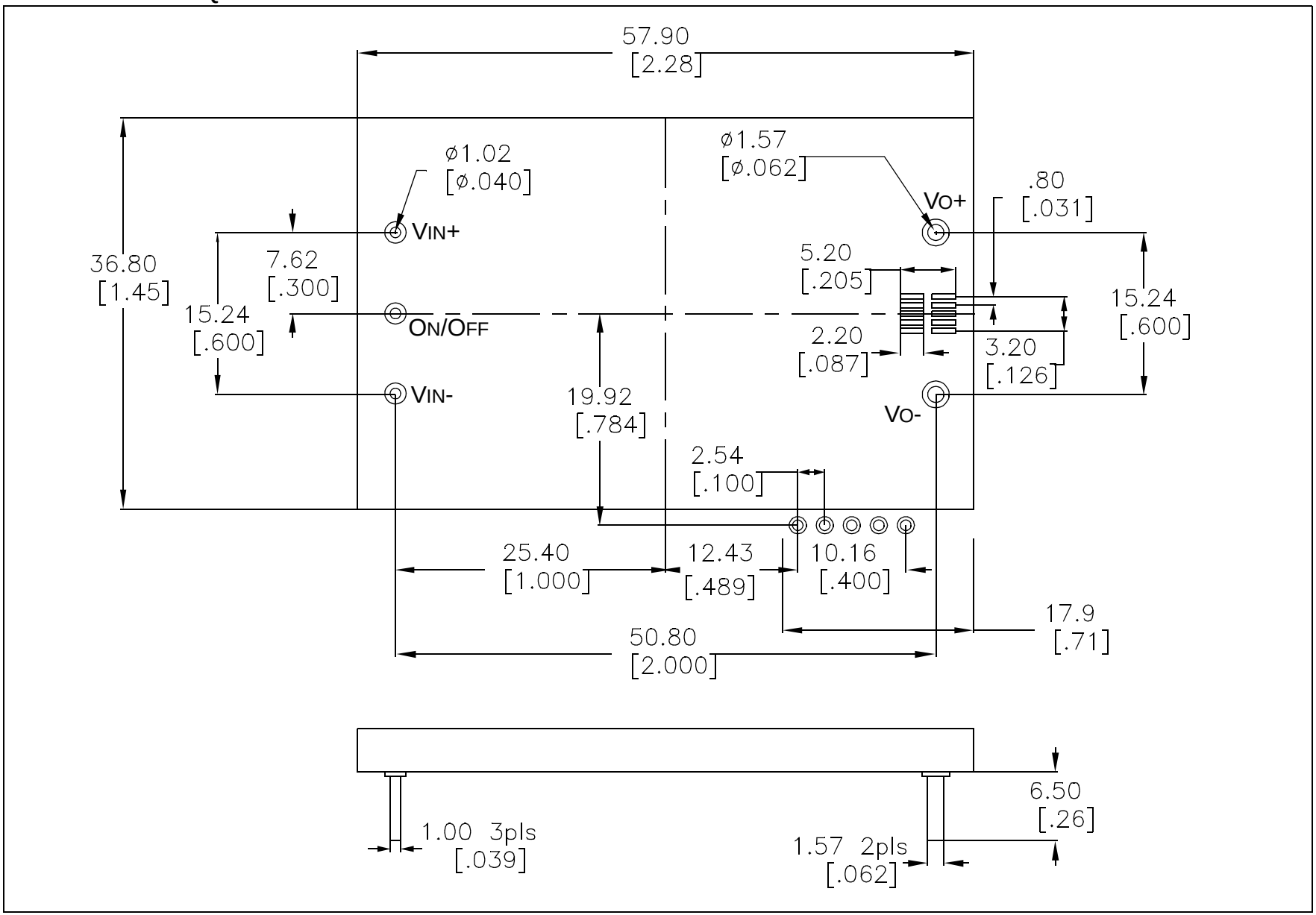


FIGURE B-6: PSFB Quarter Brick DC/DC Converter Schematic (Sheet 1 of 4)

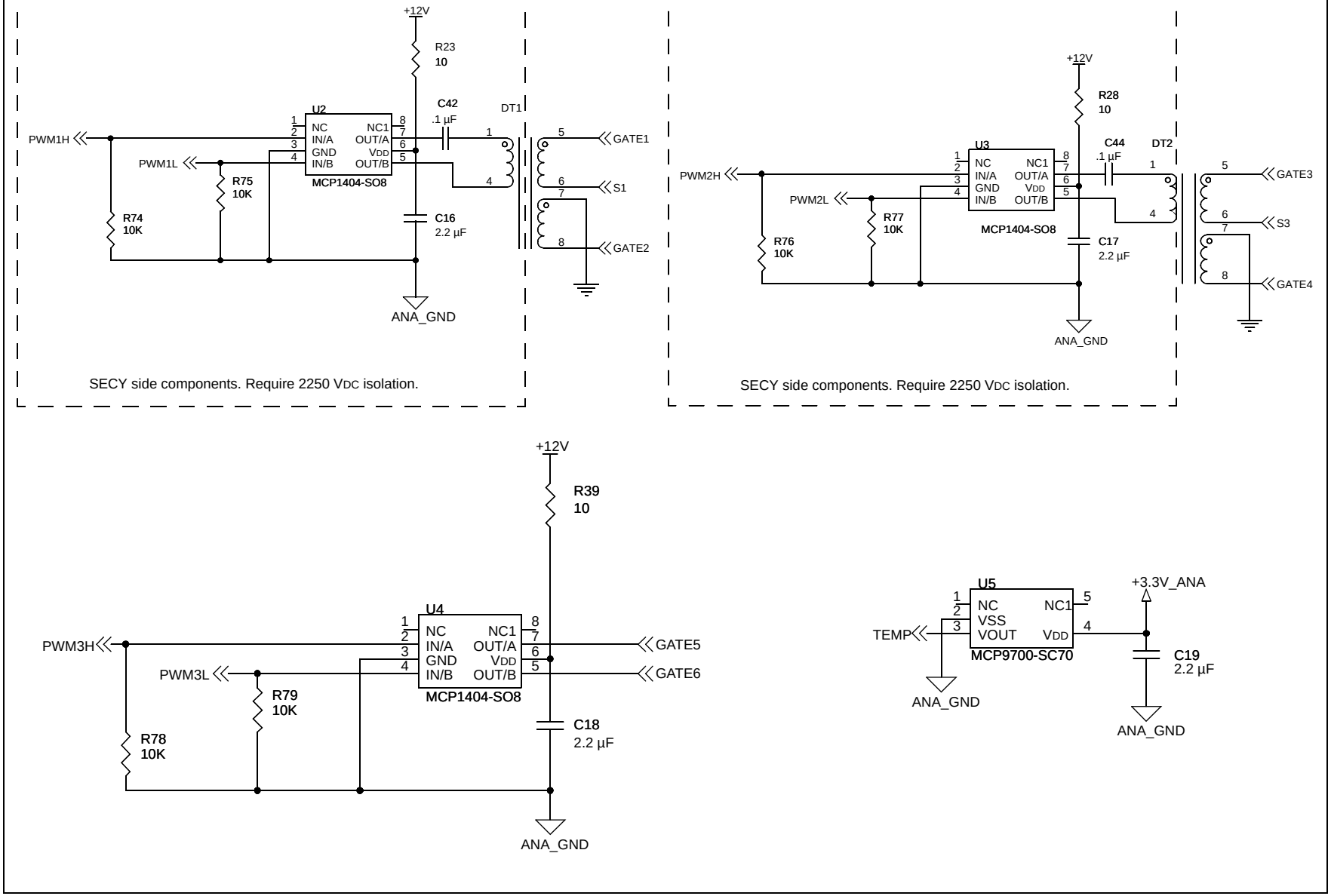


FIGURE B-7: PSFB Quarter Brick DC/DC Converter Schematic (Sheet 2 of 4)

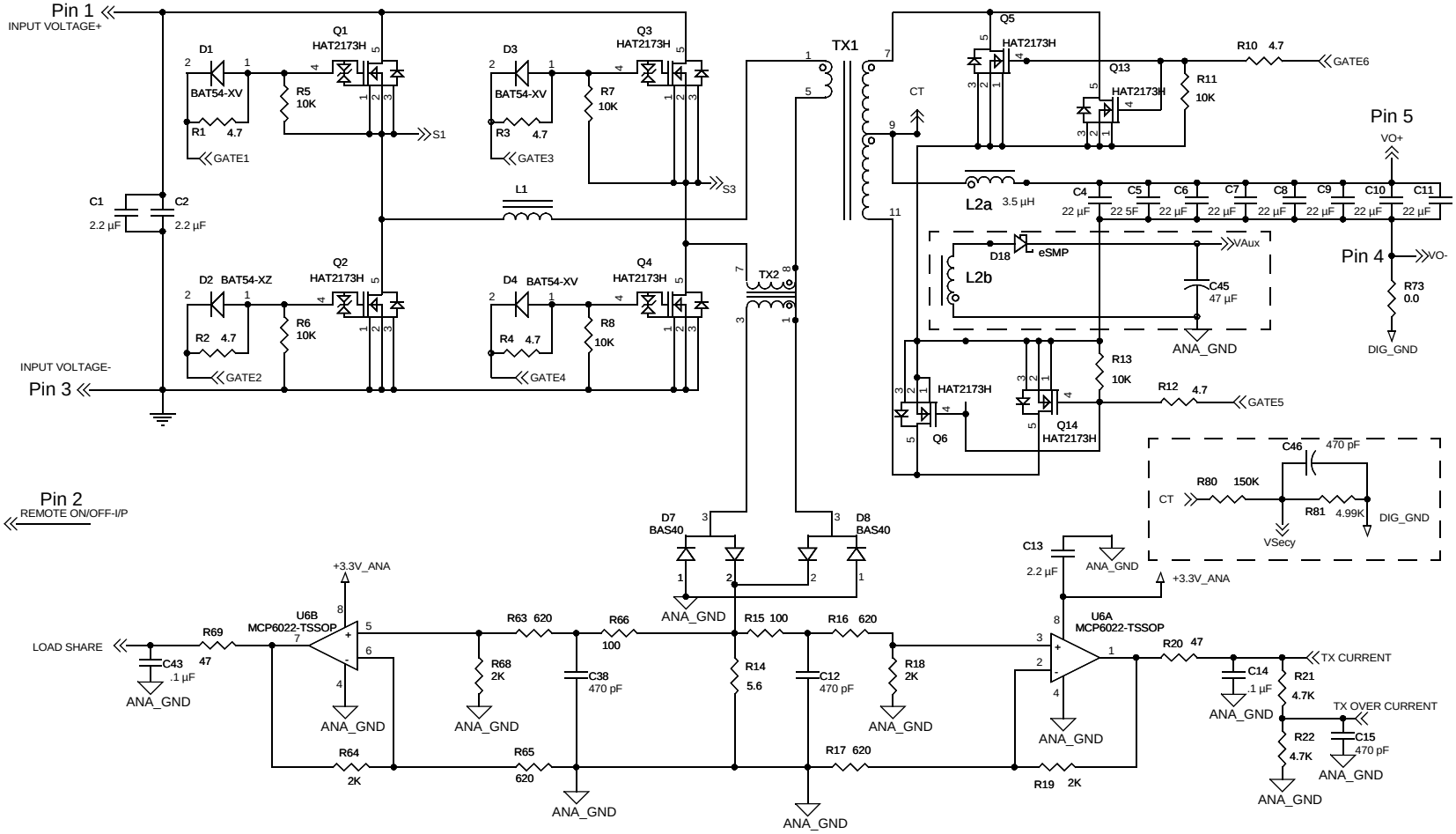


FIGURE B-8: PSFB Quarter Brick DC/DC Converter Schematic (Sheet 3 of 4)

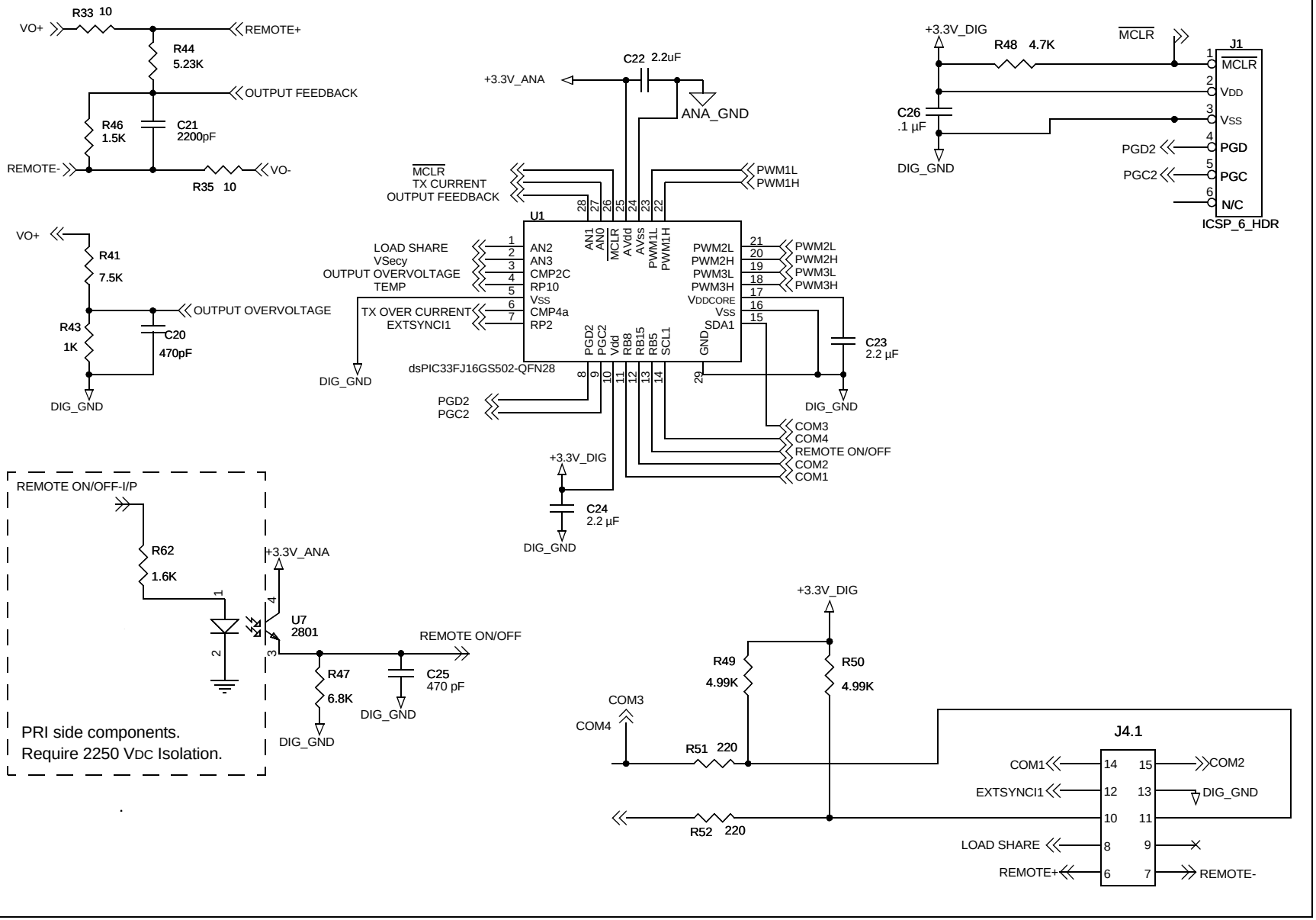


FIGURE B-9: PSFB Quarter Brick DC/DC Converter Schematic (Sheet 4 of 4)

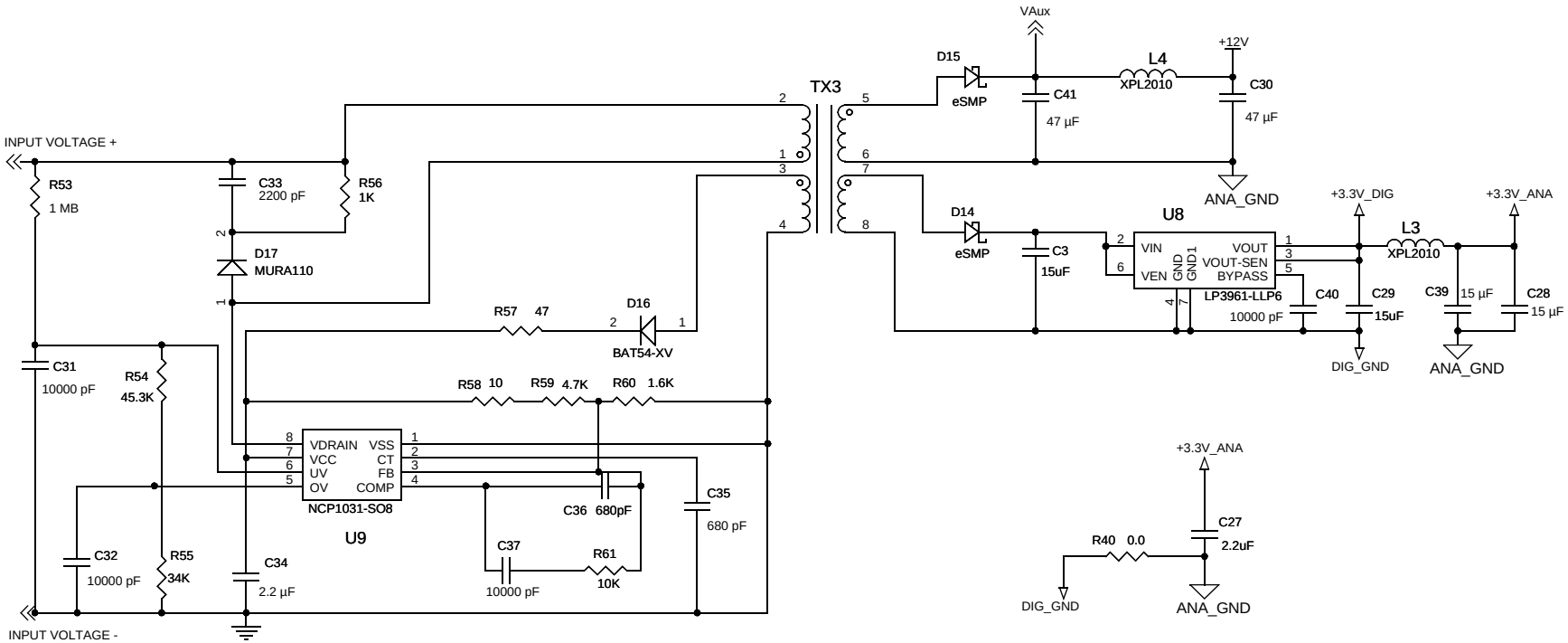
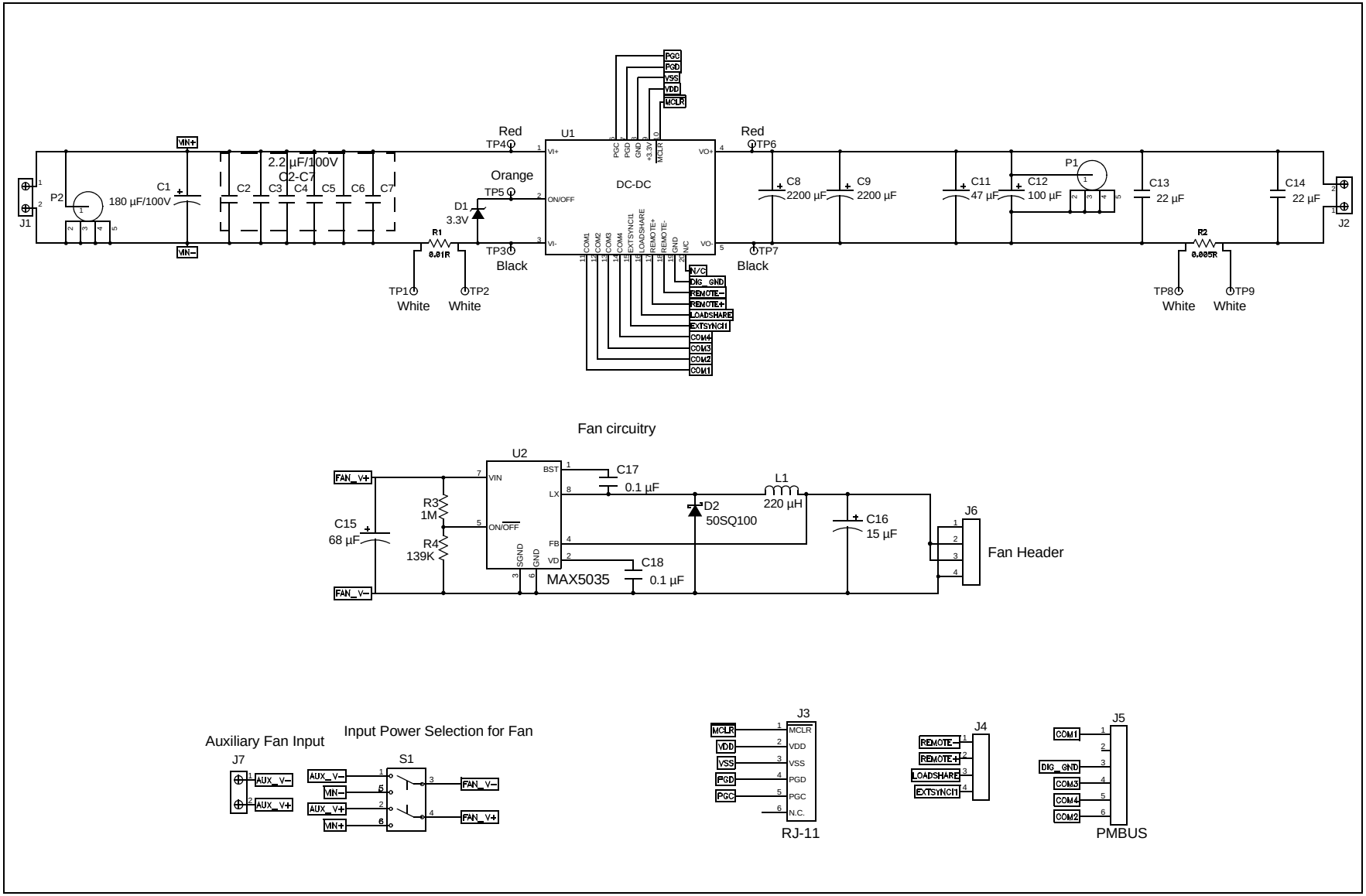


TABLE B-1: PSFB Quarter Brick DC/DC Converter Pin Out Details

Pin Number	Pin Designation	Function
1	V_{IN}+	Input Voltage Plus
2	Remote ON/OFF	Remote ON/OFF
3	V_{IN}-	Input Voltage Minus
4	V0-	Output Voltage Minus
5	V0+	Output Voltage Plus
J4-6	Remote+	Remote Sense Plus
J4-7	Remote-	Remote Sense Minus
J4-8	Load Share	Single Wire Load Share
J4-9	NC	Not Connected
J4-10	COM 4	Serial Clock Input/Output
J4-11	COM 3	Serial Data Input/Output
J4-12	EXTSYNCI 1	External Synchronization Signal
J4-13	DIG_GND	Digital Ground
J4-14	COM 1	PORTB - 8
J4-15	COM 2	PORTB - 15
J1-1	$\overline{MCLR}$	Master Clear
J1-2	+3.3V	Supply
J1-3	DIG_GND	Digital Ground
J1-4	PGD2	Data I/O Pin for Programming/Debugging
J1-5	PGC2	Clock Input Pin for Programming/Debugging

APPENDIX C: BASE BOARD SCHEMATIC AND LAYOUT

FIGURE C-1: BASE BOARD SCHEMATIC



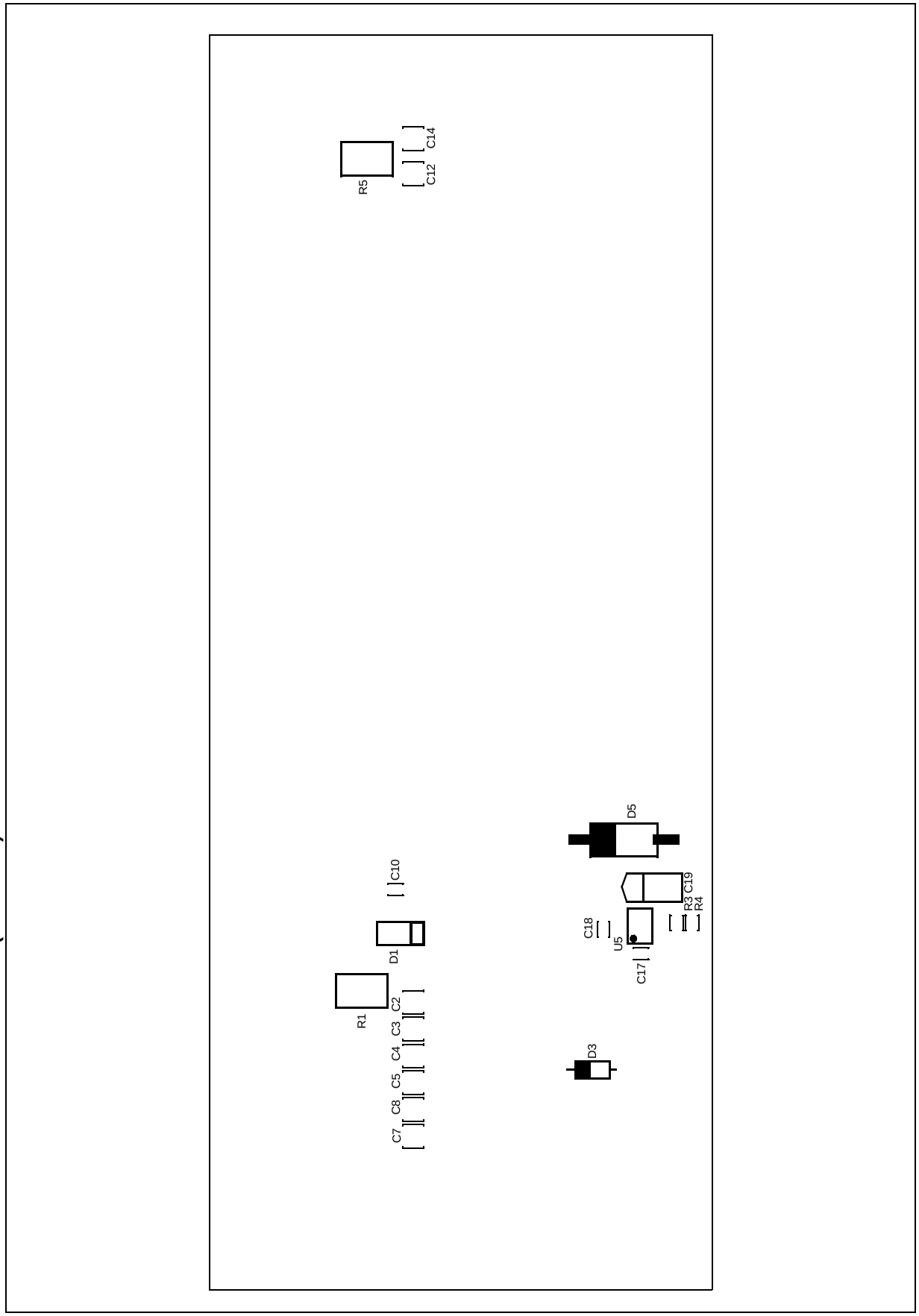
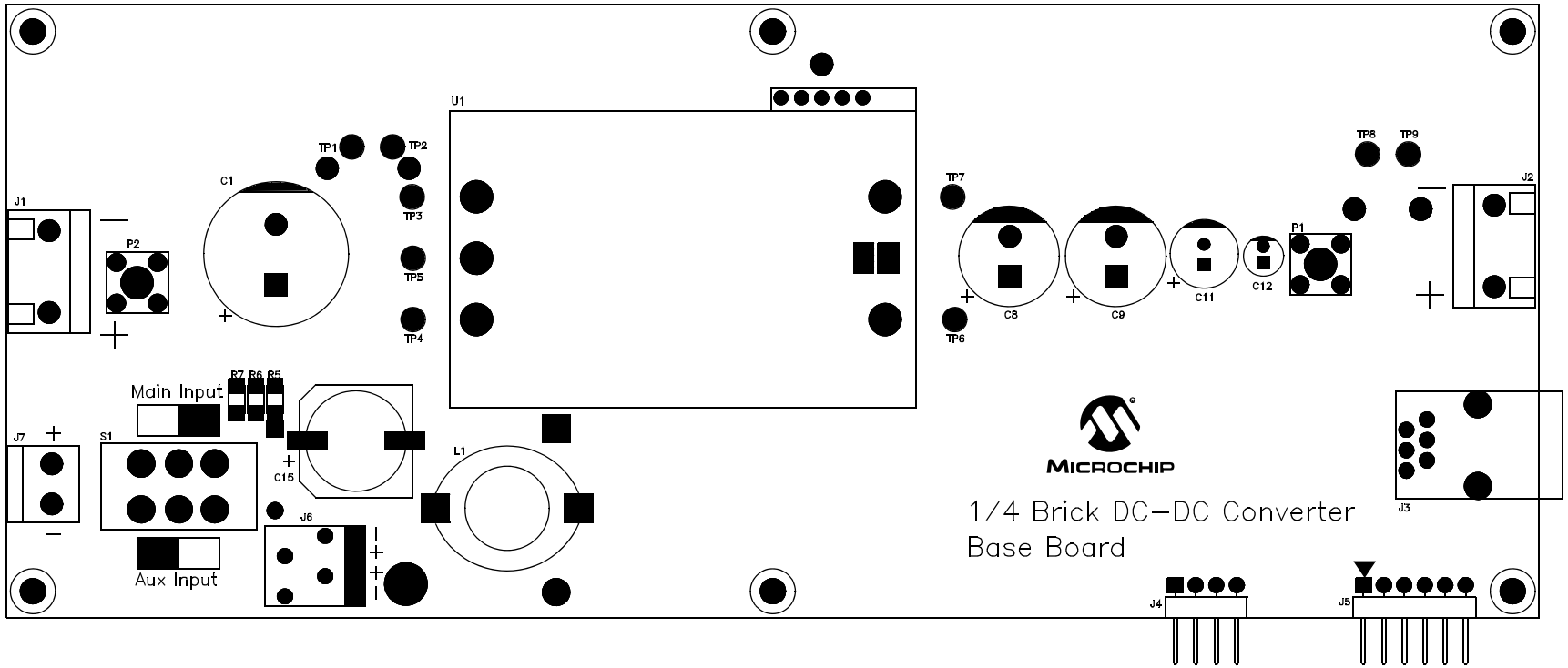


FIGURE C-2: BASE BOARD LAYOUT (TOP VIEW)

FIGURE C-3: BASE BOARD LAYOUT (BOTTOM VIEW)



C.1 Efficiency Improvement Proposals

The following proposals can be implemented to improve the efficiency of the converter.

1. Improving the rise and fall times of the MOSFETs.
2. Investigating the feasibility of using a single gate drive transformer in the Full-Bridge reference design.
3. Investigating the feasibility of using high-side and low-side drivers.
4. Using 3+3 synchronous MOSFETs in the secondary rectifications.
5. Investigating the feasibility of using fractional turns in the main transformer.

In the present design, some of the layers were made using 2 oz. copper. As an improvement, these layers could be made using 4 oz. copper.

APPENDIX D: PSFB QUARTER BRICK DC/DC REFERENCE DESIGN DEMONSTRATION

This appendix guides the user through the evaluation process to test the Quarter Brick DC/DC Converter.

The Phase-Shifted Full-Bridge Quarter Brick DC/DC Converter Reference Design is a 200W output isolated converter with 36V-76V DC input and produces 12V DC output voltage.

D.1 Tests Performed on the Quarter Brick DC/DC Converter

- Input characteristics
  - Input undervoltage/overvoltage
  - No load power
  - Input power when remote ON/OFF is active
- Output characteristics
  - Line regulation
  - Load regulation
  - Output voltage ramp-up time
  - Start-up time
  - Remote ON/ OFF start-up time
  - Remote ON/OFF shutdown fall time
  - Output overcurrent threshold
  - Output voltage ripple and noise
  - Load transient response
- Efficiency of the converter

D.2 Test Equipment Required

- DC source 30 VDC-100 VDC @ 8A (programmable DC power supply, 62012P-600-8 from Chroma or equivalent)
- DC electronic load (DC electronic load 6314/ 63103 from Chroma or equivalent)
- Digital multimeters (six and one-half digit multimeter, 34401A from Agilent or equivalent)
- Oscilloscope (mixed-signal oscilloscope, MSO7054A from Agilent or equivalent)
- Differential probe (high-voltage differential probe, P5200 from Tektronix or equivalent)

D.3 Test Setup Description

The Quarter Brick DC/DC Converter is assembled on the base board for evaluation purposes. The location of the Quarter Brick DC/DC Converter and its associated components used for testing are illustrated in Figure D-1.

FIGURE D-1: QUARTER BRICK DC/DC CONVERTER CONNECTED TO THE BASE BOARD IN THE REFERENCE DESIGN ENCLOSURE

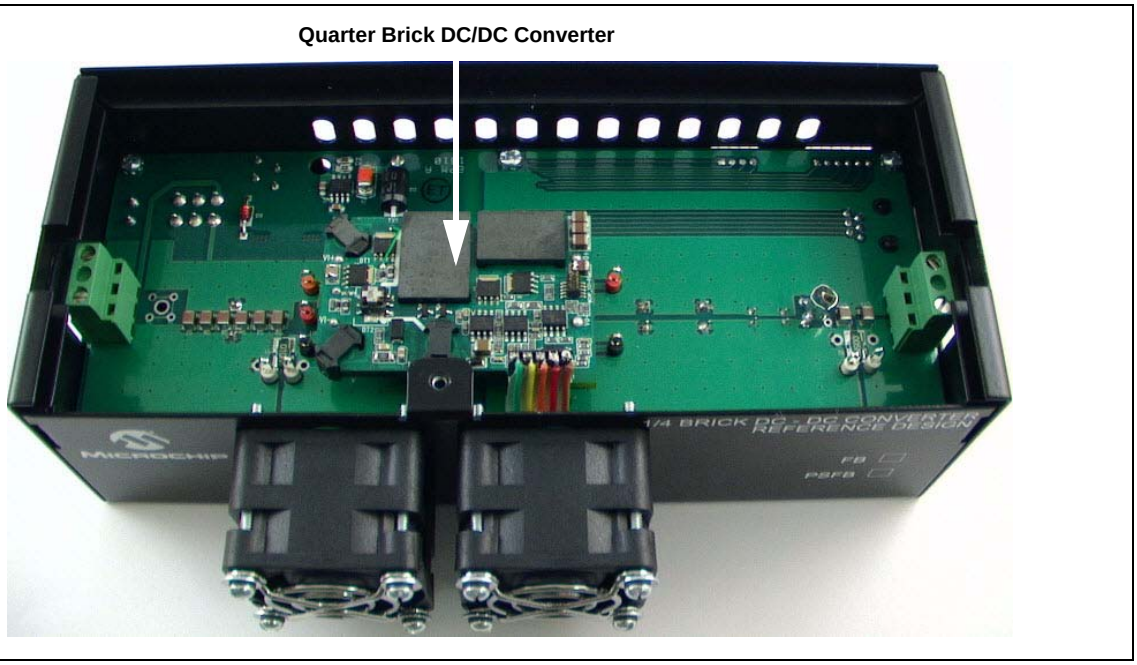


FIGURE D-2: FRONT VIEW OF THE QUARTER BRICK DC/DC CONVERTER REFERENCE DESIGN

Note: The check mark on the front of the enclosure identifies the reference design model.

FB = Full-Bridge Quarter Brick DC/DC Converter (to be discussed in a future application note)
PSFB = Phase-Shifted Full-Bridge DC/DC Converter

Use the following procedure to connect the DC load and source.

1. Connect the DC source +ve terminal and -ve terminals to the + and – input terminals (INPUT 36-76V) of the connector, as illustrated in Figure D-3.
2. Connect the DC load +ve terminal and –ve terminals to the + and – output terminals (OUTPUT 12V) of the converter, as illustrated in Figure D-4.

Note: The PROGRAM/DEBUG socket is used to program the converter with software.

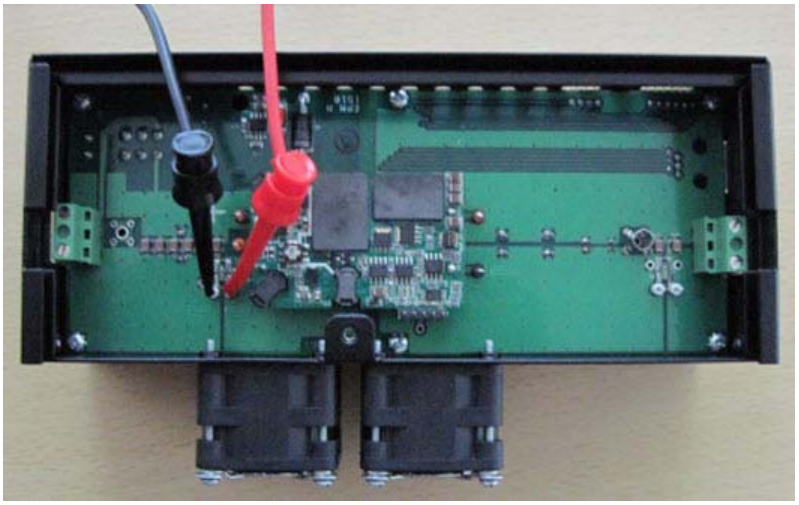
FIGURE D-3: LEFT SIDE VIEW OF THE QUARTER BRICK DC/DC CONVERTER REFERENCE DESIGN

FIGURE D-4: RIGHT SIDE VIEW OF THE QUARTER BRICK DC/DC CONVERTER REFERENCE DESIGN

Use the following procedure to prepare the reference design for testing.

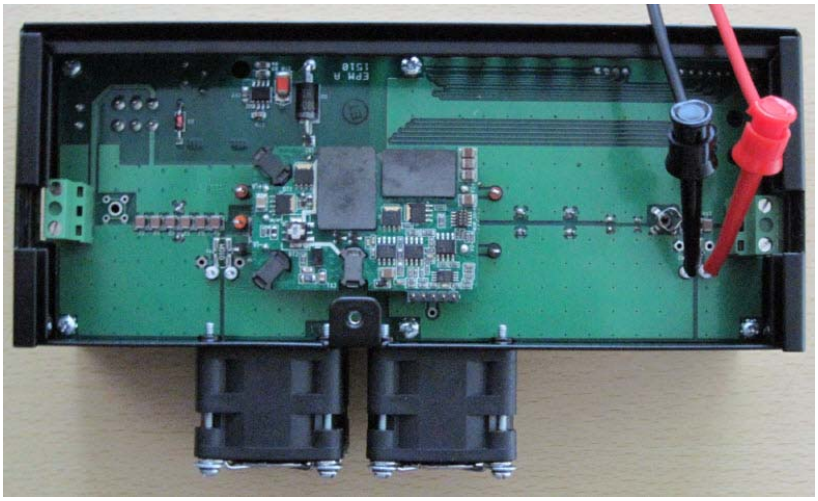
1. Connect the DMM +ve terminal and –ve terminals to the +ve and –ve terminals of the input current measurement resistor, as illustrated in Figure D-5. The current measurement resistor used to measure the input current is 10 mE. For example, if the measured voltage across the resistor is 60 mV, the input current will be 6A.

FIGURE D-5: INPUT CURRENT MEASUREMENT



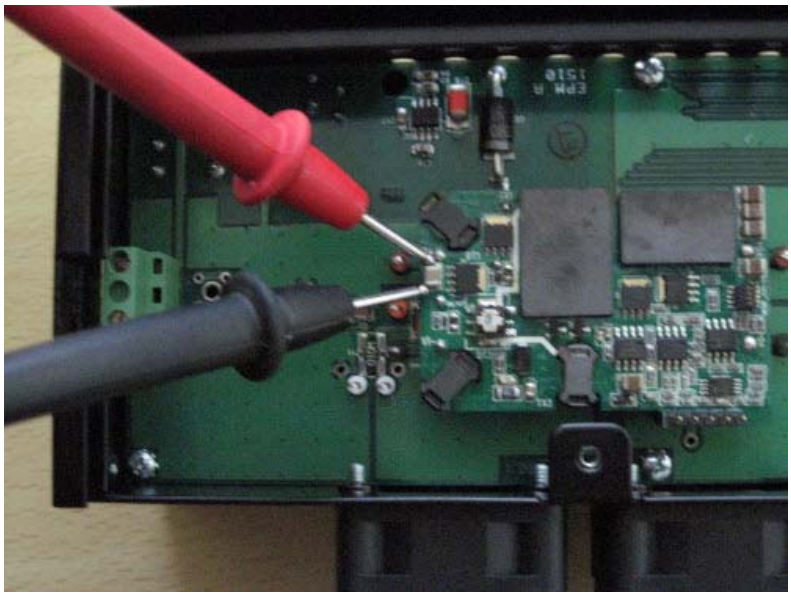
2. Connect the DMM +ve terminal and –ve terminals to the +ve and –ve terminals of the output current measurement resistor, as illustrated in Figure D-6. The current measurement resistor used to measure the output current is 5 mE. For example, if the measured voltage across the resistor is 85 mV, then the output current will be 17A.

FIGURE D-6: OUTPUT CURRENT MEASUREMENT



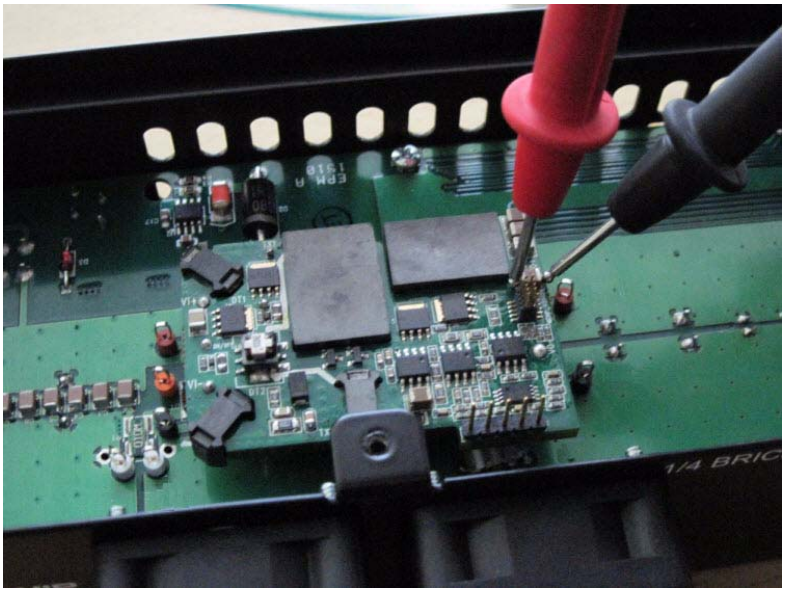
3. Connect the DMM for input voltage measurement, as illustrated in Figure D-7.

FIGURE D-7: INPUT VOLTAGE MEASUREMENT



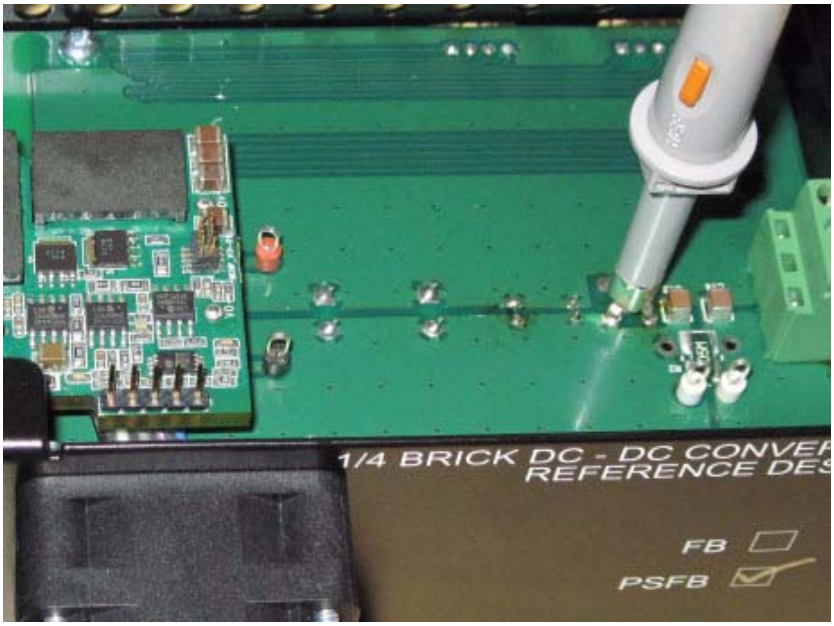
4. Connect the DMM for output voltage measurement, as illustrated in Figure D-8.

FIGURE D-8: OUTPUT VOLTAGE MEASUREMENT



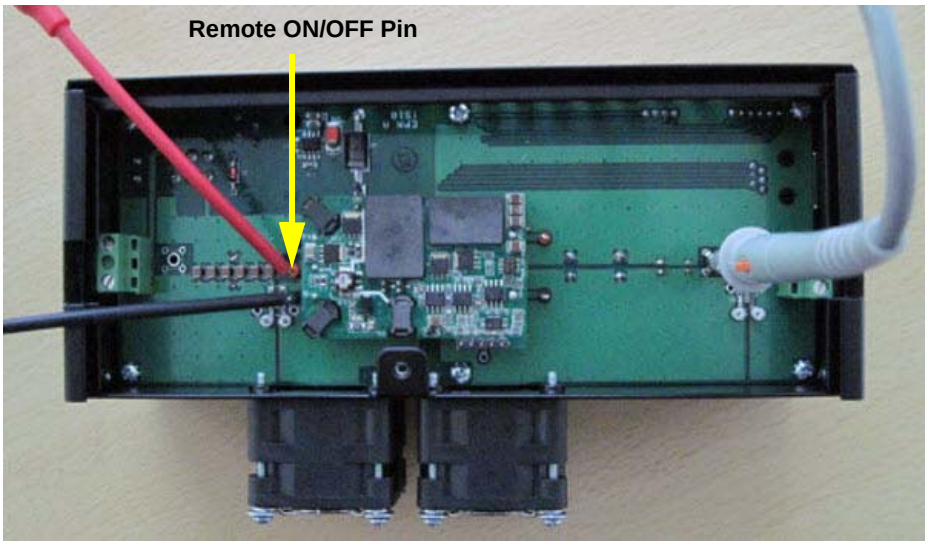
5. Connect the oscilloscope probe for output voltage (in DC coupling) and ripple and noise (In AC coupling) measurement, as illustrated in Figure D-9.

FIGURE D-9: OUTPUT VOLTAGE MEASUREMENT



6. Connect the oscilloscope probe for remote ON/OFF testing, as illustrated in Figure D-10.

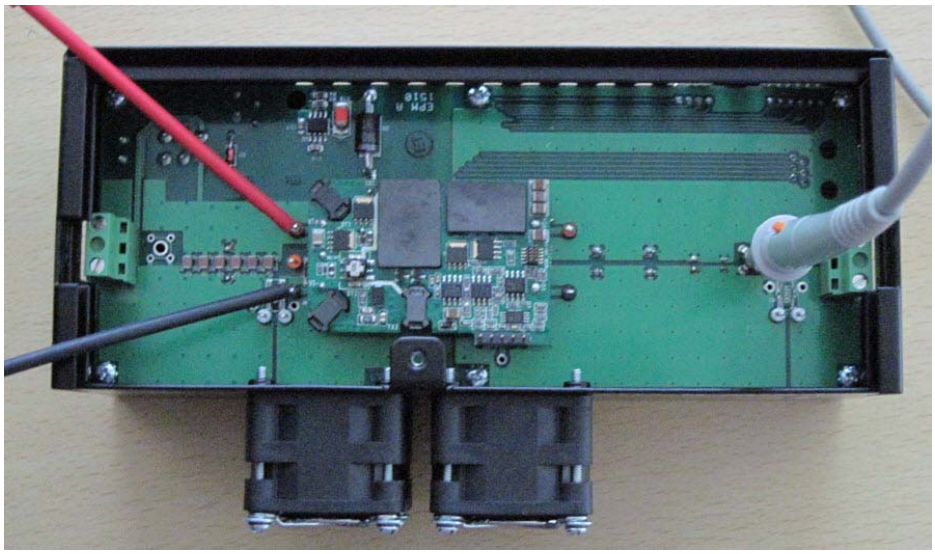
FIGURE D-10: CONNECTING THE OSCILLOSCOPE PROBE FOR REMOTE ON/OFF TESTING



Note:	Differential probe must be used to monitor the remote ON/OFF signal.

7. Connect the oscilloscope probe for start-up time, as illustrated in the Figure D-11.

FIGURE D-11: CONNECTING THE OSCILLOSCOPE PROBE FOR START-UP TIME



Note:	Differential probe must be used to monitor the input voltage.

Instructions to connect two quarter brick converters for parallel operation

1. For N+1 system operations connect COMM2-3 (load share) of converter 1 to converter2 COMM2-3(load share).
2. Connect a common DC source to the Converter1 and Converter2 input terminals as illustrated in Figure D-3.
3. Connect a Common DC electronic load to the Converter1 and Converter2 output terminal as illustrated in Figure D-4.

D.4 Forced Air Cooling

The Quarter Brick DC/DC Converter is designed to work with forced air cooling, which is provided by the fans illustrated in Figure D-2. Ensure that the fans are circulating air into the enclosure after providing the DC input supply at the + and – input terminals (INPUT 36-76V) of the connector, as illustrated in Figure D-3.

D.5 Powering Up the Quarter Brick DC/DC Converter

Before powering up the converter, ensure that polarity of the input source and DC load are connected as per the guidelines described in the section **"Test Setup Description"**.

Use the following procedure to power up the reference design.

1. Turn the DC source ON and measure the input voltage with DMM, as illustrated in Figure D-7. This voltage should be in the range of 36 VDC-76 VDC. Check to see that the fans are circulating air into the enclosure.
2. Ensure that the connected DC load is in the range of 0A-17A. The output load current measurement resistor provides a value in the range of 0 mV-85 mV when measuring with DMM, as illustrated in Figure D-6.
3. Ensure that the output voltage read by DMM (see Figure D-8) is in the range of 11.88 VDC to 12.12 VDC.

D.6 Test Procedure

The following two sections provide detailed procedures for each test.

D.6.1 INPUT CHARACTERISTICS

1. Input undervoltage/overvoltage.

   The Quarter Brick DC/DC Converter is rated to operate with regulation between the input voltage ranges 36 VDC-76 VDC. The converter features input undervoltage and overvoltage protection. This feature will not allow the converter to start-up unless the input voltage exceeds the turn-on voltage threshold and shuts down the converter when the input voltage exceeds the overvoltage threshold.

   a) Set the DC load at 8.5A and increment the input voltage from 33 VDC (read the input voltage with DMM illustrated in Figure D-7) to the voltage where output voltage is in the regulation range of 11.88 VDC to 12.12 VDC. Read the output voltage with DMM illustrated in Figure D-8.
   b) Start decrementing the input voltage and observe at what input voltage the converter shuts OFF. This input voltage point will be the input undervoltage threshold.
   c) Start incrementing the voltage from 76 VDC input and observe at what input voltage converter shuts OFF. This input voltage point will be the input overvoltage threshold.

      Typically, the unit may enter into the regulation range at around 35 VDC, undervoltage lockout at approximately 33.5 VDC, and overvoltage lockout at approximately 81 VDC.

2. No load power.
   a) Set the input voltage at 53 VDC and disconnect or turn OFF the load from the converter and record the input power.

      This value will be the product of input voltage and input current measured using the DMM illustrated in Figure D-5 and Figure D-7.

3. Input power when remote ON/OFF is active.

   Remote ON/OFF will be used to turn OFF the converter by applying a 3.3 VDC signal on the pin illustrated in Figure D-10. A high signal (3.3 VDC) will turn OFF the converter and there is no output. When a high signal is sensed by the dsPIC DSC, all of the PWM generators are shutdown. When the dsPIC DSC detects a low remote ON/OFF signal, the converter will be turned ON.

   a) Turn ON the converter with 53 VDC input at 8.5A output load. Connect an oscilloscope voltage probe to measure the output voltage and a differential voltage probe to measure the external 3.3 VDC supply, as illustrated in Figure D-10.
   b) Turn ON the external 3.3 VDC supply and the system will shut down (there will be no voltage at the output of the converter). Record the input voltage and input current to calculate the input power.

D.6.2 OUTPUT CHARACTERISTICS

1. Line regulation.

   Change the input DC voltage from 36 VDC to 76 VDC to the converter and record the output voltage. The output voltage deviation should be in the range of 11.88 VDC to 12.12 VDC.

2. Load regulation.

   Change the output load from 0A to 17A at various input voltages in the range of 36 VDC to 76 VDC and record the output voltage variations. The output voltage deviation should be in the range of 11.88 VDC to 12.12 VDC.

3. Output voltage ramp-up time.

   Turn ON the converter with the specified input voltage in the range of 36 VDC to 76 VDC and observe the DC output voltage raise time. Ramp-up time is the time taken to reach output voltage from 10% to 90% of the rated output voltage. Ramp-up time can be measured by connecting the oscilloscope voltage probe, as illustrated in Figure D-9.

4. Start-up time.

   This is the time when the input voltage applied to the converter (in the range of 36 VDC-76 VDC) when the output voltage reaches 90% of the rated 12V output voltage. Connect the voltage differential probe at the input voltage terminals and the voltage probe at the output to the oscilloscope, as illustrated in Figure D-11.

5. Remote ON/OFF start-up time.

   Remote ON/OFF will be used to disable/enable the converter by applying or removing a 3.3 VDC signal on the Remote ON/OFF pin, as illustrated in Figure D-10. Applying 3.3 VDC on the remote ON/OFF pin turns the converter OFF. Remote ON/OFF start-up time is the time duration from when the remote ON/OFF is disabled, to when the output voltage rises to 90% of the rated output voltage.

6. Remote ON/OFF shut down fall time.

   Removing the 3.3 VDC signal on the remote ON/OFF pin, turns the converter ON. The remote ON/OFF fall time is the time duration from when the remote ON/OFF signal is enabled, to when the output voltage falls to 10% of the rated output voltage.

7. Output overcurrent threshold.

   The output overcurrent limit will protect the unit from excessive loading than the rated load current. Increment the output load beyond the rated 17A, the converter enters into Hiccup mode for a few milliseconds. If overcurrent persists, the converter enters into Latch mode.

   Set the input voltage at various points in the specified range 36 VDC to 76 VDC and increment the load at the output insteps. To monitor the output voltage, connect the voltage probe, as illustrated in Figure D-9.

8. Load transient response.

   Observe the variation on the DC output voltage while step changing the output load from 25% to the 75% of the rated output load 17A. The parameters to be measured are peak-to-peak output voltage variation and load transient recovery time. Configure the oscilloscope in AC couple mode and connect the oscilloscope output voltage probe as illustrated in Figure D-9 to measure the peak-to-peak output voltage variation and load transient recovery time.

9. Output voltage ripple and noise.

   Measure the AC component on the output voltage of the converter by connecting the oscilloscope output voltage probe, as illustrated in Figure D-9. Read the output voltage by configuring the oscilloscope in the AC couple mode. The output ripple is measured in terms of peak-to-peak voltage.

D.7 Efficiency of the Quarter Brick DC/DC Converter

Efficiency is the ratio of output power to the input power:

*Efficiency (%) = Output Power / Input Power * 100*

*= [(Output voltage * Output current) / (Input Voltage * Input Current)] * 100*

Use the following procedure to measure the efficiency of the converter.

1. Connect the DMM +ve terminal and –ve terminals to the +ve and –ve of the input current measurement resistor, as illustrated in Figure D-5.
2. Connect the DMM +ve terminal and –ve terminals to the +ve and –ve of the output current measurement resistor, as illustrated in Figure D-6.
3. Connect the DMM for input voltage measurement, as illustrated in Figure D-7.
4. Connect the DMM for output voltage measurement, as illustrated in Figure D-8.

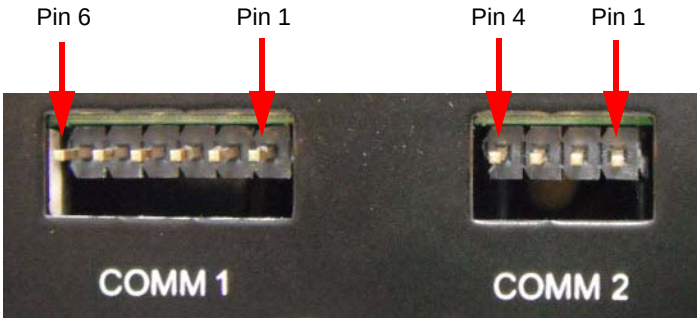
D.8 COMM 1 and COMM 2 Connectivity

The COMM 1 and COMM 2 signal connectors, pin termination, and functionality are described in Table D-1. The pin sequence is illustrated in Figure D-12.

TABLE D-1: PIN, PERIPHERAL AND FUNCTIONALITY TABLE

Pin	Peripheral	Functionality
COMM 1 - 1	RB8	Remappable I/O
COMM 1 - 2	—	No connect.
COMM 1 - 3	VSS	DIG_GND
COMM 1 - 4	SDA1	Synchronous serial data input/output for I2C1.
COMM 1 - 5	SCL1	Synchronous serial clock input/output for I2C1.
COMM 1 - 6	RB15	Remappable I/O.
COMM 2 - 1	—	Remote Sense -ve.
COMM 2 - 2	—	Remote Sense +ve.
COMM 2 - 3	AN2	Load share.
COMM 2 - 4	RP2/SYNCI1	External synchronization signal to PWM master time base.

FIGURE D-12: COMM 1 AND COMM 2 SIGNAL CONNECTORS



Note 1: For N+1 system operations connect COMM2-3 (load share) of Converter 1 to Converter2 COMM2-3(load share).

2: Connect a common DC source to the Converter1 and Converter2 input terminals as illustrated in Figure D-3.

3: Connect a Common DC electronic load to the Converter1 and Converter2 output terminal as illustrated in Figure D-4.

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