AN1327

Avoiding MOSFET Driver Overstress

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INTRODUCTION

This application note describes how to avoid MOSFET driver overstress. MOSFET drivers are used in many applications to drive the high input capacitance of a power MOSFET device. MOSFET drivers are very reliable when used within their operating specifications. Care must be taken, however, to control supply line transients and power dissipation, and prevent latch-up.

AVOIDING SUPPLY LINE TRANSIENTS

During switching transitions, parasitic inductances can create transients on the supply line, and those can create electrical overstress. Proper bypass capacitor selection and PCB layout must be performed to protect the driver from voltage transients during switching transitions. Proper PCB layout is necessary to minimize parasitic inductance in the supply path, and the ground path.

Microchip provides MOSFET driver models for the following devices:

- TC1410
- TC1411
- TC1412
- TC4404/05
- TC4420/29
- TC4421/22
- TC4423/24/25
- TC4423A/24A/25A
- TC4426/27/28
- TC4426A/27A/28A
- TC4431/32
- TC4451/52
- TC4467/68/69

These driver models can be downloaded from the Microchip web site, www.microchip.com.

Simulating Supply Line Transients

The Mindi™ Circuit Designer and Simulator can be used to simulate supply line transients. (Mindi software can be downloaded from the Microchip web site.) The following simulation includes the parasitic inductances that are associated with package inductance, bypass capacitor parasitic series inductance, and printed wiring board inductance.

The PCB Trace Inductance diagram in Figure 1 shows the TC4423A device (3A peak output current) in a circuit with following items:

- L4 – parasitic inductance in series with ground pin
- L5 – parasitic inductance in series with V_{DD} pin
- L1, L2 – parasitic inductance in series with the bypass capacitor
- Capacitor C2 (1 nF) is used to represent the MOSFET
- L3 – the inductance from the TC4423A device to the power source

Note that the inductance between the driver output and C2 (MOSFET) is not included in this circuit simulation, but should be included in common practice. Additionally, the driver should be located as close to the output MOSFET as possible.

GETTING STARTED

Before simulation can begin, a symbol for the MOSFET driver must be created, and a MOSFET driver model netlist must be assigned to that symbol. Pressing the F11 key in Mindi opens a window where the model netlist can be copied, and the symbol can be assigned to that model netlist.

For example, assume that the following characteristics are applied to the items in the simulated circuit in Figure 1:

- L4 and L5 – SOIC package leads PCB trace = 10 nH
- L1 and L2 – series inductance of a 0805 ceramic capacitor PCB trace = 10 nH
- L3 – PCB trace inductance from the V_{DD} pin to the power source that feeds the MOSFET driver

Note that the parasitic series resistance and input/output PCB inductance have been omitted from this simulation, but they are available for inclusion.

The results of the simulation, as presented in Figure 2, illustrate the voltage overshoot effect caused by the parasitic inductances.

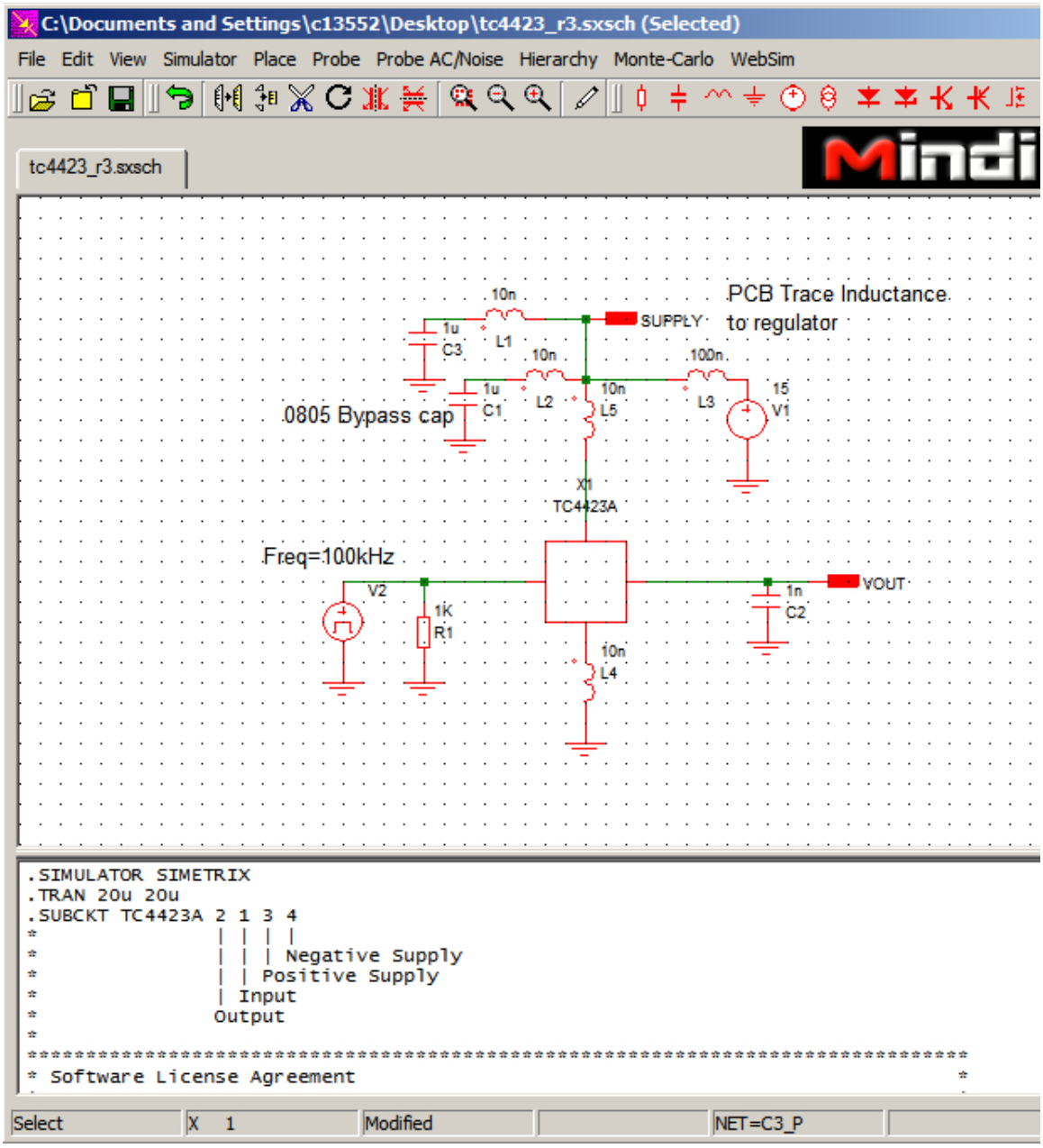

FIGURE 1: *Schematic – Parasitic Inductances.*

Figure 2 shows the results of the simulation. The supply line (SUPPLY) overshoot and V_{OUT} (VOUT) overshoot are shown. The overshoot is a result of parasitic inductance. Care must be taken so that the overshoot does not exceed the maximum operating voltage of the device.

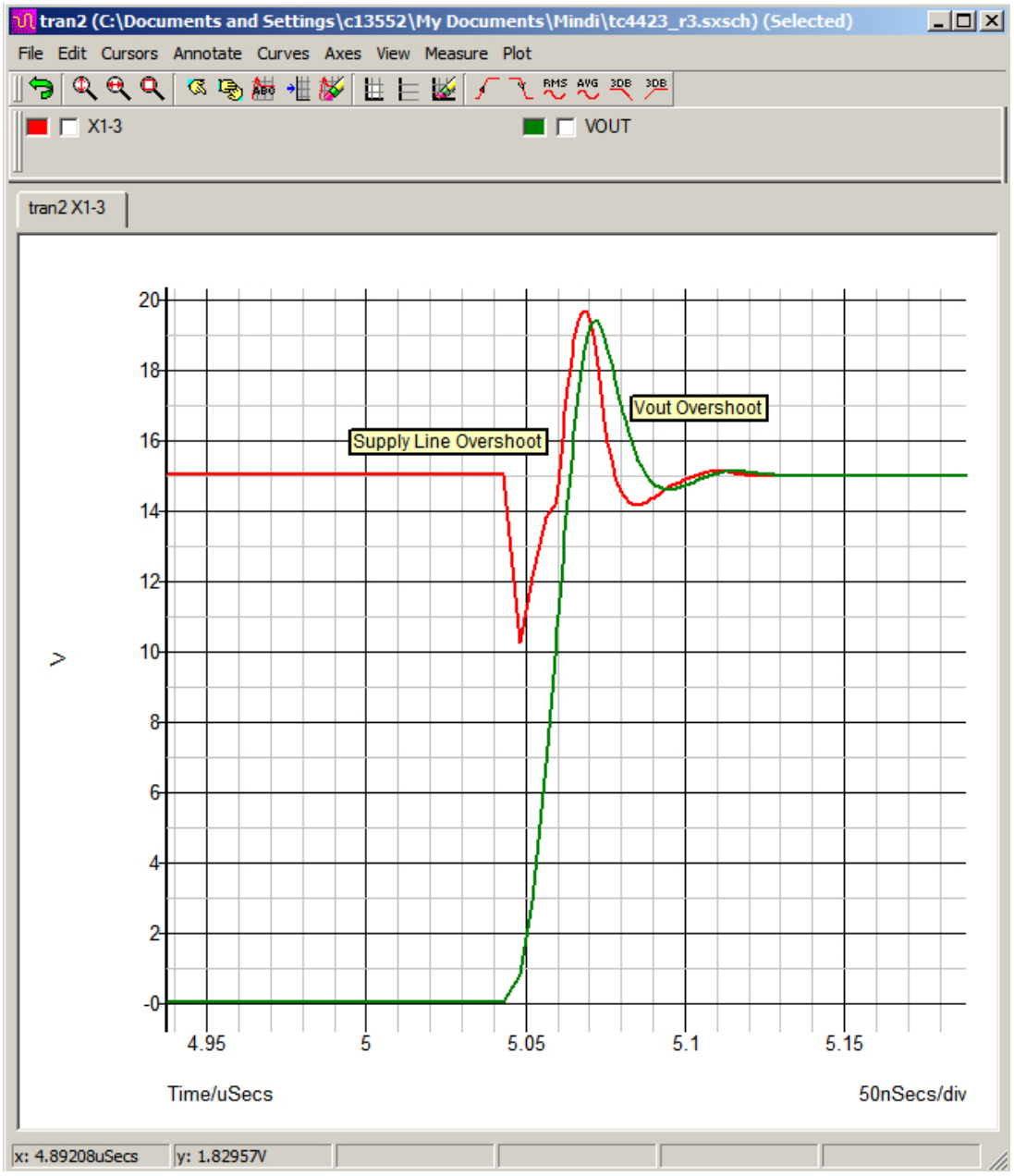

FIGURE 2: *Supply Line and V_{OUT} Overshoot.*

To minimize parasitic inductance in the supply path and ground path, a proper bypass capacitor must be selected and an associated PCB layout must be completed to reduce voltage transients during switching transitions. These steps prevent ringing on the output of the driver and supply lines. Accordingly, proper PCB line-widths must be chosen to handle the required peak current. Low-parasitic and low-ESR capacitors should be used directly at the driver, from the power supply to the ground, to minimize voltage transients to safe levels during switching.

Components in the circuit should be placed as close as possible to the driver to reduce the amount of lead inductance. V_{DD} is the bias supply input for the MOSFET driver, and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local ceramic capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents provided to the load.

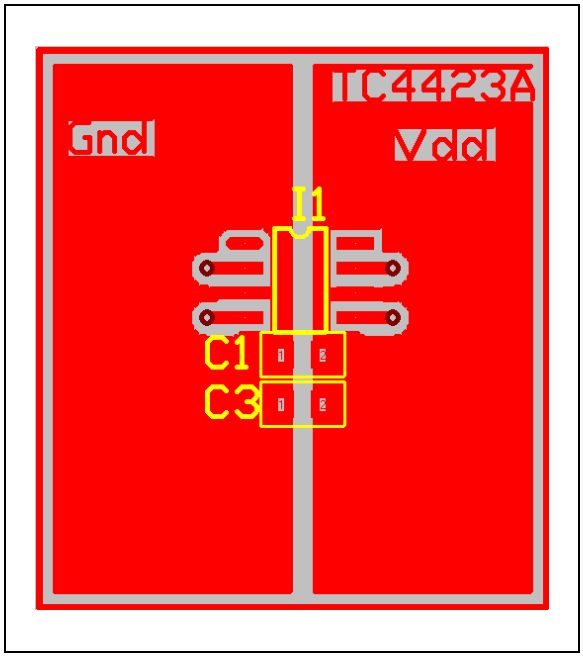

FIGURE 3: *Printed Wiring Board Layout (Top View) – Low Parasitic Inductance.*

AVOIDING EXCESSIVE POWER DISSIPATION

Calculating the power dissipation in the drivers for a desired application is critical to ensuring safe operation. Exceeding the maximum allowable power dissipation level will push the device beyond the maximum allowable operating junction temperature of +125°C.

The total power dissipation in a MOSFET driver is comprised of three separate power dissipations. These power dissipations are due to the following activities:

- charging and discharging of the total gate capacitance of the MOSFET
- power dissipation quiescent current draw of the MOSFET driver when the output is high and low
- internal shoot-through current of the MOSFET driver

CALCULATING CHARGING AND DISCHARGING POWER DISSIPATION

The charging and discharging power dissipation is calculated using the gate charge. The gate charge for a particular V_{GS} and V_{DS} is usually available from the appropriate Power MOSFET Driver data sheet. These data sheets[1] are available on the Microchip web site (www.microchip.com).

The charging and discharging power dissipation of the gate capacitance is calculated by Equation 1.

EQUATION 1:

$$P_C = C_G \times V_{DD}^2 \times F_{SW}$$

(or with gate charge capacitance, $P_C = Q_G \times V_{DD} \times F_{SW}$)

Where:

- P_C = Power dissipation due to charging and discharging the load
- C_G = Total gate capacitance
- Q_G = Total gate charge
- V_{DD} = MOSFET driver supply voltage
- F_{SW} = switching frequency

If the following values apply:

Q_G = 100 nC
V_{DD} = 15V
F_{SW} = 100 kHz

then:

$P_C = (100\ nC) \times (15V) \times (100\ kHz) = 150\ mW$

CALCULATING QUIESCENT CURRENT DRAW POWER DISSIPATION

The quiescent current draw power dissipation is calculated through use of Equation 2.

EQUATION 2:

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

- P_Q = Power dissipated due to the quiescent current draw
- I_{QH} = Quiescent current draw with the input in high state
- I_{QL} = Quiescent current draw with the input in low state
- D = Duty Cycle
- V_{DD} = MOSFET driver supply voltage

If the following values apply:

- I_{QH} = .5 mA
- I_{QL} = 50 µA
- D = 50%
- V_{DD} = 15V

then:

$P_Q = (0.5\ mA \times .5 + 50\ \mu A \times (1 - .5)) \times 15V = 4.125\ mW$

CALCULATING SHOOT-THROUGH CURRENT POWER DISSIPATION

The shoot-through current power dissipation is calculated from the crossover energy. The crossover energy is usually available in the appropriate data sheet.

The shoot-through current power dissipation is calculated through use of Equation 3.

EQUATION 3:

$$P_S = CC \times F_{SW} \times V_{DD}$$

Where:

- P_S = Power dissipation due to the shoot-through current
- CC = Crossover energy constant
- F_{SW} = Switching frequency
- V_{DD} = MOSFET driver supply voltage

If the following values apply:

- V_{DD} = 15V
- F_{SW} = 100 kHz
- CC = 47 nA/sec

then:

$P_S = (47\ nA \times sec) \times (100\ kHz) \times (15V) = 70.5\ mW$

The total power dissipated is:

$P_T = P_C + P_Q + P_S = 150\ mW + 4.125\ mW + 70.5\ mW = 224.63\ mW$

This value is less than the maximum power dissipation of the device.

CALCULATING INTERNAL JUNCTION TEMPERATURE

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance, from junction to ambient, for the application.

A value for thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from JESD51-7[2], the EIA/JEDEC Standard for measuring thermal resistance of small surface mount packages. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary, depending on many factors, such as the amount of copper traces on the board and thickness of the layers.

EQUATION 4:

$$T_{J(RISE)} = P_{TOTAL} \times R\theta_{JA}$$

$$T_{JRISE} = 224.63\ mW \times 155.0°C/Watt$$

$$T_{JRISE} = 34.82°C$$

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated using Equation 5.

EQUATION 5:

$$T_J = T_{JRISE} + T_{A(MAX)}$$

$$T_J = 74.72°C$$

$$T_A = 40°C$$

Maximum package power dissipation at +40°C ambient temperature is derived from Equation 6.

EQUATION 6:

SOIC (155°C/Watt = $R\theta_{JA}$)

$$P_{D(MAX)} = (T_{A(MAX)} - T_A)/R\theta_{JA}$$

$$P_{D(MAX)} = (125°C - 40°C)/155°C/W$$

$$P_{D(MAX)} = 548\ mW$$

AVOIDING LATCH-UP

Latch-up occurs in CMOS technologies due to parasitic transistors that form a silicon controlled rectifier (SCR). Once triggered, the parasitic SCR turns on and shorts V_{DD} to ground, usually destroying the CMOS device. Microchip application note AN763 – *"Latch-Up Protection For MOSFET Drivers"*[3], describes in detail the latch-up effect and how to prevent it.

CONCLUSIONS

Avoid supply voltages exceeding the absolute maximum ratings. Ratings of the maximum voltage that can be applied safely to a particular device are supplied in the corresponding data sheet. Anything in excess of that voltage may result in electrical overstress of an internal junction, and damage to the device. In addition, operation of the device under conditions that are close to the maximum ratings may degrade long-term reliability.

It is important to note that these ratings apply at all times, including those intervals when the device is being powered on and off. The triggering mode could result from transients on supply lines. Care should be taken to ensure that the maximum ratings are not exceeded.

Also avoid input/output pin voltage that exceeds either supply line by more than a diode drop. This could occur as a result of transients on input/output line. Care should be taken to ensure that the maximum ratings are not exceeded.

Avoid improper power-supply sequencing. Latch-up can occur from improper power-supply sequencing in devices that have multiple power supplies. It is possible for the maximum ratings to be exceeded and the device to enter a latch-up state, in some cases, when the digital supply is applied prior to other supplies. For this reason, care should be taken to ensure the maximum ratings are not exceeded.

Microchip application note AN763 recommends the following course of action, summarized below, to prevent latch-up:

- properly decouple IC
- clamp outputs with diodes when driving inductive loads
- clamp inputs with diodes if input signal exceeds the negative or positive rails of the power supply
- use star grounds, if at all possible, in high current applications

REFERENCES

[1] *Tiny 1.5A, High-Speed Power MOSFET Driver Data Sheet* (DS22092) Microchip Technology Inc., 2008.

4.0A Dual High-Speed Power MOSFET Drivers With Enable Data Sheet (DS22062) Microchip Technology Inc., 2008.

2A Synchronous Buck Power MOSFET Driver Data Sheet (DS220830) Microchip Technology Inc., 2008.

Tiny 500 mA, High-Speed Power MOSFET Driver Data Sheet (DS22052) Microchip Technology Inc., 2007.

4.5A Dual High-Speed Power MOSFET Drivers Data Sheet (DS22022) Microchip Technology Inc., 2007.

3A Dual High-Speed Power MOSFET Drivers Data Sheet (DS21998), Microchip Technology Inc., 2007.

[2] *EIA/JEDEC Standard JESD51-7*, “High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages”, Electronic Industries Alliance, February 1999.

[3] *Latch-Up Protection For MOSFET Drivers Application Note AN763* (DS00763), Microchip Technology Inc., 2009.

APPENDIX A: CIRCUIT NETLIST

```
******************   Circuit Netlist ********************************************

X1 VOUT V2_P L5_N L4_P TC4423A
V1 L3_N 0 15
V2 V2_P 0 PULSE 0 5.5 0 10n 10n 4.99u 10u
R1 V2_P 0 1K
L1 C3_P L1_N 10n
L2 C1_P L1_N 10n
L3 L1_N L3_N 100n
L4 L4_P 0 10n
L5 L1_N L5_N 10n
C1 C1_P 0 1u
C2 VOUT 0 1n
C3 C3_P 0 1u
.TRAN 20u 20u
.SUBCKT TC4423A 2 1 3 4
*                                |  |  |  |
*                                |  |  |  | Negative Supply
*                                |  |  | Positive Supply
*                                |  |  Input
*                                |  Output
*
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********************************************************************************
*
* The following MOSFET drivers are covered by this model:
*      3A Inverting Driver - TC4423A
*
* Polarity: Inverting
*
* Date of model creation: 11/14/2008
* Level of Model Creator: G
*
```

```
* Revision History:
*      11/14/08 RAW Initial model creation
*      11/20/08 RAW Adjusts to rise/fall times
*
*
*
*
*
* Recommendations:
*      Use PSPICE (or SPICE 2G6; other simulators may require translation)
*      For a quick, effective design, use a combination of: data sheet
*            specs, bench testing, and simulations with this macromodel
*      For high impedance circuits, set GMIN=100F in the .OPTIONS statement
*
* Supported:
*      Typical performance for temperature range (-40 to 125) degrees Celsius
*      DC, AC, Transient, and Noise analyses.
*      Most specs, including: propgation delays, rise times, fall times, max sink/source current,
*            input thresholds, voltage ranges, supply current, ... , etc.
*      Temperature effects for Ibias, Iquiescent, output current, output
*            resistance,....,etc.
*
* Not Supported:
*      Some Variation in specs vs. Power Supply Voltage
*      Vos distribution, Ib distribution for Monte Carlo
*      Some Temperature analysis
*      Process variation
*      Behavior outside normal operating region
*
* Known Discrepancies in Model vs. Datasheet:
*
*
*
* Input Impedance/Clamp
R1  4    1    100MEG
C1  4    1    20.0P
G3  3    1    TABLE { V(3, 1) } ((-770M,-1.00)(-700M,-10.0M)(-630M,-1.00N)(0,0)(20.0,1.00N))
G4  1    4    TABLE { V(1, 4) } ((-5.94,-1.00)(-5.4,-10.0M)(-4.86,-1.00N)(0,0)(20.0,1.00N))
* Threshold
G11 0    30   TABLE { V(1, 11) } ( (-1m,10n)(0,0)(0.78,-.1)(1.25,-1)(2,-1) )
G12 0    30   TABLE {V(1,12)} ( (-2,1)(-1.2,1)(-0.6,.1)(0,0)(1,-10n))
G21 0    11   TABLE { V(3, 4) } ((0,1.35)(4.00,1.35)(6.00,1.5)(10.0,1.48)(13.0,1.49)(16.0,1.5))
G22 0    12   TABLE { V(3, 4) } ((0,1.35)(4.00,1.16)(6.00,1.25)(10.0,1.24)(13.0,1.24)(16.0,1.25))
R21 0    11   1 TC 504U  2.33U
R22 0    12   1 TC 231U  -103N
C30 30   0    1n
* HL Circuit
G31 0    31   TABLE { V(3, 4) } ((0,170)(4.5,80)(10.0,46.2)(12.0,39.1)(14.0,35.8)(18.0,35.1))
R31 31   0    1 TC 2.42M  -3.91U
G33 0    30   TABLE { V(31, 30) } ( (-1M,-10)(0,0)(1,10N) )
S31 31   30 31 30 SS31
* LH Circuit
G32 32   0    TABLE { V(3, 4) }
((0,190)(4.5,52)(5,67)(10.0,41.0)(12.0,38.6)(14.0,34.5)(18.0,36.8))
R32 0    32   1 TC 2.50M  1.09U
G34 30   0    TABLE { V(30, 32) } ( (-1M,-10)(0,0)(1,10N) )
R30 32   30   1MEG
* DRIVE
G51 0    50   TABLE { V(30, 0) } ( (-5,-1U)(-3,-1U)(0,0)(6,4)(18,4.1) )
G52 50   0    TABLE { V(0, 30) } ( (-5,-1U)(-3,-1U)(0,0)(6,3.5)(18,3.6) )
R53 0    50   1
G50 51   60   VALUE {V(50,0)*300M/(-700M+18.0/(V(3,4) + 1M))}
R51 51    0   1
G53  3    0   TABLE {V(51,0)} ((-100,100)(0,0)(1,1n))
G54  0    4   TABLE {V(0,51)} ((-100,100)(0,0)(1,1n))
```

```
R60 0    60   100MEG
H67 0    69   V67 1
V67 60   59   0V
C60 561  60   1000P
R59 59   2    1.28
L59 59   2    5.0N
* Shoot-through adjustment
VC60 56 0 0V
RC60 56 561 1m
H60 58 0 VC60 56
G60P 0 3 TABLE { V(58, 0) } ((-1,-1u)(0,0)(20,0)(200,-2))
G60N 4 0 TABLE { V(0, 58) } ((-1,-1u)(0,0)(20,0)(200,-2))
* Source Output
E67 67   0    TABLE { V(69, 0) } ( (-4.5,-4.5)(0,0)(1,2.00) )
G63 0    63   POLY(1) 3 4 6.81 -439M 12.9M
R63 0    63   1 TC 3.45M -4.18U
E61 61   65   VALUE {V(67,0)*V(63,0)}
V63 65   3    100U
G61 61   60   TABLE { V(61, 60) } (-20.0M,-450)(-15.0M,-225)(-10.0M,-45.0)(0,0)(10,1N))
* Sink Output
E68 68   0    TABLE { V(69, 0) }  ( (-1,-2.00)(0,0)(4.5,4.5) )
G64 0    64   POLY(1) 3 4 6.49 -455M 12.6M
R64 0    64   1 TC 3.18M -5.83U
E62 62   66   VALUE {V(68,0)*V(64,0)}
V64 66   4    100U
G62 60   62   TABLE { V(60, 62) } (-20.0M,-450)(-15.0M,-225)(-10.0M,-45.0)(0,0)(10,1N))
* Bias Current
G55 0    55   TABLE { V(3, 4) } ((0,0)(4.5,75.0U)(10.0,97.5U)(14.0,120U)(18.0,145U))
G56 3    4    55 0 1
R55 55   0    1 TC  2.49M -16.9U
G57 0    57   TABLE { V(3, 4) } ((0,0)(4.5,35.0U)(10.0,37.5U)(14.0,40.0U)(18.0,40.0U))
G58 3    4    57 0 1
R57 57   0    1 TC  1.03M 15.4U
S59 55   0    1 0 SS59
* Models
.MODEL SS59 VSWITCH Roff=1m Ron=100Meg Voff=1.2V Von=1.5V
.MODEL SS31 VSWITCH Roff=100MEG Ron=800 Voff=0.2V Von=0.1V
.ENDS
```

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