AN1321

KEELOQ® Microcontroller-Based Transmitter with Acknowledge

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INTRODUCTION

This application note describes the design of a microcontroller-based KEELOQ® transmitter with receiver acknowledge using the KEELOQ encryption algorithm. This transmitter is implemented on the Microchip PIC16F636 microcontroller. Descriptions of the encoding process, the encoding hardware and description of the software modules are included within this application note. The software was designed to be backwards compatible with an HCS365 dual transmitter in terms of memory map programming.

The software used in this implementation makes use of the PIC16F636 internal encryption engine to generate the hopping codes required for transmission. This design can be used to implement a secure system transmitter that has the flexibility to be designed into various types of KEELOQ receiver/decoders. The Acknowledge is achieved by using an MRF49XA transceiver.

TRANSMITTER OVERVIEW

The transmitter has the following key features:

Security

- Two programmable 28-bit serial numbers
- Two programmable 64-bit encryption keys
- Two programmable 32-bit user values
- Each transmitter is unique
- 64-bit transmission code length
- 32-bit hopping code

Operation

- 2.0-5.5V operation
- Four-button inputs
- Automatic packet retry feature
- Nonvolatile synchronization data
- FSK modulation (handled internally by the MRF49XA)
- Dual transmitter functionality

DUAL TRANSMITTER OPERATION

This firmware contains two transmitter configurations with separate serial numbers, transmitter keys, user values, counters and seed values. This means that the transmitter can be used as two independent systems. The SHIFT (S3) input pin is used to select between transmitter configurations. When the dual transmitter feature is disabled, the button acts as a local status request, displaying the last received status on the LEDs.

RECEIVER ACKNOWLEDGE

On any button press, a data packet is sent over the air. The transmitter then goes to Receive mode for a period of time. During this time, the MRF49XA transceiver is in Receive mode and waits for a data packet coming back from the receiver. If no packet is received from the receiver end, then the transmitter has the ability to re-send the data packet (if the feature is enabled). The Acknowledge indication is done using the two LEDs on the transmitter board.

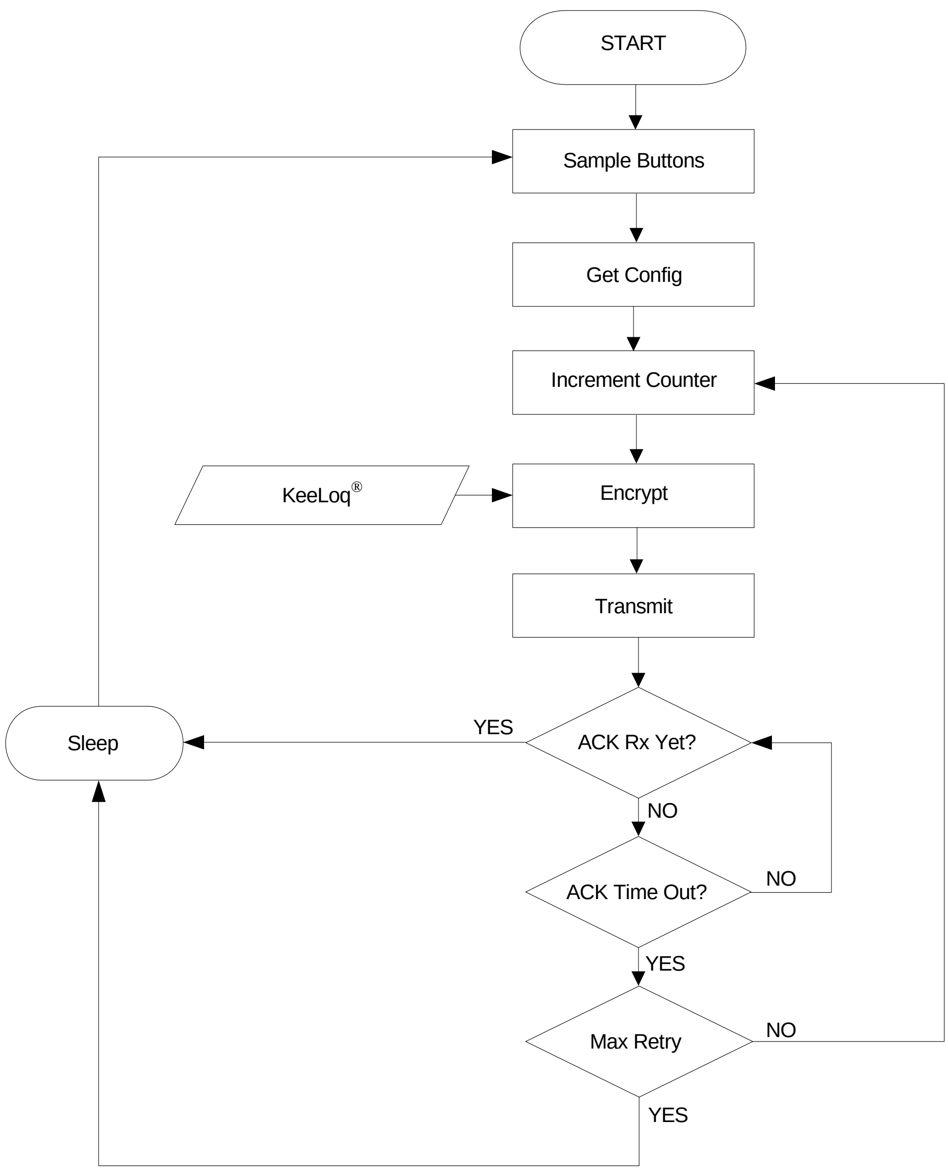
SAMPLE BUTTONS/WAKE-UP

Upon power-up, the transmitter verifies the state of the buttons inputs and determines if a button is pressed. If no button press is detected, the transmitter will go to Sleep mode. The transmitter will wake-up whenever a button is pressed. Wake-up is achieved by configuring the input port to generate an interrupt-on-change. The button input values are then placed in the transmission buffer, in the appropriate section.

LOAD SYSTEM CONFIGURATION

After waking up and debouncing the input switches, the firmware will read the system Configuration bytes. All the system Configuration bytes are stored in the EEPROM. Below is the EEPROM mapping for the PIC16F636 transmitter showing the Configuration and data bits stored.

FIGURE 1: SOFTWARE FLOW DIAGRAM



MRF49XA RADIO CONFIGURATION

The radio link parameters in the MRF49xA are set to a default configuration that is adequate for the majority of applications. The baud rate is 9600 bps, using an FSK modulation with deviation of 60 kHz. For a more detailed description on how to setup the MRF49XA, please refer to AN1252, *"Interfacing the MRF49XA Transceiver to PIC® Microcontrollers"*.

The following considerations were made to select the MRF49XA Configuration Words.

The configuration considers the use of standard 30ppm crystal accuracy. Such a crystal will generate a frequency error of:

EQUATION 1:

$$\Delta f_0 = \frac{30ppm}{10^6} * 915 * 10^6 = 27.45kHz$$

The deviation can now be calculated:

EQUATION 2:

$$\Delta f_{FSK} = 9600 + 2 * \Delta f_0 + 10 * 10^3$$

For the above values, we get a result of 74.5 kHz. The closest deviation supported by the MRF49XA transceiver is 75 kHz. For a maximum power output and a 75 kHz deviation, a value of 0x9840 is loaded into the TXCREG register.

Now, we can calculate the baseband bandwidth:

EQUATION 3:

$$BBBW = deviation*2 - 10 * 10^3\ Hz$$

For the above values, we get a result of 140 kHz. Picking a BBBW of 200 kHz, an RSSI of minus 97 dBm, and a maximum LNA gain, we get a value of 0x9481 to be loaded into the RXCREG register.

This code to configure the transceiver is contained in module `MRF49XA.c`.

TABLE 1: EEPROM MAPPING FOR THE KEELOQ® TRANSMITTER

Offset	Description	MNEMONIC
0x00	Sync Counter Transmitter 0	`EE_CNT0`
0x01	Sync Counter Transmitter 0	
0x02	Sync Counter Transmitter 0	
0x03	Sync Counter Transmitter 0, Checksum AB	
0x04	Sync Counter Transmitter 0, Checksum BC	
0x05	Sync Counter Transmitter 0, Checksum AC	
0x06	—	
0x07	—	
0x08	Sync Counter Transmitter 1	`EE_CNT1`
0x09	Sync Counter Transmitter 1	
0x0A	Sync Counter Transmitter 1	
0x0B	Sync Counter Transmitter 1, Checksum AB	
0x0C	Sync Counter Transmitter 1, Checksum BC	
0x0D	Sync Counter Transmitter 1, Checksum AC	
0x0E	—	
0x0F	—	
0x10	32-BIT SERIAL NUMBER for TX#0 (MSB)	`EE_SER0`
0x11	32-BIT SERIAL NUMBER for TX#0	
0x12	32-BIT SERIAL NUMBER for TX#0	
0x13	32-BIT SERIAL NUMBER for TX#0 (LSB)	
0x14	—	
0x15	—	
0x16	—	
0x17	—	
0x18	—	
0x19	—	

TABLE 1: EEPROM MAPPING FOR THE KEELOQ® TRANSMITTER (CONTINUED)

0x1A	—	
0x1B	—	
0x1C	DISC_0	EE_DISC
0x1D	—	
0x1E	64-BIT KEY (MSB) for TX #0	EE_KEY0
0x1F	64-BIT KEY for TX #0	
0x20	64-BIT KEY for TX #0	
0x21	64-BIT KEY for TX #0	
0x22	64-BIT KEY for TX #0	
0x23	64-BIT KEY for TX #0	
0x24	64-BIT KEY for TX #0	
0x25	64-BIT KEY-0 (LSB) for TX #0	
0x26	32-BIT SERIAL NUMBER for TX#1 (MSB)	EE_SER1
0x27	32-BIT SERIAL NUMBER for TX#1	
0x28	32-BIT SERIAL NUMBER for TX#1	
0x29	32-BIT SERIAL NUMBER for TX#1 (LSB)	
0x2A	—	
0x2B	—	
0x2C	—	
0x2D	—	
0x2E	—	
0x2F	—	
0x30	—	
0x31	—	
0x32	DISC_1	
0x33	—	
0x34	64-BIT KEY (MSB) for TX#1	EE_KEY1
0x35	64-BIT KEY for TX#1	
0x36	64-BIT KEY for TX#1	
0x37	64-BIT KEY for TX#1	
0x38	64-BIT KEY for TX#1	
0x39	64-BIT KEY for TX#1	
0x3A	64-BIT KEY for TX#1	
0x3B	64-BIT KEY (LSB) for TX#1	
0x3C	—	
0x3D	EE_CFG	EE_CFG
0x3E	—	
0x3F	—	

TABLE 2: TRANSMITTER CONFIGURATION OPTIONS

BIT	Field	Description	Values
0	MRT	Maximum number of transmission retries	00 – None 01 – Once 10 – Twice 11 – Three times
1			
2	INDESEL	Dual Transmitter Enable	0 = Disable 1 = Enable
3	Not used	—	-
4	TSEL	Time-out Select	00 – 300 ms 01 – 500 ms 10 – 1000 ms 11 – 2000 ms
5			
6	Not used	—	—
7	Not used	—	—

EE_SER0 AND EE_SER1

These locations store the 4 bytes of the 32-bit serial number for transmitter 1 and transmitter 2. There are 32 bits allocated for the serial number and the serial number is meant to be unique for every transmitter.

EE_DISC0 AND EE_DISC1

These locations store the 8-bit discrimination value. This value is typically the 8 LSBs of the serial number. This field can serve as a post decryption packet check.

EE_KEY0 AND EE_KEY1

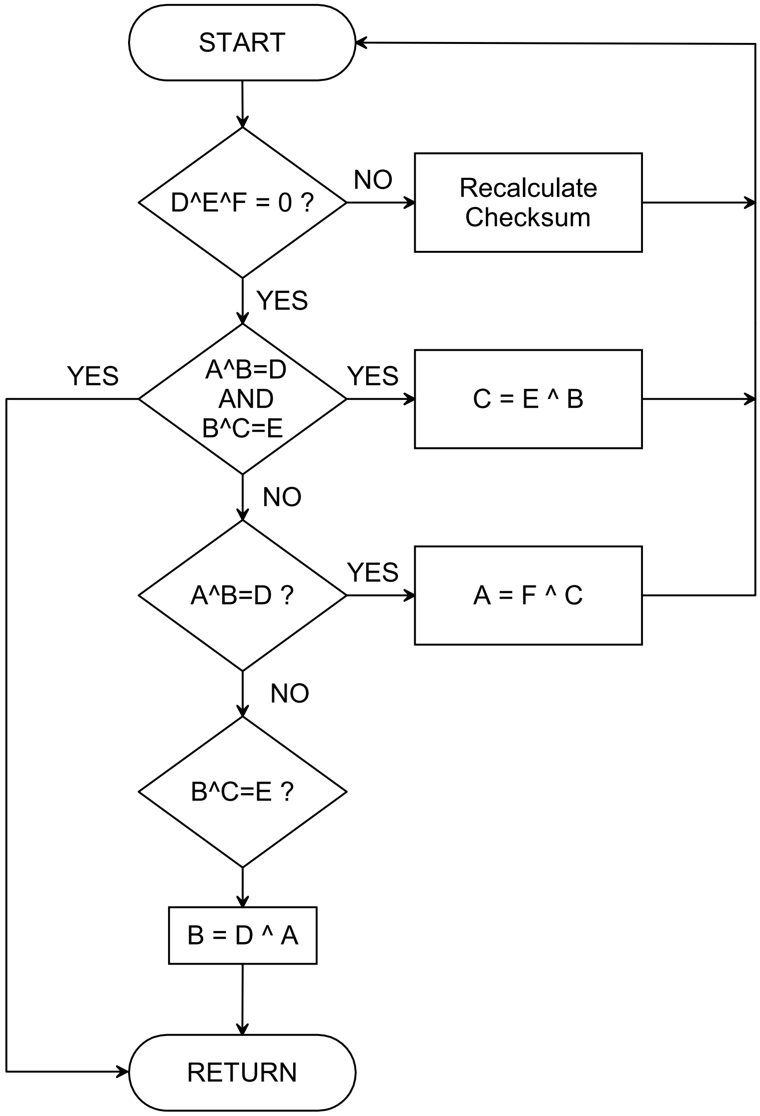
The 64-bit encryption key is used by the transmitter to create the encrypted message transmitted to the receiver. This key is created using a key generation algorithm. The inputs to the key generation algorithm are the secret manufacturer's code, and the serial number. The user may choose to use the algorithm supplied by Microchip or to create their own method of key generation.

SYNCHRONIZATION COUNTER STORAGE

The following addresses save the counter and the checksum values. The counter value is stored in the counter locations (EE_CNT0 for transmitter 1 and EE_CNT1 for transmitter 2) described in the EEPROM table. This code is contained in module counter.c.

Along with the counter values, three counter checksums are stored. These are calculated by a XOR operation between different bytes of the counter value. Thus, three new values are being used: A XOR B, B XOR A, and C XOR A. When reading the counter value from EEPROM memory, the counter values are being checked and, if necessary, they are being corrected using the checksum values. The firmware flow diagram is shown in Figure 2.

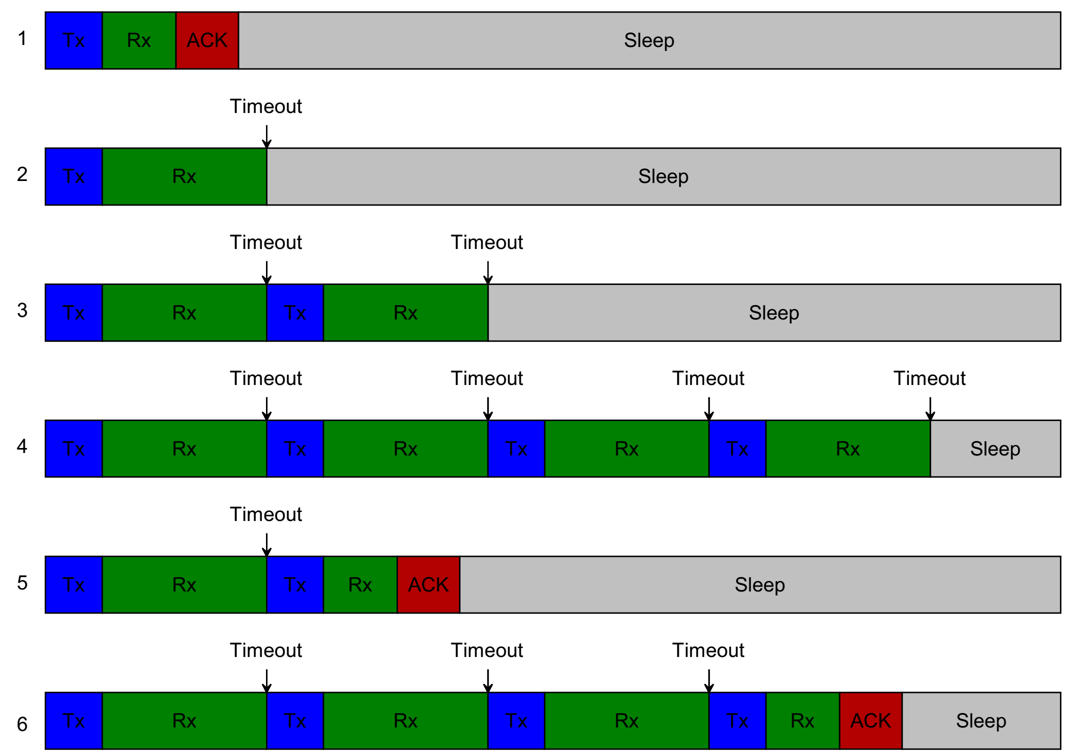
FIGURE 2: COUNTER CHECK DIAGRAM



AUTOMATIC RETRY

Upon transmission of a data packet, the transmitter waits for reception of acknowledge from the receiver. The Acknowledge reception can occur after the transmission of a radio packet. A time-out period is used and, if the Acknowledge is not received, the reception is aborted. The time-out period is set according to the TSEL field of the Configuration register. If a packet acknowledge is not received, the transmitter has the ability to resend the data packet and wait for another acknowledge. The number of retries is defined in the MRT field of the Configuration register. This feature can be enabled, with a maximum of three retires, or it can be completely disabled. The sequence can be one of the following scenarios (see Figure 3).

FIGURE 3: DIFFERENT ACKNOWLEDGE SCENARIOS



In Figure 3 we see a total of six different acknowledge scenarios.

The first one is the most simple and will occur for the majority of time under normal conditions. Immediately after a transmission, the transmitter goes to Listening mode waiting for acknowledge. In this case, acknowledge is received on time and no time-out event occurs.

The second case represents a transmitter that has the automatic retry feature disabled. After a time-out event, the transmitter is not sending a new transmission.

In cases 3 and 4, we can see the transmitter's automatic retry feature. After a time-out event, the transmitter sends a new data packet. In case 4, no acknowledge is received, even though the transmitter retried three times – the maximum allowed by the MRT setting.

In cases 5 and 6, we have a successful acknowledge on the first transmission retry and on the third transmission retry.

CODE TRANSMISSION FORMAT

The following is the data stream format transmitted (Table 3):

TABLE 3: KEELOQ® PACKET FORMAT

Plain Text (32 bits)	Encrypted (32 bits)		
Serial number (32 bits)	Function code (8 bits)	Discrimination (8 bits)	Counter (16 bits)

A KEELOQ transmission consists of 32 bits of hopping code data and 32 bits of fixed code data.

HOPPING CODE PORTION

The hopping code portion is calculated by encrypting the function code, serial number, user code, counter, and a checksum with the Transmitter Key (KEY). A new hopping code is calculated every time a button is pressed. The user code can be programmed with any fixed value to serve as a post decryption check on the receiver end. This code portion is transmitted in encrypted format.

FIXED CODE PORTION

The fixed code portion consists of 32 bits of serial number and, therefore, is transmitted in non-encrypted format (plain text).

FIRMWARE MODULES

The following files make up the KEELOQ transmitter firmware:

- `main.c`: this file contains the main loop routine, as well as the wake-up, debounce, read configuration, load transmit buffer and transmit routines.
- `packet.c`: this file loads the transmit buffer according to the encryption algorithm.
- `MRF49XA.c`: this file contains all the functions that control the MRF49XA transceiver.
- `counter.c`: this file loads the synchronization counter, checks its validity and automatically corrects any errors.
- `encryption.c`: this file contains the functions that provide the encryption algorithm. Because of statutory export license restrictions on encryption software, the source code listings for the AES algorithms are not provided here.

These applications may be ordered from Microchip Technology Inc. through its sales offices, or through the corporate web site: www.microchip.com.

FIRMWARE CONFIGURATION

The transmitter firmware is fully configurable. The encryption algorithm can be changed very easily. All the necessary functions and definitions are contained in the `encryption.c` and `encryption.h` modules. Changing the encryption algorithm is as simple as replacing the above module and recompiling the source code.

CONCLUSION

This KEELOQ transmitter firmware has all the features of a standard hardware transmitter. What makes this firmware implementation useful is that it gives the designer the power and flexibility of modifying the encoding and/or transmission formats and parameters to suit their security system. In addition, this system allows the user to receive acknowledge from the intended receiver.

REFERENCES

C. Toma, AN1252, "*Interfacing the MRF49XA Transceiver to PIC® Microcontrollers*", (DS01252), Microchip Technology Inc., 2009.

ADDITIONAL INFORMATION

Microchip's Secure Data Products are covered by some or all of the following:

Code hopping encoder patents issued in European countries and U.S.A.

Secure learning patents issued in European countries, U.S.A. and R.S.A.

REVISION HISTORY

Revision B (June 2011)

- Added new section **Additional Information**
- Minor formatting and text changes were incorporated throughout the document

ISBN: 978-1-61341-254-1

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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