

AN1302

An I²CTM Bootloader for the PIC16F1XXX Enhanced Core

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INTRODUCTION

The new PIC16F1XXX enhanced core microcontroller has the ability to write its own program memory under software control. This allows the microcontroller to make modifications in the program Flash memory. This application note explains the implementation of a bootloader using I^2C^{TM} as a communication channel.

BOOTLOADER CONCEPT

The bootloader allows a processor to change its firmware without any physical intervention to the device itself. There is no need for a hardware programmer when using the bootloader. The firmware is downloaded from a host system by means of a communication channel, usually through a USB or a serial port. This bootloader implementation uses a standard I²C bus as a communication channel between the microcontroller and the host system.

In general, when using a bootloader, the code is transferred from a host device. Typically, this is comprised of a PC computer using a RS-232 serial cable or a USB port. Any other device can act as a host device.

The target device needs bootloader firmware. This is basically a software that accepts commands and data from a host device and reads/erases/writes data to the Flash program memory. This firmware is typically located on the lower part of the program memory. The bootloader code is started by default at system Reset. It then checks if there is any application code loaded and jumps into application code if any is found. Alternatively, a button can be used to instruct the bootloader to stay in bootloader code even if a firmware is already present. This is useful when reading the application firmware or in case of an application firmware update.

BOOTLOADER REQUIREMENTS

The bootloader makes it unnecessary for any physical intervention with a hardware programmer. The target device must have some form of data connection with the host. In this application note, I^2C communication is used. If the device uses the I^2C port to communicate with other devices on the bus, then no additional connection is needed.

The bootloader will require the lower side of the program memory reserved for the bootloader firmware (see Figure 1). The rest of the program memory can be used by application. No RAM memory needs to be reserved, since it is used in different contexts and not at the same time.

FIGURE 1: FLASH MEMORY MAP



BASIC OPERATION

The basic functionality of a bootloader is to receive, interpret and execute a set of commands known both by the host software and the target firmware. The command set can be more or less complex than shown in the application note, but it must generally support commands to read, erase and write the Flash memory. Additionally, it must support a command to jump from the bootloader code to the application code. This command is typically issued at the end of a program/verify cycle. The application code might require a command to exit the application code and enter the bootloader code.

ERASING PROGRAM MEMORY

The program memory can be erased under software control only in rows of instructions. A row consists of 32 instruction words of program memory. Please note that the address must be aligned to a 32-word boundary (EEADRL <4:0> = $0 \ 0 \ 0$).

Because the erase sequence can modify existing data, the special unlock sequence is needed. The unlock sequence consists in consecutive write values 0x55, 0xAA to the EECON2 register.

UPDATING PROGRAM MEMORY

Before writing to the program memory, an erase operation should be performed. The program memory is written in blocks. A block consists of 8 words of program memory data with sequential address, aligned to an 8-word boundary (EEADRL <2:0> = $0 \ 0 \ 0$). If smaller blocks of memory need to be modified, then a read-modify-erase program approach should be used, as the program memory can only be written in 8-word blocks.

An erase operation sets the value of 0x3FFF to all erased locations. This corresponds to an all-ones in binary.

BOOTLOADER COMMANDS

The bootloader firmware used in this design supports a set of commands used to read, erase and write to the Flash memory of the target device. The commands are shown in Table 1.

Command	Name	Read/Write	Description
0x01	Set/Get Address Pointer	R/W	Sets/Reads the Address Pointer. Data is written/read in two bytes format, MSB first.
0x02	Download data to internal buffer	-/W	8 words of data are downloaded from the host into an internal buffer. Data is downloaded MSB first starting from the lower address. This command is usually followed by a Write command (0x05).
0x03	Read Flash command	R/-	Reads 8 words from the Flash memory starting with the address specified by the Address Pointer. The Address Pointer is automatically incremented by 8 words upon a read.
0x04	Erase Flash command	R/-	Erases a row of 32 words starting with the address specified by the Address Pointer. The Address Pointer must be aligned to a 32-word boundary (0x0000, 0x0020, 0x0040, 0x0060). The Address Pointer is automatically advanced by 32 words. This command uses clock stretching and returns a dummy 0x00 byte after command completion.
0x05	Write Flash command	R/-	The data that is stored into the buffer is written into the Flash memory at the address pointed to by the Address Pointer. The Address Pointer is automatically incremented by 8 words upon a successful write. This command uses clock stretching and returns a dummy 0x00 byte after command completion.
0x06	Jump to application code	R/-	Usually used after a successful firmware download. The application resets itself and jumps to the application segment. This command uses clock stretching and returns a dummy 0x00 byte after command completion.

TABLE 1: BOOTLOADER COMMANDS

BOOTLOADER FIRMWARE

As mentioned before, the bootloader firmware resides in the lower part of the Flash memory. The firmware receives, interprets and executes a set of I²C commands (the complete list of commands is described in Table 1). In order to respond to the I^2C commands, the firmware must access the Flash memory. For some commands that involve operations with the internal Flash memory that takes time to complete the operation. These commands are implemented as I²C Read command. They will return a dummy 0x00 byte after the operation has completed. During this time, the slave will clock stretch the I²C bus by pulling the SCL line low to signal the master device that the operation has not completed. The download of data to the internal buffer does not need any response from the target system, thus the command is implemented as a normal I²C Write command.

The structure of the I^2C commands is described in the following. These are implemented as the target being an I^2C slave device.

General configuration of an I^2C write operation (see Table 2):

- 1. Send a "Start" condition to the slave device
- Send the device address with the R/W bit low (even address). If the sent address matches the slave device address, then the slave device sends an ACK signal.
- 3. Send the internal register number you want to write to.
- 4. Send data. Depending on the command used, the master can send multiple data bytes. Please note that the master device can send a multiple number of bytes.
- 5. Send a "Stop" condition.

MAND	
١	IAND

Start	Address	Register	Data (nbytes)	Stop

General configuration of an I^2C read operation (see Table 3):

- 1. Send a "Start" condition.
- Send the device address with the R/W bit low (even address). Notice that the slave sends an Acknowledge signal if the address matches.
- 3. Send the bootloader command number you want to read from.
- 4. Send a "Restart" condition.
- 5. Send the device address again. This time with the R/W bit high (odd address).
- Read a number of bytes from the slave device. If data is not yet available, the slave will use clock stretching (pull SCL line low).
- 7. Send a "Stop" condition

TABLE 3: I²C READ COMMAND

Start	Address	Address Register		Restart Address		Stop
					(nbytes)	

The bootloader code must exit after completing the download of the new firmware. This is typically implemented using a Reset instruction. The decision to go to bootloader code or application code is based on a bootloader flag placed in the Flash memory. The location of this flag is at the highest address of Flash memory for the target device. In the current implementation using the PIC16F1937, this location is 0x1FFF. Other devices might have more or less available Flash program memory and the last available Flash memory location will vary accordingly. Following an Erase command, the data at address 0x1FFF is 0x3FFF. After a successful code download and verify, the data contained at this address will be changed to a special value (0x55), indicating that an application is loaded. When the application code needs to jump to the bootloader code it will write an all-zeros value to the bootloader flag address. When writing an all-zeros value to a Flash memory location there is no need for a previous erase operation. An erase operation sets the Flash memory location to an all-ones value. The special value can be either contained in the application hex file or written by the bootloader upon a successful code update.

Alternatively, any means of code-present flags can be used, such as flags in EEPROM memory or any other address in the Flash memory.

The full source code of the bootloader is available with this application note. The firmware runs on the F1 Evaluation Platform containing a PIC16F1937. Three demo applications are provided along with this application note. These are relatively simple and are provided with the purpose of demonstrating firmware upload. The first two applications are just "Hello world" kind of firmware. The third application showcases the use of interrupt forwarding.

FIRMWARE FUNCTION DESCRIPTIONS

Among the functions of the bootloader firmware, some of them are more important:

 do_{i2c}_{tasks} : This function services all the I²C related events. The event decoding is based on the SSPIF flag and the SSPSTAT register.

flash_memory read: This function takes a 16-bit value as a address parameter and returns the data read from Flash memory at the specified location.

flash_memory_write: This function has two parameters. The first one is a 16-bit value as an Address Pointer. Please note that the address must be properly aligned to an 8 word boundary. The second parameter is a pointer to buffer containing the data being written. It does not return any value (void).

flash_memory_erase: Performs an erase operation starting with the address specified as a parameter. 32 instruction words are erased in a row and the specified address must be aligned to a 32 word boundary.

service_isr: This function performs the interrupt forwarding feature. It is implemented as a GOTO instruction. For more information see the following section.

INTERRUPT FORWARDING

The PIC16F1XXX enhanced core has the interrupt vector at 0x0004. This address is located in the area where the bootloader firmware is located. To maintain the interrupt functionality it is required that the Interrupt Service Routine (ISR) be relocated at a different address, in the application segment. In the bootloader code, at the interrupt vector location (0x0004), a GOTO instruction is present. The Interrupt Service Routine is contained in the application code. The application code is shifted by 0x200, leaving room for the bootloader in the lower part of the Flash memory. It will also contain the Interrupt Service Routine at 0x0204. The bootloader code will contain a "GOTO 0x0204" instruction. When an interrupt occurs, the program counter (PC) jumps to 0x0004 in the bootloader segment. At this address, the "GOTO 0x0204" instruction will cause the PC to jump to 0x0204 in the application segment, where the Interrupt Service Routine is located (see Figure 1). Please notice that the PIC16F1XXX enhanced core features Automatic Context Saving.

The interrupt latency will be increased by the GOTO instruction execution time. See the example demo application(s) for more details.

MULTIPROCESSOR SYSTEM

Since the proposed bootloader uses a standard I²C protocol, the target microcontroller can be interfaced with a larger microcontroller having more processing power (such as a main processor in a multiprocessor system). Several such devices can be connected in parallel on the I²C bus, each slave device having its own address (see Figure 2).



FIGURE 2: MULTIPLE SLAVE DEVICES CONNECTED TO THE SAME BUS

PC SIDE SOFTWARE

The bootloader presented here uses an I^2C bus as a communication channel. The main use for such a bootloader is in a multiprocessor system where the main processor can update the firmware of several processors in the same system.

We can, however, use PC software if we use a device that will act as a master I²C device controlled by PC software. We used the PICkitTM Serial analyzer configured as I²C master device.

The software is written using Visual C# 2008, Express Edition. The PC software has the primary function of importing the hex file, splitting it into smaller packets and sending the data to the bootloaded device. Reading back program data from the device is also possible. When designing the firmware for the main processor in a multiprocessor system, the above software can serve as a starting point.

FIGURE 3: PC HOST APPLICATION WINDOW

-ile B	ootloader	About							
PKSA co	onfigured for I	2C mast	er						
0+020	0 2666	2666	2666	2666	2666	2666	2666	2666	
0x020	0 3111	DEEE	2666	SEEE	2666	2666	2666	2666	-
0x020	0 3666	SEEE	SEEE	SEEE	SEEE	SEEE	2666	SEEE	
0x021	0 3111 0 3666	2666	2666	2666	SEEE.	2666	2666	2666	
0x021	0 3666	SEEE	SEEE	SEEE	SEEE	SEEE	SEEE	SEEE	
0x022	0 3666	2666	SEEE	2666	SEEE	2666	2666	2666	_
0x022	0 3666	SEEE	SEEE	SEEE	SEEE	SEEE	SEEE	SEEE	
0x023	0 3fff	SEE	SEEE	SEEE	SEEE	SEEE	SEEE	SEEE	
0x023	0 3666	SEFE	SEEE	SEEE	SEEE	SEEE	SEFE	SEEE	
0x024	8 3fff	SEE	SEEE	SEEE	SEEE	SEEE	SEEE	SEEE	
0x025	0 3666	SEFE	SEEE	SEEE	SEFE	SEFE	SEFE	SEEE	
0x025	8 3fff	Sfff	Sfff	3fff	3fff	Sfff	Sfff	Sfff	
0x026	0 3666	3fff	3fff	3fff	3fff	3fff	3fff	3fff	
0x026	8 3fff	Sfff	Sfff	Sfff	SEEE	Sfff	Sfff	Sfff	
0x027	0 3666	3fff	3fff	3fff	3fff	3fff	3fff	3fff	
0x027	8 3fff	Sfff	Sfff	Sfff	SEEE	Sfff	SEE	Sfff	
0.027	o orre	OLLL	OLLL	OLLL	OLLL	OTTT	OLLL	OLLL	

To upload a new hex file to the device you must first open the hex file. This can be done using the Import Hex command found in the File menu (see Figure 3). You will notice that the content of the currently loaded file is displayed in the lower side of the window. Once the new firmware is loaded, it is ready to be sent to the target device. This is done by using the Program command under the Bootloader menu. The programming operation will consist in a full erase followed by a firmware download. The erase-only operation is available in the same menu. The firmware can also be read from the target device using the Read command in the Bootloader menu. The program memory data can be saved into a hex file using the Export Hex command in the File menu. After a successful firmware download operation, switching to the application code is done using the Run firmware command in the Bootloader menu.

CONCLUSION

Using a bootloader is a very efficient way to allow firmware upgrades in the field. Products can be easily upgraded to support new features. Fixing code bugs is also easier.

The bootloader code occupies the lower part of the program memory between 0x0000 and 0x01FF (512 bytes). The bootloader features interrupt forwarding to allow applications to use interrupts.

When using I²C communication, multiple bootloaded devices can be connected on the same bus, each device having it's own address.

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