

# Single-Shunt Three-Phase Current Reconstruction Algorithm for Sensorless FOC of a PMSM

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# INTRODUCTION

A large number of motor control applications are consistently and continuously looking for methods to improve efficiency while reducing system cost. These are the two main factors that are driving the efforts to improve existing motor control techniques, such as trapezoidal control, scalar control and Field-Oriented Control (FOC).

FOC has become more popular in recent years due to the fact that the cost required to implement this technique is no longer a constraint. The available technology and manufacturing process now make it possible to implement this control technique in a 16-bit fixed-point machine such as the dsPIC<sup>®</sup> Digital Signal Controller (DSC).

Efficiency is another reason that has allowed FOC to gain ground over scalar and trapezoidal control techniques on low-cost and mid-cost applications. It is also well suited in applications in which hard requirements are low noise, low torque ripple and good torque control over a vast speed range.

Field-oriented control can be implemented using position sensors such as encoders, resolvers or Hall sensors. However, not all motor control applications require such granularity given by a resolver or encoder; and, in many cases, they do not require control at zero speed.

These applications are a perfect target for using sensorless techniques in which the motor position can be estimated using the information provided by the currents flowing through the motor coils. There are two popular approaches to this sensing technique: the dual-shunt resistor and the single-shunt resistor.

The dual-shunt resistor technique utilizes the information contained in the current flowing through two motor coils in order to estimate the motor position. The single-shunt resistor technique utilizes only the information contained in the current flowing through the DC bus to reconstruct the three-phase currents, and then estimate motor position.

In this application note, the single-shunt approach is discussed. For information on the dual-shunt resistor approach, please refer to the application note, AN1078 *"Sensorless Field Oriented Control of PMSM Motors"*.

# **CURRENT MEASUREMENT**

The information contained in the current flowing through the motor coils allows a motor control algorithm to operate the motor in a region where the motor produces the maximum torque, or to operate the motor at certain performance, or even to be able to approximate or estimate internal motor variables such as position.

Three-phase AC Induction Motors (ACIMs), Permanent Magnet Synchronous Motors (PMSMs) and Brushless Direct Current (BLDC) motors in particular use a three-phase inverter as the topology of preference. This topology, which is shown in Figure 1, allows individual control of the energy applied to each coil, which enables the motor to be efficiently operated.



#### FIGURE 1: THREE-PHASE INVERTER TOPOLOGY

The three-phase inverter is compounded by three legs. Each leg contains two electronic switches that are arranged in such a way that create a half-bridge topology. Therefore, current can flow in both directions to and from the legs. The electronic switches can be either power MOSFETs or IGBTs.

Current MOSFET and IGBT manufacturing technologies have allowed digital controllers to take advantage of Pulse-Width Modulation (PWM) techniques to control the amount of energy applied to each coil.

The most common techniques used are sinusoidal modulation, third-harmonic modulation and Space Vector Modulation (SVM). These PWM techniques are suitable to operate the electronic switches in saturation mode, which helps to increase system efficiency.

In order to determine the amount of current flowing through the coils, a shunt resistor is required on each coil. A typical three-phase inverter with current measurement on three phases is shown in Figure 2.





Assuming there is a balanced load, we can consider that the sum of the three phases is equal to zero, as described by Kirchhoff's Current Law. This law is shown in Equation 1.

#### EQUATION 1: KIRCHHOFF'S CURRENT LAW

$$IA + IB + IC = 0$$

Therefore, by measuring only two, the third can be solved using Equation 1. A simplified version using two shunt resistors is shown in Figure 3.

#### FIGURE 3: CIRCUIT FOR MEASURING CURRENT IN TWO PHASES



The intention of the algorithm presented in this application note is to be able to measure all three phases with a single-shunt resistor and a single differential amplifier. A circuit showing a single-shunt resistor is shown in Figure 4.



#### CIRCUIT FOR MEASURING CURRENT FLOWING THROUGH DC BUS



# ADVANTAGES AND DISADVANTAGES OF USING A SINGLE-SHUNT RESISTOR

#### **Advantages**

As previously mentioned, one of most important reasons for single-shunt three-phase reconstruction is cost reduction. Which in turn, simplifies the sampling circuit to one shunt resistor and one differential amplifier.

In addition to cost reduction benefits, the single-shunt algorithm allows the use of power modules that do not provide individual ground connection of each phase.

Another benefit of single-shunt measurement is that the same circuit is being used to sense all three phases. Gains and offset will be the same for all measurements, which eliminates the need to calibrate each phase amplification circuit or compensate in software.

## Disadvantages

During single-shunt measurements, a modification on the sinusoidal-modulation pattern needs to be made in order to allow current to be measured. This pattern modification could generate some current ripple. Due to modification of patterns and correction of the same modifications, more CPU is used to implement this algorithm.

# IMPLEMENTATION DETAILS

In order to drive the motor with AC signals, PWM methods are used to drive the switching transistors shown in the three-phase inverter. This modulation and resulting modulated waveform are shown in Figure 5.

A sinusoidal waveform can be generated by loading a series of duty cycle values into the PWM generator module. The values in the lookup table represent a modulated sine wave, so once these duty cycles are fed into the motor windings through the inverter, the motor windings will filter the switching pattern. The resulting sine wave is shown Figure 5.

The downside of a lookup table with sine values is the maximum value that can be achieved. This value is limited to 86% of the input voltage. Another sinusoidal modulation method is Space Vector Modulation, which is used to overcome this limitation. SVM allows 100% utilization of input voltage. SVM is described and used in several application notes such as AN908 *"Using the dsPIC30F for Vector Control of an ACIM"* and AN1017 *"Sinusoidal Control of PMSM Motors with dsPIC30F DSC"*. The typical voltage shape generated using SVM is shown in Figure 6.







When calculating the resulting voltage from line-to-line, we get three sinusoidal waveforms phase shifted  $120^{\circ}$ , as shown in Figure 7.





# SVM and Current Measurement Relationship

When measuring current through a single-shunt resistor, the state of the bottom switches is critical. To show this, Sector I of SVM is magnified in Figure 8. In addition, PWM waveforms on each switching transistor are also shown.

To observe the relationship between PWM modulation and current measurement through a single-shunt resistor, let us consider PWM Cycle 2 as an example. Since we are only interested in the low-side switch PWM, we will only show the PWMxL components of the PWM (Figure 9).



# FIGURE 8: PWM SIGNALS ON SWITCHING TRANSISTORS IN SECTOR I





Looking at the three-phase inverter, we will analyze all of the different PWMxL combinations (T0, T1, T2 and T3) for this period to see what the current measurement represents. Starting with T0, we have the following combination of the electronic switches (MOSFETs or IGBTs) in the inverter, where we see that there is no current flowing through the single-shunt resistor (Figure 10).

#### FIGURE 10: NO CURRENT FLOWING THROUGH THE SHUNT RESISTOR



Moving on to T1, we see that PWM2L is active, while PWM1H and PWM3H are active as well (not currently shown, but assuming PWM outputs are complementary). Since there is current flowing into the motor through phases A and C, and coming out of phase B, we can consider this current measurement to represent –IB, as shown in Figure 11.

#### FIGURE 11: CURRENT IB FLOWING THROUGH THE SHUNT RESISTOR



During T2, PWM2L and PWM3L are active, and PWM1H is active. This combination gives us current IA flowing through the single-shunt as shown in Figure 12.

#### FIGURE 12: CURRENT IA FLOWING THROUGH THE SHUNT RESISTOR



T3 is the same scenario as T0, where there is no current flowing through the shunt resistor; therefore, IBUS = 0 as shown in Figure 13.





The pattern repeats the second half of the PWM period. Looking at a complete PWM cycle, there are two windows of time where current represents an actual phase current. In this example –IB and IA were measured in one PWM cycle. Since this is a balanced system, IC can be calculated using Equation 2. This allows three current measurements to be done in one PWM cycle using a single-shunt resistor.

# EQUATION 2: IC CALCULATION

IC = -IB - IA

A truth table (Table 1) was created to help illustrate what the measured current represents for all possible combinations of the electronic switches. First, let us name each electronic switch as shown in Figure 14.





Table 1 shows what IBUS represents for all eight possible combinations of the circuit. Keep in mind that the H and L switches from the same leg cannot be ON at the same time to avoid shoot-through, so these combinations are not listed in the table. Also, any other combination that does not allow any current flowing through the shunt resistor is not listed in Table 1.

TABLE 1: SHUNT RESISTOR TRUTH TABLE

IH	2H	3H	1L	2L	3L	IBUS
ON	OFF	OFF	OFF	ON	ON	+IA
OFF	ON	OFF	ON	OFF	ON	+lB
OFF	OFF	ON	ON	ON	OFF	+lc
OFF	ON	ON	ON	OFF	OFF	-la
ON	OFF	ON	OFF	ON	OFF	–lb
ON	ON	OFF	OFF	OFF	ON	–IC

#### FIGURE 15: SAMPLING TIME WINDOW FOR SIMILAR DUTY CYCLES



#### Special Cases

There are special situations that do not allow singleshunt three-phase reconstruction.

# DUTY CYCLES ARE SIMILAR OR EQUAL DURING HIGH-MODULATION INDEX

As sinusoidal waveforms are generated with SVM, there are some PWM periods in which time windows where current is sampled, are simply not wide enough. One example of this situation is PWM cycle 1, which is shown in Figure 8. If we zoom in, we notice that PWM1L and PWM3L are the same, which leads to a T2 of '0'. Figure 15 shows a magnification of this condition.

This situation does not allow the controller to measure a second current. Therefore, three-phase current information cannot be constructed for that particular cycle.

#### DUTY CYCLE SIMILARITY DURING LOW-MODULATION INDEX

Low-modulation index means that the amplitude of the modulating signal is low, as opposed to a highmodulation index where the duty cycle can go all the way to 100% due to a high-amplitude of the modulating signal. Low-modulation index is usually done when there is no load on the motor shaft. Therefore, the amplitude of the modulating signal is low. Since Complementary mode is used to modulate sinusoidal voltages, duty cycles are centered in 50% duty cycle. If we take the same sector as before, but for a lowmodulation index, we will end up with a situation similar to what is shown in Figure 16. We can see how close the duty cycles are to 50% duty cycle. In fact, a modulation index of '0' would be generating by 50%, duty cycles on all PWM outputs.

Let us take a closer look at PWM cycle 4 to see what the limitation is when using a single-shunt resistor to reconstruct the three phases as shown in Figure 17.

The two windows used to measure current through single-shunt, T1 and T2, may be too narrow to let the differential amplifier stabilize its output to a steady state value.

## FIGURE 16: SIMILAR DUTY CYCLES DURING LOW-MODULATION INDEX



#### FIGURE 17: SAMPLING TIME WINDOW FOR SIMILAR DUTY CYCLES DURING LOW-MODULATION INDEX



#### DEAD TIME

Additionally, dead time is also present during Complementary mode, reducing these time windows even further. Showing the same PWM cycle with high side outputs and dead time, we end up with a situation similar to what is shown Figure 18.



#### FIGURE 18: SAMPLING TIME WINDOW AFFECTED BY DEAD TIME

Dead time also affects the time window where singleshunt current measurements are done. The minimum time window to measure current through single-shunt depends on the following parameters:

• PWM Frequency:

This is because the higher the PWM frequency is, the smaller all of these time window values are.

• Dead Time Required by the System:

As shown in the previous figure, dead time directly affects the measurement window.

Hardware:

Differential amplifier slew rate, output filter delay and MOSFET switching noise affect this measurement window as well.

#### HARDWARE

In order to illustrate how the hardware affects the single-shunt measurement, let us take a closer look at the first half of the period of the last PWM cycle (Figure 18) to see what the output of the actual single-shunt conditioning circuitry (shown in Figure 19) looks like.

FIGURE 19: HA ME US

HARDWARE UTILIZED FOR MEASURING CURRENT USING A SINGLE-SHUNT RESISTOR



The effective measurement window is reduced to whenever the output of the amplifier is stable, which means after MOSFET switching noise, dead time, the operation amplifier's slew rate, and the output RC filter settling time. These effects are shown in Figure 20.

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Zooming in to the transient response of the amplifier (shown in Figure 21), the green box shows where it is okay to sample at T1. However, since T2 is not wide enough, current cannot be sampled during T2. The transient response in gray represents the time to sample T2 if it would have been wide enough.

#### FIGURE 21: MAGNIFICATION OF THE HARDWARE EFFECTS ON THE SAMPLING TIME WINDOW



In general, single-shunt reconstruction of three-phase currents is not possible when modulating the shaded areas from the hexagon shown in Figure 22.

FIGURE 22: CRITICAL SVM VECTOR AREAS TO RECONSTRUCT THREE-PHASE CURRENTS USING A SINGLE-SHUNT RESISTOR



The shaded areas represent the low-modulation index region, and sections of mid-to-high modulation index when transitioning from sector to sector.

For additional details on SVM, refer to the following application notes:

- AN908 "Using the dsPIC30F for Vector Control of an ACIM"
- AN955 "VF Control of 3-Phase Induction Motor Using Space Vector Modulation"
- AN1017 "Sinusoidal Control of PMSM Motors with dsPIC30F DSC"
- AN1078 "Sensorless Field Oriented Control of PMSM Motors"

If current reconstruction is done without any modification of the SVM pattern, that is, ignoring the fact that during some periods current cannot be reconstructed, the resulting three-phase current measurement are shown in Figure 23. The SVM voltages are shown in Figure 24.





FIGURE 24: SPACE VECTOR MODULATION VOLTAGES

We can see how current measurement is quite noisy during critical periods.

# Possible Techniques to Overcome These Problems

- One possible solution to this problem is to ignore current measurements during these critical periods. This is not desirable since some algorithms, including the one used in this application note, require information from all three currents in order to estimate the position of the rotor.
- Another solution is to estimate current measurements. This could be one good solution, but requires fine tuning since current increase would depend on pass current measurement, motor parameters, and so on.
- The third solution is to expand the period of time where measurement is taking place. This would force a minimum time (critical measuring time) so that current stabilizes to a new value that is actually measurable by the Analog-to-Digital Converter (ADC).

We will focus on modifying the switching pattern to a minimum measurement time window (TCRIT), which is present all of the time.

# MODIFYING SVM PATTERNS TO ALLOW CURRENT RECONSTRUCTION

The method proposed in this application note is simple and it can be easily implemented in a dsPIC DSC. This case is shown in Figure 25, where T2 is not wide enough to measure single-shunt current.

In order to allow a minimum time window for current measurement, we modify this time. The new PWM timing diagram is shown in Figure 26.

The modification of the SVM pattern allows a minimum time to sample current through the single-shunt, which then allows three-phase reconstruction using the single-shunt.

When this is done, we notice how timing has changed, and also that the effective duty cycle during one PWM period is changed. This would introduce an error on voltage generation, since we are adding a delta to the modulation. Software and control loops running inside the dsPIC DSC would think that the output of the controller was set to duty cycles, but in fact a different value is applied to the PWM due to these modifications.

## FIGURE 25: CASE WHEN SAMPLING WINDOW IS NOT WIDE ENOUGH







Another task is then needed to compensate for any modifications we made to the duty cycles to allow the minimum window. The proposed solution corrects the duty cycles during the next half period of the same PWM cycle. If we refer to the last example, the final duty cycle is shown in Figure 27, where compensation is made on the second half of the period.

On PWM2L we see what the original PWM signal looks like in light gray. We also show the modified and compensated PWM signal in black. There is a simple rule this algorithm follows. Whatever is added to the first half of the PWM cycle, is subtracted on the second half, just as was shown in the previous figure. One important point is that current measurements are done during the first half of the PWM period, so not having enough window to measure current during the second half is irrelevant.

To illustrate where the currents are measured in the last example, we show a time diagram with current sampling points. Figure 28 shows the sampling points.

The single-shunt reconstruction algorithm consists of calculating what the modification should be according to the current SVM state and also consists of a state machine that executes all of these operations.









For comparison purposes, Figure 29 shows a timing diagram of events when two shunt measurements are available without the need of modifying SVM patterns.

During event A, all control loops are executed. Since there is no reconstruction needed, there is no need to change the ADC trigger point. This is also an advantage of having multiple sample-and-holds in the dsPIC DSC so that up to four signals can be sampled at the same time. During event B of the dual-shunt algorithm, two current measurements are taken, since all three low side switches are conducting. The only limitation of dualshunt measurement when this topology is available is the minimum duty cycle in which the low side switches are conducting.

The timing diagram where a series of events are shown in Figure 30, provides more details on how the singleshunt reconstruction algorithm is implemented in comparison with dual-shunt.



#### FIGURE 29: TIMING DIAGRAM OF EVENTS FOR DUAL-SHUNT ALGORITHM





For simplicity, let us consider the four consecutive PWM cycles as previously shown. A series of operations and events happen every single cycle. We have divided these events into four, represented with the letters A through D.

Let us start with event C. This event happens after the second conversion of the ADC takes place. The Analog-to-Digital (A/D) interrupt is triggered and an Interrupt Service Routine (ISR) is fetched. When the single-shunt state machine is in this state, both currents are already buffered and ready for processing. Before returning from this interrupt, the duty cycle (previously enlarged to allow current measurement) is then compensated in the duty cycle registers. The PWM module will take these new compensated duty cycles and make them effective after the first half of the period, since the PWM is configured for double update mode.

Event D is triggered by the PWM interrupt. By the time this interrupt is fetched, the PWM module has already loaded into the duty cycle registers what was previously written based on duty cycle compensation. Since there are two current measurements already saved, a third current is then calculated in this event. All other tasks are also performed in this event, such as FOC, position estimation, speed control and so on. In the case of this application note, Sensorless FOC for PMSM is implemented along with the single-shunt reconstruction algorithm. All of the sensorless algorithm is executed here in event D.

A time constraint to consider is that whatever the algorithm or operations needed to be executed in event D, a maximum execution time of the PWM period divided by 2 is allowed. This is because the result of all control loops and operations done during this period are written back to the PWM module, which will reload duty cycle values as soon as a new PWM period starts.

After control loops and operations are executed, new SVM output is calculated in event D. Then, these new values are analyzed by the single-shunt algorithm to see if SVM pattern modification is needed for the next PWM cycle. If correction is needed, additional duty cycle is added to the resulting SVM output, which takes effect as soon as a new cycle is started. The last thing done in event D is to configure the Special Event Trigger register on the ADC to enable the first current measurement on the next PWM cycle. This makes sure that during the next PWM cycle, current measurements are taken during a valid measurement window.

Event A is initiated by a PWM interrupt at the beginning of the PWM cycle. All corresponding duty-cycle adjustments done in a previous PWM cycle take effect in this event. The first A/D sample is also configured into the Special Event Trigger mode register (SEVTCMP) during Event A.

Event B is triggered by the A/D as a result of the first conversion. The value is saved, and a second trigger point is set in the SEVTCMP register.

The critical time window and the dead time influence the value assigned to SEVTCMP. The SEVTCMP register value at event A is calculated when the PWM is counting down. There is a unique SEVTCMP value for each SVM sector. The average value of PDC1, PDC2 and PDC3 is used to calculate the next ADC triggering point. This average value is right shifted one position in order to match the size of the SEVTCMP register (15 bits) and the PDCx registers (16 bits). Hence, the next SEVTCMP value is equal to the sum of the PDCx registers divided by 4 plus the dead time. As shown in Equations 3 through 8.

## EQUATION 3: SECTOR 1

$SEVTCMP A = \frac{(PDC1 + PDC3)}{4} + Dead Time$	
$SEVTCMP B = \frac{(PDC1 + PDC2)}{4} + Dead Time$	

## EQUATION 4: SECTOR 2

$SEVTCMP A = \frac{(PDC2 + PDC3)}{4} + Dead Time$	
$SEVTCMP B = \frac{(PDC1 + PDC3)}{4} + Dead Time$	

# EQUATION 5: SECTOR 3

SEVTCMP $A = \frac{(PDC2 + PDC3)}{4} + Dead$ Time	
$SEVTCMP B = \frac{(PDC1 + PDC2)}{4} + Dead Time$	

# EQUATION 6: SECTOR 4

$SEVTCMP A = \frac{(PDC1 + PDC2)}{4} + Dead Time$	е
$SEVTCMP B = \frac{(PDC2 + PDC3)}{4} + Dead Time$	е

# EQUATION 7: SECTOR 5

SEVTCMP $A = \frac{(PDC1 + PDC3)}{4} + Dead$ Time	
$SEVTCMP B = \frac{(PDC2 + PDC3)}{4} + Dead Time$	

# EQUATION 8: SECTOR 6

 $SEVTCMP A = \frac{(PDC1 + PDC2)}{4} + Dead Time$  $SEVTCMP B = \frac{(PDC1 + PDC3)}{4} + Dead Time$ 

Registers PDC1, PDC2 and PDC3 contain the actual PWM duty cycles calculated after the SVM pattern modification. The compensation is calculated twice during a PWM cycle. When the PWM counter is counting up, the TCRIT value is subtracted from the SVM pattern. This ensures that the correct PWM duty cycles are applied for the compensation occurring at the second half of the PWM cycle.

When the PWM counter is counting down, the TCRIT is added to the SVM pattern in order to ensure that the time window is wide enough for the next sampling events A and B. Equations 9 through 17 show the relationship between the SVM pattern modification and the TCRIT. These are the equations utilized for the compensation occurring at the second half of the PWM cycle.

### EQUATION 9: SVM PATTERN COMPENSATION REQUIRED AT TIME T1

SVM Pattern B = SVM Pattern C + T1 - (T1 - TCRIT)

#### EQUATION 10: SVM PATTERN COMPENSATION *NOT* REQUIRED AT TIME T1

SVM Pattern B = SVM Pattern C + T1

### EQUATION 11: SVM PATTERN COMPENSATION REQUIRED AT TIME T2

SVM Pattern A = SVM Pattern B + T2 + (T2 - TCRIT)

#### EQUATION 12: SVM PATTERN COMPENSATION NOT REQUIRED AT TIME T1

SVM Pattern A = SVM Pattern B + T2

These are the equations utilized for the compensation occurring at the first half of the PWM cycle.

#### EQUATION 13: WHEN T1 ≥ TCRIT

SVM Pattern B = SVM Pattern C + T1

### EQUATION 14: WHEN T1 ≥ TCRIT

SVM Pattern B = SVM Pattern C + T1

## EQUATION 15: WHEN T1 < TCRIT

*SVM Pattern B* = *SVM Pattern C* + *TCRIT* 

EQUATION 16: WHEN  $T2 \ge TCRIT$ 

SVM Pattern A = SVM Pattern B + T2

#### EQUATION 17: WHEN T2 < TCRIT

SVM Pattern A = SVM Pattern B + TCRIT

Figure 31 shows the relationship between TCRIT, the dead times, T1 and T2, and the results of these compensations.





# **PRACTICAL RESULTS**

After implementing three-phase reconstruction using a single-shunt resistor, the resulting current is shown in Figure 32.

If we zoom in and add the IBUS signal in orange, we get the results shown in Figure 33.



#### FIGURE 32: RECONSTRUCTED CURRENTS BASED ON THE SINGLE-SHUNT RESISTOR



SVM looks as follows for high-modulation index. It is possible to see the adjustments to SVM to allow the minimum measurement window, as illustrated in Figure 34.



FIGURE 34: SVM FOR HIGH-MODULATION INDEX

Figure 35 shows an actual waveform, displaying all PWM signals and the IBUS signal.

# FIGURE 35: ACTUAL PWM WAVEFORMS VERSUS IBUS



Figure 36 shows a magnified section of Figure 35. In this figure, a few key points are marked. Note that the ADC starts sampling within a valid sampling time window to allow current measurement. We also show a pin toggling when the ADC ISR is executed.



#### FIGURE 36: SAMPLING POINTS SHOW THE ACTUAL PWM AND IBUS WAVEFORMS

# CONCLUSION

This application note illustrates the advantages, limitations and constraints of the single-shunt algorithm.

The single-shunt algorithm method is able to recreate the current flowing through the motor phases using a single-shunt resistor to sense the current flowing through the DC bus. In order to obtain the information contained in the DC bus current, Space Vector Modulation is used.

SVM creates a series of sampling time windows that allows the observation of the current flowing through the motor phases. These time windows are classified and grouped in the shunt resistor truth table (Table 1). This truth table shows the relationship between the information present at the shunt resistor versus the state of the electronic switches.

However, it is not possible to obtain the desired information from the DC bus current in certain SVM areas. This limitation is overcome by modifying the SVM switching patterns. Modifying these patterns makes it possible to extract the desired information from the single-shunt resistor in every SVM operating state.

These practical results demonstrate that the singleshunt resistor technique provides information accurate enough to meet the requirements of Field-Oriented Control. It is possible to obtain the motor information such as position and torque based on the reconstructed information extracted from the current flowing through the DC bus.

# REFERENCES

The following application notes, which are available for download from the Microchip website (www.microchip.com) were referenced in this application note:

- AN908 "Using the dsPIC30F for Vector Control of an ACIM" (DS00908)
- AN955 "VF Control of 3-Phase Induction Motor Using Space Vector Modulation" (DS00955)
- AN1017 "Sinusoidal Control of PMSM Motors with dsPIC30F DSC" (DS01017)
- AN1078 "Sensorless Field Oriented Control of PMSM Motors" (DS01078)

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