AN1269

Using C30 Compiler to Interface Serial SRAM Devices to dsPIC33F and PIC24F

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INTRODUCTION

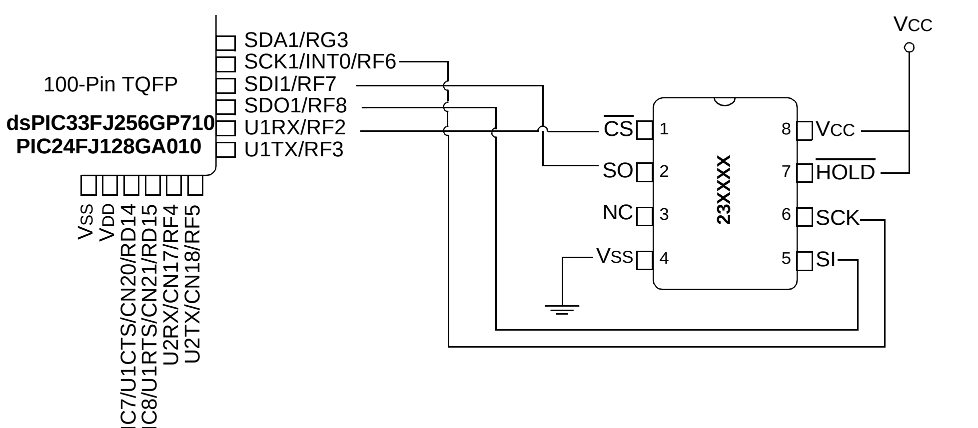
Microchip's serial SRAM product line represents a new way to add additional RAM to an application. With the small, 8-pin packages and the SPI interface these devices give designers added system flexibility. The 23XXXX series of serial SRAM devices from Microchip Technology support a half-duplex protocol that functions on a master-slave paradigm that is ideally suited to data stream applications.

The bus is controlled by the microcontroller (master), which accesses the 23XXXX using the SPI peripheral built into the MCU. The SPI bus can operate at speeds up to 20 MHz for enhanced throughput. Communications can be paused using the $\overline{HOLD}$ pin.

This application note is part of a series that provide source code to help the user implement the protocol with minimal effort.

Figure 1 describes the hardware schematic for the interface between Microchip's 23XXXX series devices and the dsPIC33F DSC or the PIC24F MCU. The schematic shows the connections necessary between either controller and the serial SRAM as tested, and the software was written assuming these connections. The $\overline{HOLD}$ pin is tied to VCC because this feature is not used in the examples provided.

FIGURE 1: CIRCUIT FOR dsPIC33FJ256GP710, PIC24FJ128GA010 AND 23XXXX SERIES DEVICE



Note: $\overline{CS}$ and $\overline{HOLD}$ pins should all have pull-up resistors (~10k-ohms). See recommended usage application note.

FIRMWARE DESCRIPTION

The purpose of this application note is to offer the designer a set of examples for the read and write functions for using the Microchip SPI Serial SRAM. Examples are included for the following modes: Byte, Page and sequential Read and Writes. The code uses the on-chip SPI hardware peripheral to communicate with the serial SRAM.

The code was tested using the 23K256 SRAM mounted to one of the SPI PIM modules. The code is compatible with the PIC24F, PIC24H and dsPIC33F families of MCU.

Oscilloscope screen shots are shown in this application note. The MCU was configured to use the crystal on the Explorer 16 board, the internal PLL was enabled and the SPI peripheral was configured to generate a serial clock rate of 4 MHz.

The following functions are provided to access the serial SRAM:

- `SRAMWriteStatusReg`
- `SRAMReadStatusReg`
- `SRAMWriteByte`
- `SRAMReadByte`
- `SRAMWritePage`
- `SRAMReadPage`
- `SRAMWriteSeq`
- `SRAMReadSeq`

INITIALIZATION

Only one function needs to be called to initialize the SRAM. Using the on-chip SPI peripheral makes communication easier than bit-banging the I/O ports. The `InitSRAM()` function initializes the SPI module and configures the I/O ports. Some devices support Peripheral Pin Select feature (PPS) and the SPI peripheral is one peripheral that is remappable. If the MCU that you are using supports this feature, additional steps must be taken to map the SCK, SDI and SDO pins accordingly.

WRITE STATUS REGISTER

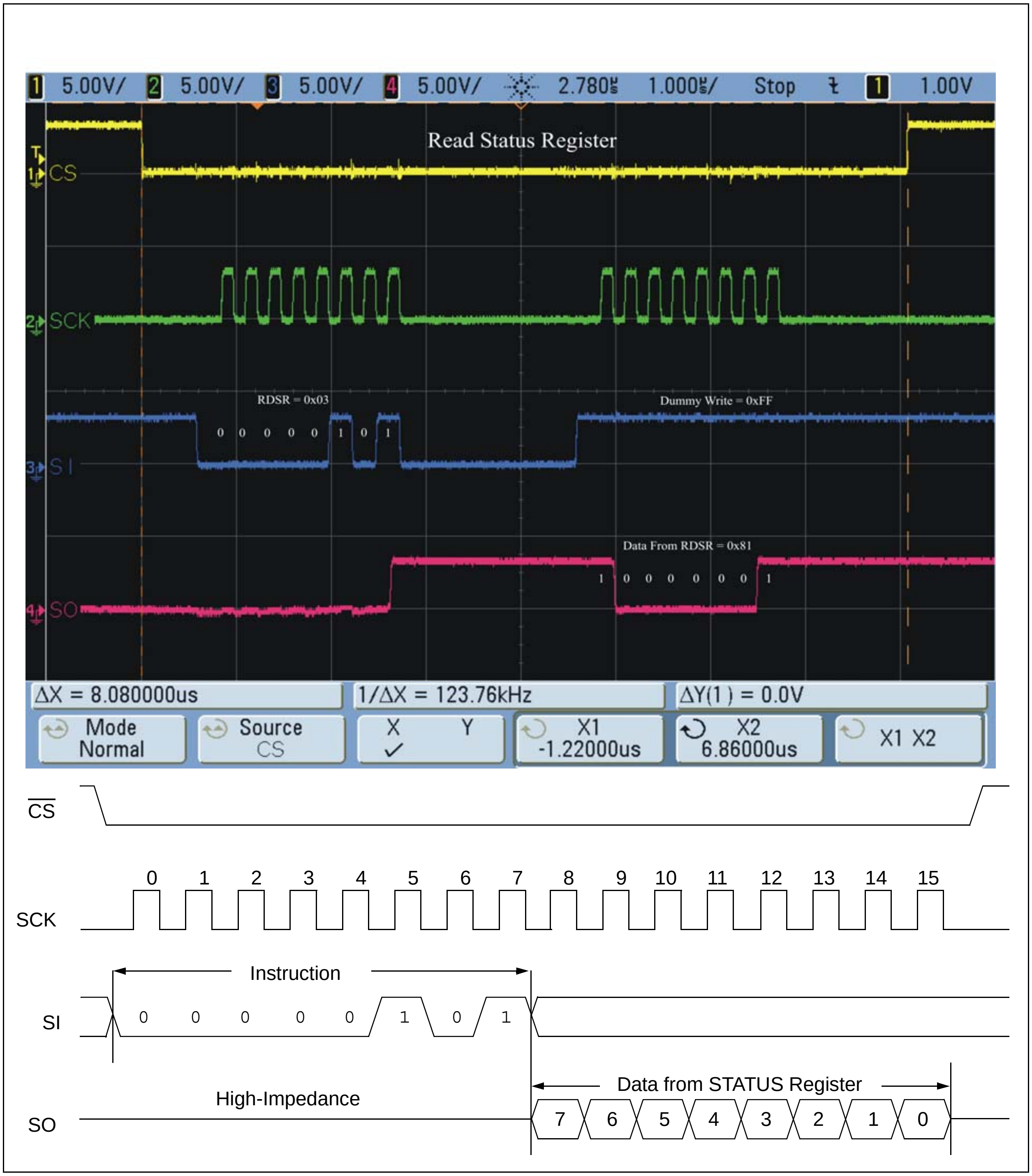
The default mode of operation for the serial SRAM is Byte mode and the user must select the appropriate mode before the read or write operation. The functions that are provided configure the SRAM for the correct mode of operation, for example, if a `SRAMWritePage` command is called, then the appropriate operating mode is selected. The STATUS register also has provision for enabling the HOLD feature, but this is not used in these examples. Figure 2 shows an example of the Write Status Register command. Chip Select is brought low (active) and the opcode is sent out through the SPI port. The Write Status command is given followed by the data to be written, in this case Page mode is selected.

FIGURE 2: WRITE STATUS REGISTER

READ STATUS REGISTER

Figure 3 shows an example of the Read Status Register command to check for the mode of operation and also the current status of the HOLD function.

FIGURE 3: READ STATUS REGISTER

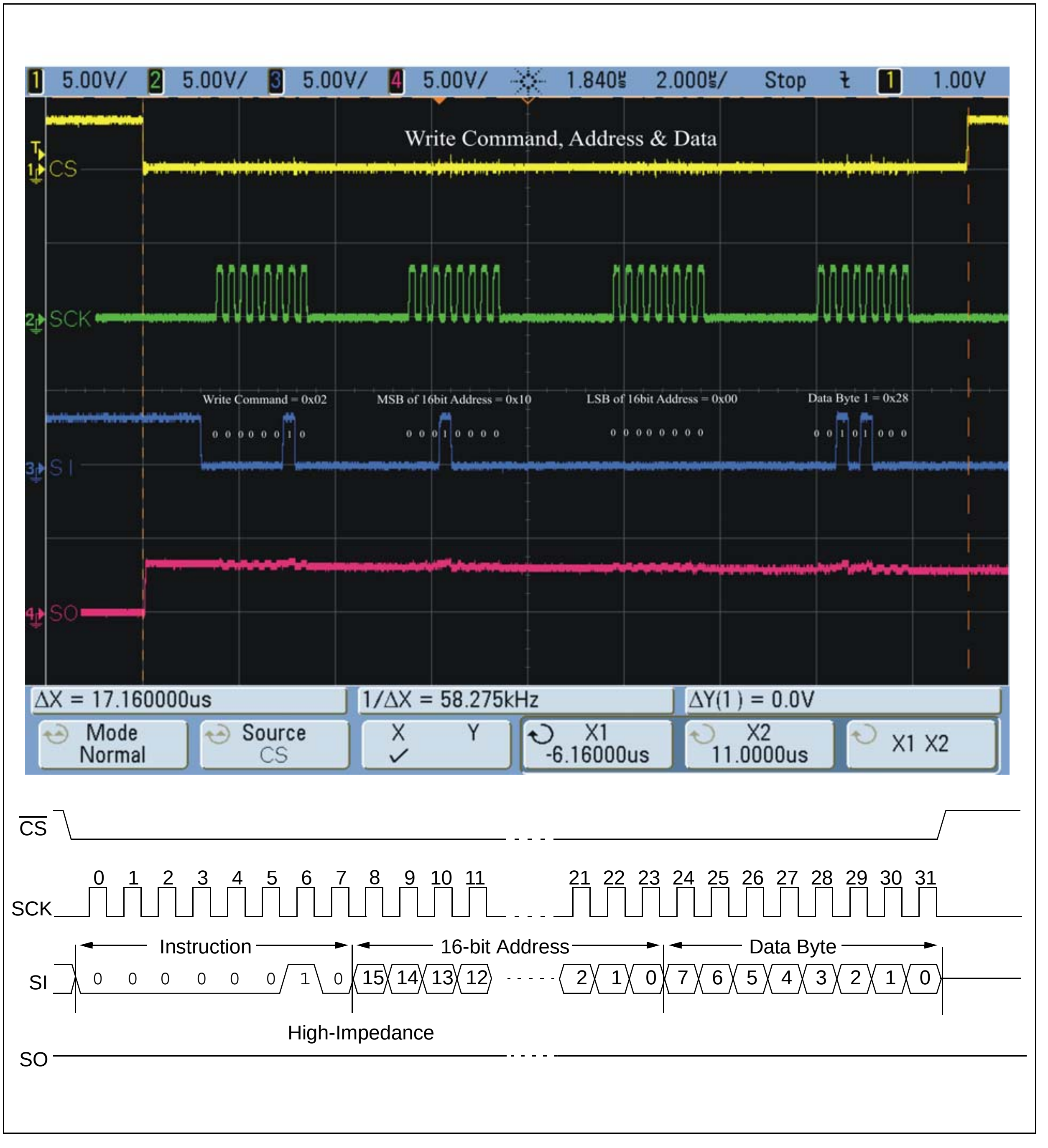


BYTE WRITE

The byte write operation consists of the following sequence: The Write command followed by the word address and data byte. The serial SRAM uses a 16-bit address, so two bytes must be transmitted for the entire word address, with the Most Significant Byte (MSB) first.

Figure 4 shows an example of the Write command. For this, the device is selected and the opcode, 0x02, is sent. The High Address byte is given 0x00, followed by the Low Address byte, 0x10. Finally, the data is clocked in last, in this case, 0x28.

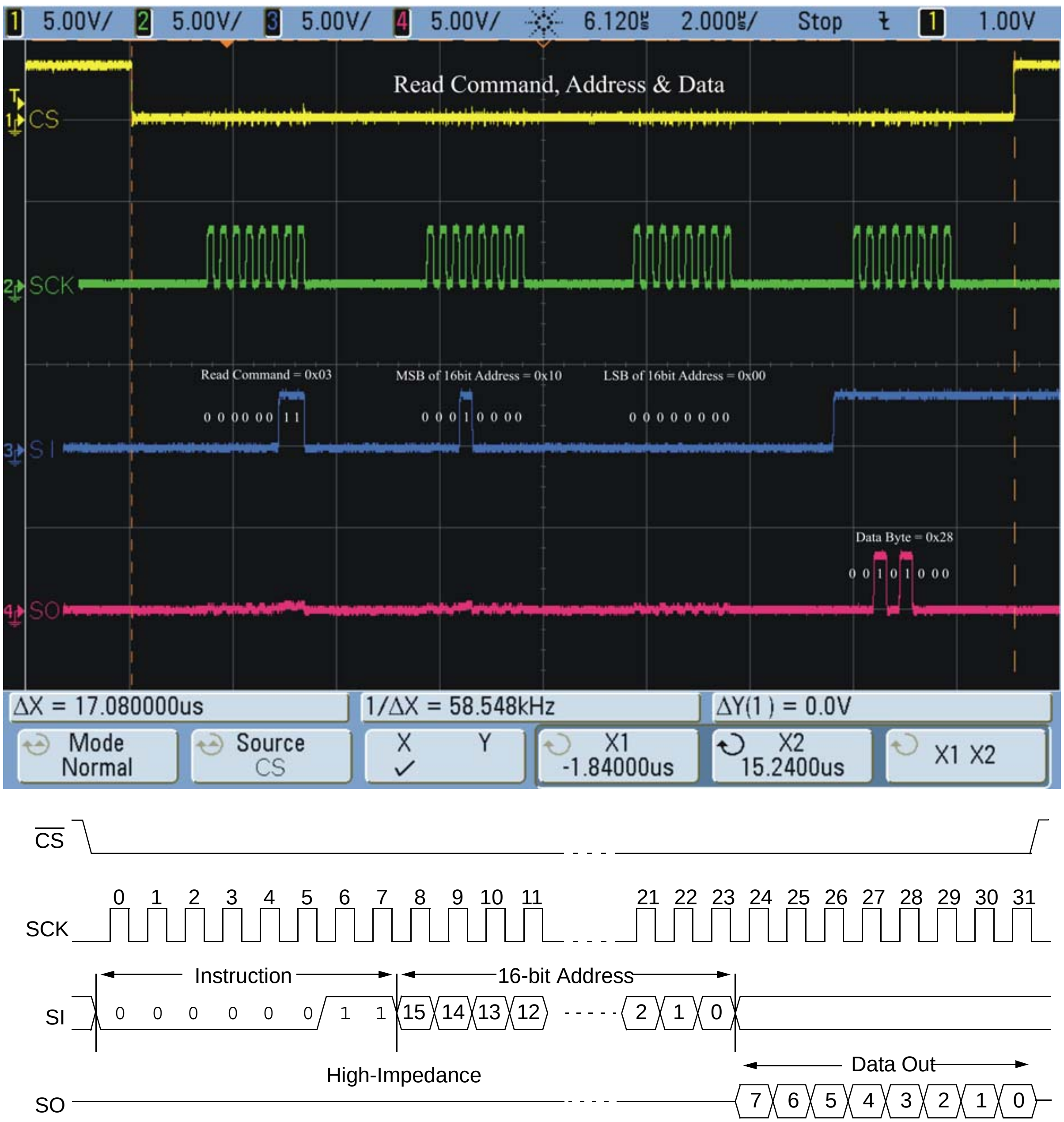
FIGURE 4: BYTE WRITE COMMAND, ADDRESS AND DATA



BYTE READ

The byte read operation can be used to read data from the serial SRAM. The MCU/DSC sends the command byte followed by the word address. Figure 5 shows an example of the Read command, followed by the MSB and LSB address bytes, followed by the read byte.

FIGURE 5: BYTE READ (COMMAND BYTE, WORD ADDRESS AND READ BYTE)



PAGE WRITE

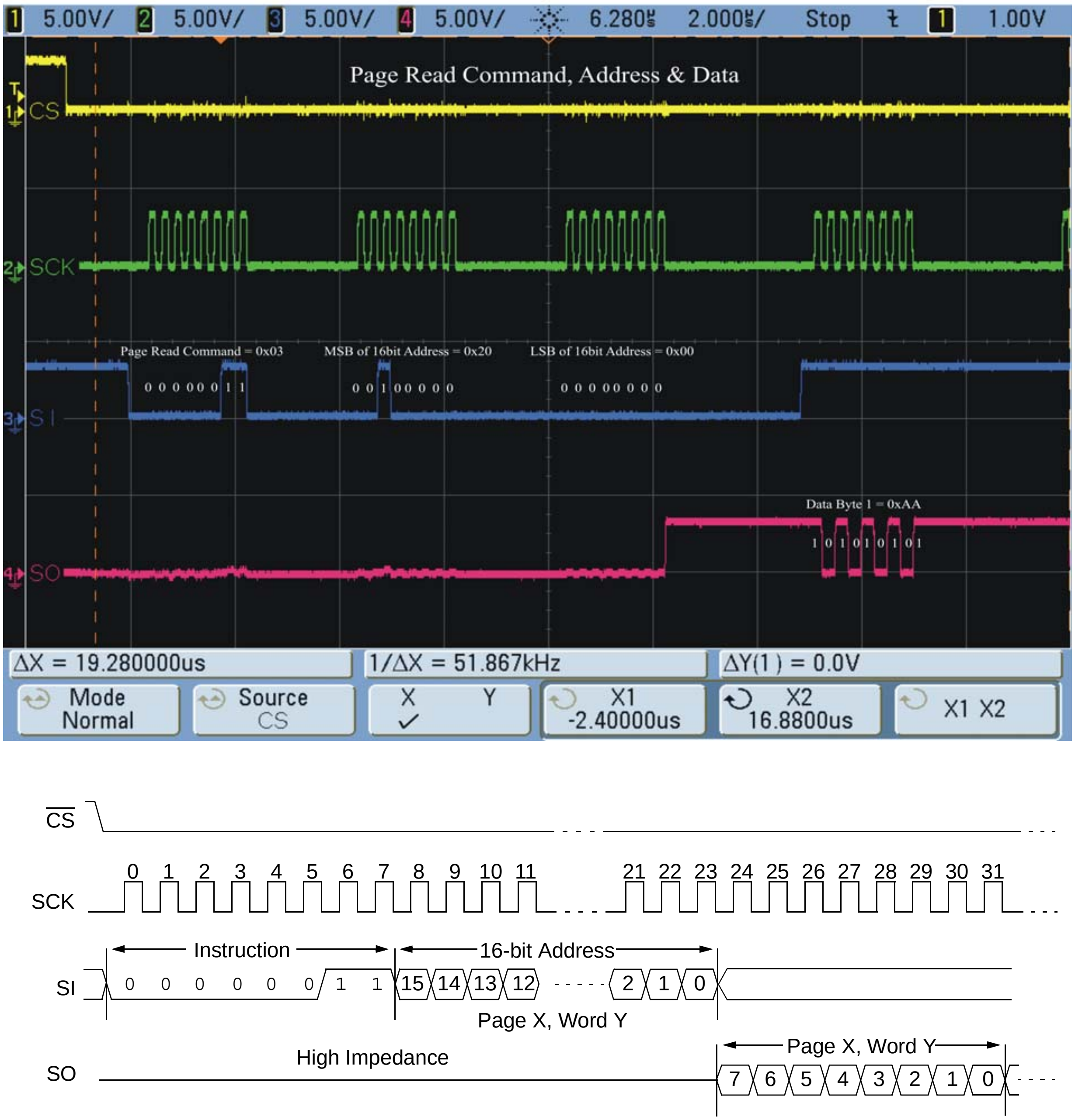
Page write operations provide a technique for increasing throughput when writing large blocks of data. The serial SRAM features a 32-byte page. By using the page write feature, up to 1 full page of data can be written consecutively. It is important to point out that page write operations are limited to writing bytes within a single physical page regardless of the number of bytes being written. Physical page boundaries start at addresses that are integer multiples of the page size and end at addresses that are [integer multiples of the page size] - 1. Attempting to write across a page boundary results in the data being wrapped back to the beginning of the current page. Figure 6 shows the Write command, address and data byte during a page write operation.

FIGURE 6: PAGE WRITE (FIRST DATA BYTE)

PAGE READ

Page read operations read a complete string, starting with the specified address. The page read operation also works similar to page write operation and thus a maximum of 32 bytes can be read consecutively. Figure 7 shows an example of the entire sequence of commands necessary to perform the page read operation. For clarity, only the first byte is shown.

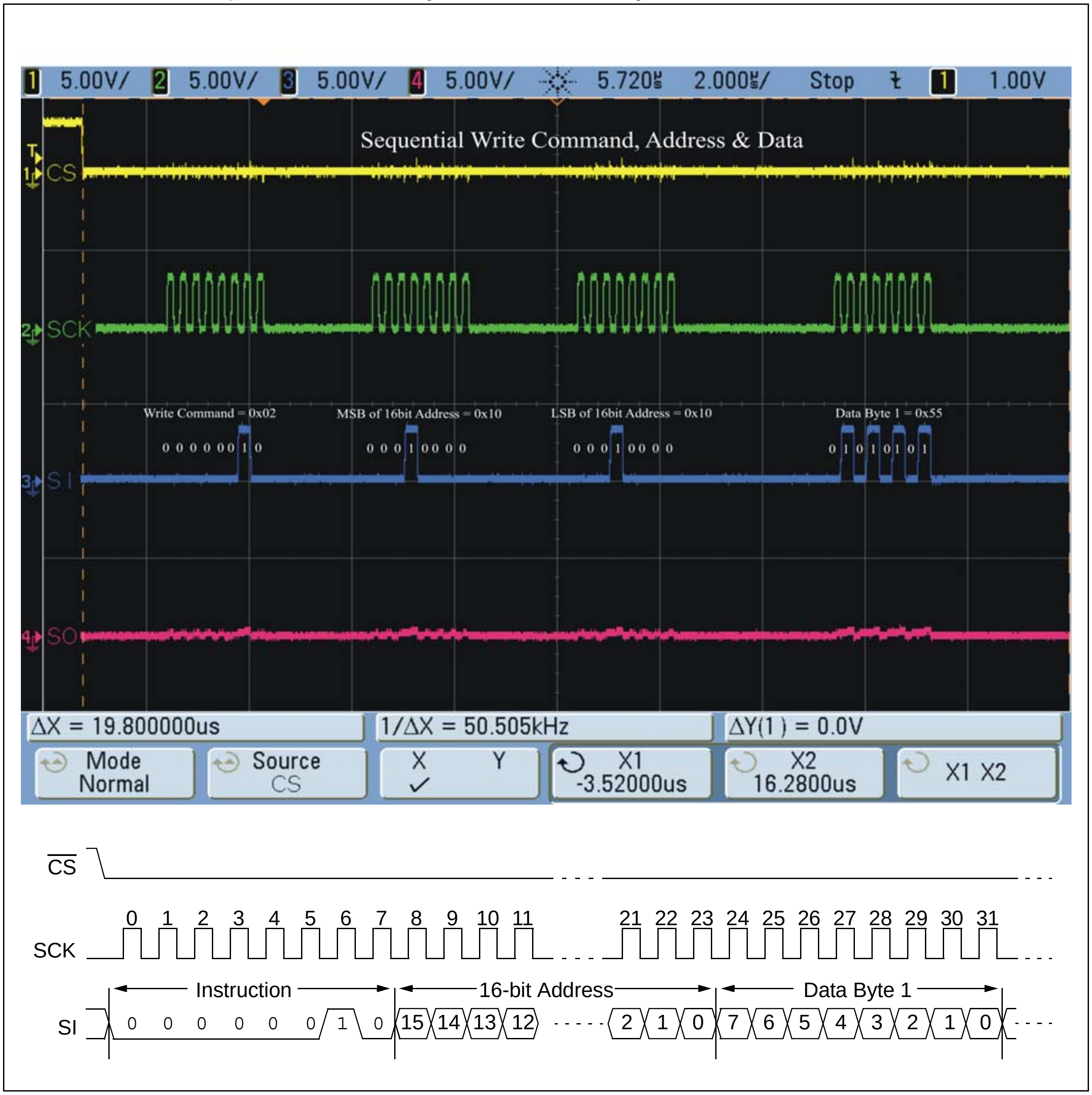
FIGURE 7: PAGE READ (FIRST READ DATA BYTE)



SEQUENTIAL WRITE

This operation is very useful while writing a long string, which is more than the page size (32 bytes). This operation needs a Write command (0x02) to be sent followed by upper address byte and lower address byte. The SRAM keeps writing data as long as it receives clock and valid data. When the last location of memory is reached, the next location that is written is the first address (0x0000), that is, the internal address counter rolls over. Figure 8 depicts the entire sequence of commands necessary to perform the sequential write operation. For clarity, only the first byte is shown.

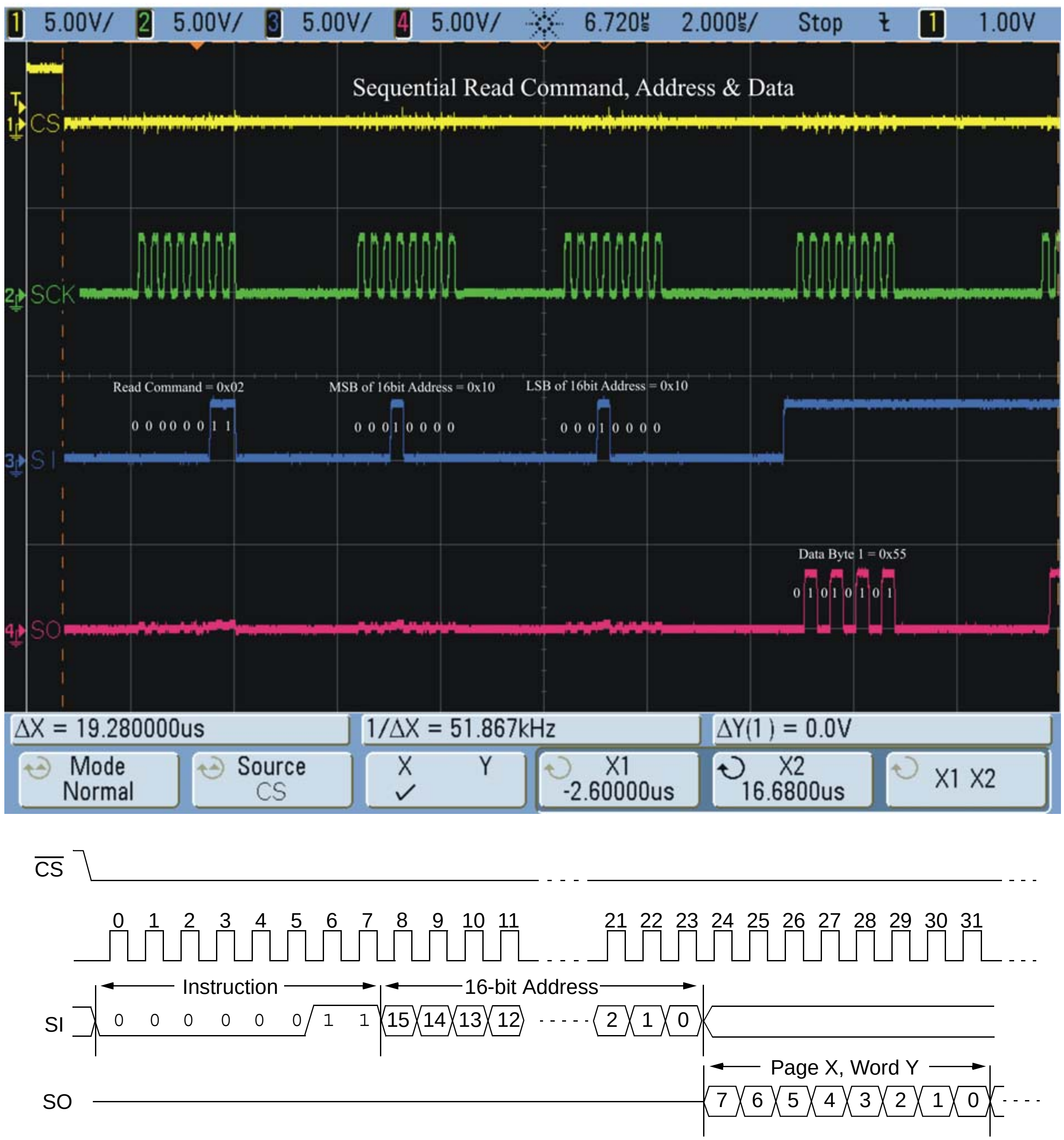
FIGURE 8: SEQUENTIAL WRITE (FIRST DATA BYTE)



SEQUENTIAL READ

Sequential read operation allows the entire array to be read from the SRAM. The internal address counter automatically increments and page boundaries are ignored. When the internal address counter reaches the end of the array, the address counter will roll over to 0x0000. Figure 9 shows an example of the sequence of commands necessary to perform a sequential write operation.

FIGURE 9: SEQUENTIAL READ (FIRST READ DATA BYTE)



CONCLUSION

This application note offers designers a set of firmware routines to access SPI serial SRAM. The code demonstrates byte, page and sequential operations. All the routines were written in C using the C30 package from Microchip. The code was tested on Microchip's Explorer 16 Development Board with the connections shown in Figure 1 with the PIC24FJ128GA010 PIM module.

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