# AN1252

# Interfacing the MRF49XA Transceiver to PIC® Microcontrollers

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## INTRODUCTION

Microchip Technology's MRF49XA is a highly integrated RF transceiver, used in the 433, 868 and 915 MHz frequency bands. The transceiver uses FSK modulation internally.

A transceiver is a device that can both transmit and receive. Thus, the word 'transceiver'. A system that can send *and* receive data at the same time is called a full-duplex system. On the other hand, a system that can only send *or* receive at a time is called a half-duplex system. Thus, half-duplex systems use only one frequency carrier and the two ends share the same frequency. Full-duplex systems use two carrier frequencies, known as uplink frequency and downlink frequency.

This document discusses what is required to successfully develop a half-duplex radio application using the Microchip Technology MRF49XA transceiver. For more information on this transceiver, please refer to the MRF49XA data sheet (DS70590).

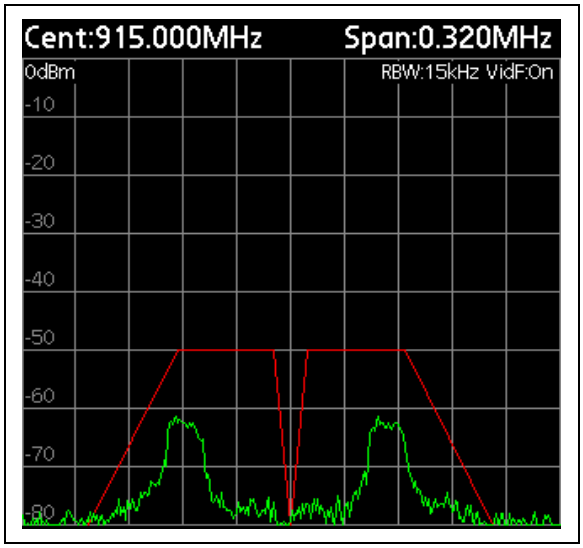
## FSK SHORT THEORY

The most common radio modulation used in Remote Keyless Entry (RKE) systems is the Amplitude Shift Keying (ASK). Data is transmitted by varying the amplitude of a fixed-frequency carrier. When data is encoded as maximum amplitude for a '1' or mark, and zero amplitude – the power amplifier (PA) is switched off – for a '0' or space, this type of modulation is also named On-Off Keying, or OOK. This modulation format allows very simple and low-cost transmitter designs.

Another type of modulation is Frequency Shift Keying (FSK). This is done by shifting the carrier's frequency on either side of an average (or carrier) frequency. The amount by which the carrier shifts on either side of the carrier's frequency is known as deviation. The FSK modulation has several advantages over the ASK modulation. While the AM modulation is very sensitive to variations of amplitude and noise, the FSK encoded transmissions are more immune to signal attenuation or other amplitude-based disturbance. Although the apparent bandwidth is from $f_0 - \Delta f$ to $f_0 + \Delta f$, in reality, the bandwidth spreads larger than the span between $f_0 - \Delta f$ to $f_0 + \Delta f$, because the speed of transition between the two frequencies generates additional spectral content.

In short, think of FSK modulation as a more reliable transmission medium having much less noise. In order to achieve a successful design, you will need a deeper understanding of the requirements of an FSK modulated radio link.

**FIGURE 1: THE COMBINED SPECTRUM GENERATED BY A '01010...' PATTERN**




To see an example of what FSK looks like, take a look at Figures 1 through 3. These plots are taken from a spectrum analyzer, a tool that plots amplitude (in dB) versus frequency (linearly, in Hz). Each of the plots has about an 80 dB range, with a frequency range or "span" of 320 kHz (since there are 10 divisions, this is 32 kHz per division).

The plot is "centered" at 915 MHz. This means perfectly aligned between the left and right side of the plot, at 915 MHz. Left of this point is the lower frequency and to the right is the higher frequency (at 32 kHz per division).

Figure 1 shows what the frequency plot looks like for our example design when its transmitter generates a continually alternating stream of ones and zeros (a 01010101… pattern). The green line is from the spectrum analyzer and shows two peaks. Since FSK means shifting the frequency based on the symbol sent (a '1' or a '0'), there are two peaks.

The red line represents the baseband filter response of the receiver, discussed later in this document. In this design, the receiver portion needs the green line to fit inside of each area between the red lines. As you can see, each green peak is reasonably centered under each area, showing that the transceiver performance should function correctly. We will show mismatch examples later.

**FIGURE 2: THE SPECTRUM GENERATED BY A '0' SYMBOL**

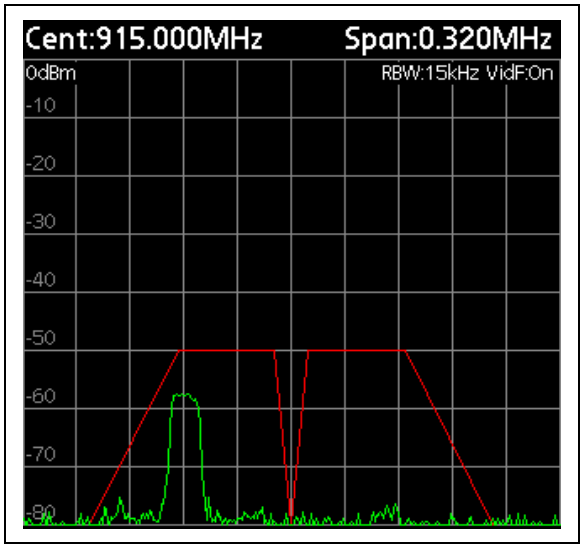



Figure 2 shows what the output looks like when only a '0' is transmitted. Note that only one peak is shown, the lower frequency peak exists only in this example.

**FIGURE 3: THE SPECTRUM GENERATED BY A '1' SYMBOL**

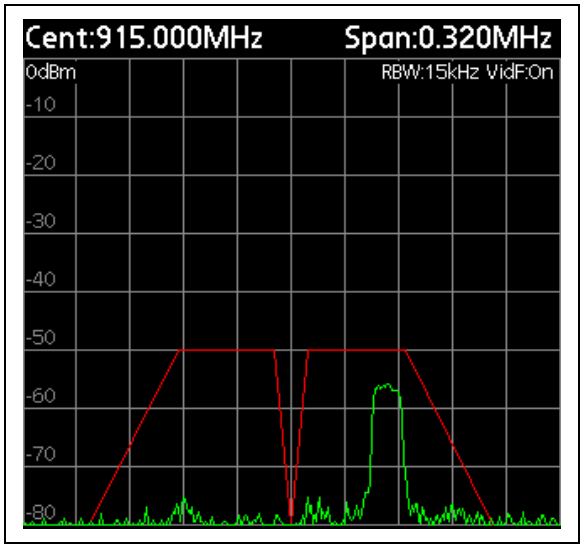



Figure 3 shows the result of just transmitting a '1' symbol, which has only the higher frequency peak as expected.

## CONTROL INTERFACE

MRF49XA uses a 4-line SPI interface to communicate with the host microcontroller/system. These lines are SDO, SDI, CLK and $\overline{CS}$. The SPI port is used for the control interface and for sending data to and from the 16-bit data TX register/RX FIFO (if the TXDEN/FIFOEN bit is enabled in the General Configuration register).

In order to use a MRF49XA radio device, it has to be initialized first. Initializing the device is done by writing commands to the internal register through the control interface. There are 16 control (commands) and one Status Read register. The explanation of these registers can be read from the MRF49XA data sheet.

Commands to the transceiver are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the Chip Select pin, $\overline{CS}$, is low. When the $\overline{CS}$ signal is high, it initializes the serial interface. All registers consist of a command code, followed by a varying number of parameters or data bits. All data are sent, MSB first (e.g., bit 15 for a 16-bit register). On a Power-on-Reset, the circuit sets the default values for all the registers.

The transceiver will generate an interrupt request to the host microcontroller by pulling the $\overline{IRO}$ line low if one of the following events takes place:

- TX register is ready to receive the next byte
- RX FIFO has received the pre-programmed amount of bits
- FIFO overflow/TX register underrun (TXUROW overflow in Receive mode and underrun in Transmit mode)
- Negative pulse on interrupt input pin, $\overline{INT}$
- Wake-up timer time-out
- Supply voltage below the pre-programmed value is detected
- Power-on Reset

After receiving an interrupt request, the host microcontroller identifies the source of the interrupt by reading the Status bits.

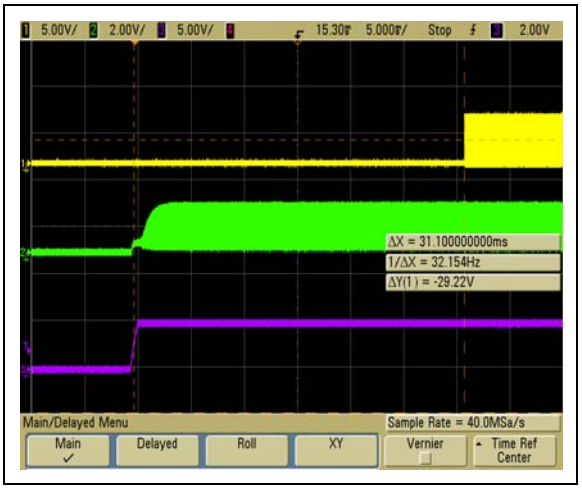
## DEVICE INITIALIZATION

The device features a Power-on-Reset circuit, which has a time-out of 100 ms. During this time, the oscillator should have enough time to start the oscillations and reach a point of stability.

In Figure 4, signal 1 (yellow) is the CLK output (1 MHz), signal 2 (green) is the waveform at the crystal output and signal 3 (violet) is $V_{DD}$. This oscilloscope print indicates that, after applying the $V_{DD}$ voltage to the device, it takes 31.1 ms for the crystal to start oscillating and stabilize and for the digital circuitry to begin operation. SPI commands sent before the POR

time-out are ignored. Thus, after power-up, a delay of at least 100 ms should be provided. Alternatively, the host can pool the RESET line.

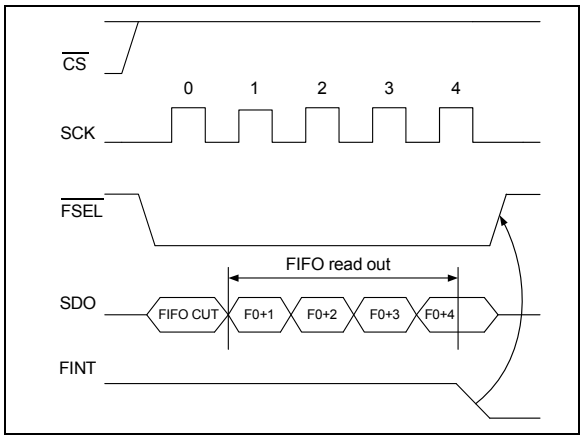
**FIGURE 4: DEVICE INITIALIZATION**




## BUFFERED DATA RECEIVE

If the receive FIFO is enabled, the received data is clocked into the 16-bit buffer. The receiver starts to fill the FIFO when the synchronization pattern circuit has detected a valid data packet. This prevents the FIFO from being loaded by random data. When the FIFO has reached a predefined level of loading, then a signal is present on the FINT pin (pin 7 on the device, active-high). A logic level '1' on this pin means that the number of bits in the RX FIFO has reached the pre-programmed limit. The level at which the RF device will generate an interrupt can be set by means of the FIFO and the Reset Mode Configuration register. This value is typically set to 8 bits (one byte) to allow a byte-by-byte loading of the FIFO during the transmit/receive process. This is true only in FIFO mode, when bit FIFOEN is set in the General Configuration register. An SPI buffer read will cause the RX FIFO to reach a lower number of bits, and the FINT pin to go back to the logic level zero. When the FSEL line is low, the FIFO output is connected to the SDO pin and its content can be clocked out.

**FIGURE 5: BUFFERED MODE**




In addition to the Buffered mode, the MRF49XA device can be used in a Non-Buffered mode in which pin 6 (FSK/DATA/FSEL) is the TX data input pin in Transmit mode, while, in Receive mode, it is the RX data output. Pin 7 (RCLKOUT/FCAP/FINT) is the RX data clock output.

## BUFFERED DATA TRANSMIT

In this mode, data is clocked into one of the two 8-bit data registers forming a 16-bit register. The transmitter starts to send data into the air from the first register as soon as the TXCEN bit is set with the in the Power Management Configuration register. These two registers contain an initial value of 0xAA and this value can be used to generate a preamble to a data packet. During the transmitting process, the SDO pin must be monitored (SDO goes high) if the data register is ready to receive another byte from the host microcontroller.

| | |
|---|---|
| **Note:** | The user must pay attention when using these registers as, at the initial state, these registers already contain data. Also, the transmitter should not be turned off before the last byte in the register has been sent. To meet this requirement, the last byte loaded to the FIFO is a dummy byte to allow the last byte to be sent. At the next SDO pin rise (FIFO ready for the new byte), the transmitter can be turned off. |

## RADIO LINK REQUIREMENTS

For an FSK modulated radio link there is a set of a few basic parameters to describe the link itself:

- Data rate
- Deviation
- RX baseband bandwidth
- Crystal accuracy (frequency reference)

### Data Rate

Depending on the application, it can be a low-speed or a high-speed radio link. Low-speed is typically used in applications where only short data packages need to be sent with very long delays between transmissions (hours to days). High-speed is used only when the device needs to send large amounts of data, such as in radio modems, digital audio links, etc. A low data rate will allow a longer range for the radio link due to less noise in the receiver demodulation circuit. On the other hand, a high-speed link can also be used to provide a much shorter data packet and, thus, a longer battery life (if powered by any).

### Deviation

To calculate the recommended deviation, you need to know the data rate and the crystal accuracy. As a rule of thumb, the deviation must be bigger than the data rate. Then, you must also provide some space for the RX to TX frequency offset (which is tunable and is discussed later in the document). The minimum recommended deviation is 30 kHz.

### RX Baseband Bandwidth

This is defined by the crystal accuracy and by the range requirement. The longer the needed range, the smaller the baseband bandwidth (in order to filter the noise).

### Crystal Accuracy

Use a low ppm accuracy crystal. A better accuracy of the crystal allows for less TX to RX offset, smaller deviation, and baseband bandwidth. A good crystal should have a ppm value of ≤ 40 ppm.

**Note:** The ppm value of a crystal defines its accuracy. It stands for parts-per-million. The lower the ppm value, the better the crystal accuracy. The frequency error generated by a crystal can be calculated with the following formula:

$$\Delta f_0 = ppm\_value * \frac{f_0}{10^6}$$

Where $f_o$ is the crystal nominal frequency.

## EXAMPLE CALCULATION

Data rate 9.6 kbps, crystal accuracy 40 ppm, 915 MHz band. What are the deviation and baseband bandwidth?

**EQUATION 1:**

$$\Delta f_0 = \frac{40ppm}{10^6} * 915 * 10^6 = 36.6kHz$$

**EQUATION 2:**

$$Deviation = data\_rate + 2*\Delta f_0 + 10 * 10^3\ Hz =$$
$$= 9600 + 2*36600 + 10 * 10^3\ Hz = 92.800\ kHz$$

Hence, according to the standard frequency consideration, the closest deviation possible is 90 kHz.

**EQUATION 3:**

$$Baseband\ BW = deviation*2 – 10 * 10^3\ Hz =$$
$$= (90*2 – 10)* 10^3\ Hz = 170\ kHz$$

The closest possible baseband BW is 200 kHz.

## FREQUENCY OFFSET

In a radio link, the transmitter and the receiver are working on the same frequency. Only one device can transmit at one time and the other must receive.

Once the transmission is done, they can change roles and send back data (i.e., send back an acknowledgement).

Even if the two ends are, theoretically, using the same frequency, in practice there will be a finite frequency offset. The RX-TX frequency offset can be caused by differences in the reference frequency. This is generated by the crystal oscillator. To minimize this frequency error, it is recommended to use the same type of crystal on both sides of the radio link and, as much as possible, the same PCB layout for the crystal reference section.

To determine the actual RX-TX offset, the use of a high-precision frequency counter is recommended. To measure the oscillator frequency, connect the measuring probe to the CLKOUT (pin 8) of both the RX and TX units. Do not connect the probe directly to the crystal pin, as the probe itself has an internal capacitance and the measurement process will modify the reference frequency. The CLKOUT of the device gives a frequency divided by a default value of ten (it can be programmed to other values) from the reference oscillator frequency. To disable CLKOUT, set the CLKOEN bit from the Power Management Configuration register.

The actual frequency can be calculated using the formula below:

**EQUATION 4:**

For 915 MHz:

$$F_{ref} = (Frequency[Mhz]) * 91.5$$

For 868 MHz:

$$F_{ref} = (Frequency[Mhz]) * 86.8$$

For 433 MHz:

$$F_{ref} = (Frequency[Mhz]) * 43.3$$

A 30 ppm, 10 MHz crystal will generate a maximum error of:

**EQUATION 5:**

$$\Delta f_0 = \frac{CrystalAccuracy[ppm]}{10^6} * XtalFrequency[MHz] * 10^6$$

$$= \frac{30}{10^6} * 10 * 10^6 = 300Hz$$

Thus, a maximum frequency error of:

**EQUATION 6:**

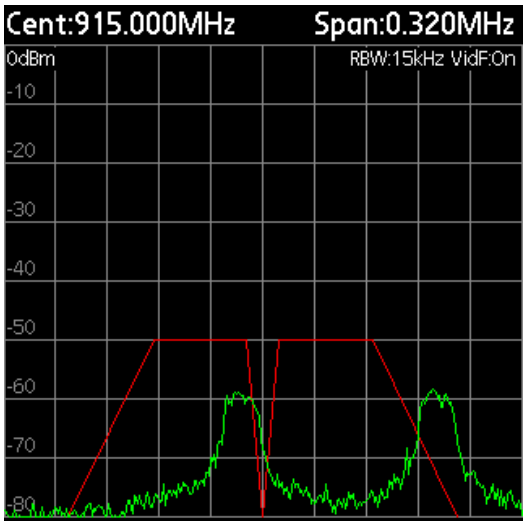
$$F_0 = \frac{Frequency[Mhz]}{10} * \left(XtalFrequency[MHz] * 10^6 \pm \Delta f_0\right)$$

$$= 915\ MHz \pm 27.45KHz$$

Where the TransmissionBand is 868 or 915, depending on the frequency setting.

Adjusting the RX-TX frequency offset can be done using the General Configuration register and changing the crystal load capacitance. This allows small changes in the reference frequency. Adjust the crystal load capacitance in order to get the same frequency on both devices – as close as possible.

**FIGURE 6: EXAMPLE OF BADLY TUNED TRANSMITTER**




In Figure 6, we have the example of a badly tuned transmitter. Here we see that the center frequency is misaligned. The red lines represent the receiver baseband filter response. As you can clearly see, a radio link cannot be established in this case, since the receiver cannot interpret the '1' and the '0' symbols. The amplitudes of the signals are not of interest here and are shown only for illustration purposes.

## CONCLUSION

MRF49XA is a highly integrated RF transceiver. It requires only a few external components and can be controlled via an SPI interface.

Thus, MRF49XA is ideal for low-power, short-range radio communications, where the host system is a microcontroller, such as Microchip's PIC® microcontrollers.

## FAQS

Q1: I cannot establish a radio communication. The two modules (TX and RX) work only if they are placed very close to each other (a few inches).

A1: Using a frequency counter, check the clock output from the MRF49XA CLKOUT (pin 8). Align the reference frequency as close as possible (using the General Configuration register) on both ends of the radio link. Do not place the probe on the RFXTAL pad, as the probe also has some internal capacitance and the measurement process will shift the actual frequency.

Q2: Transmission only works in one direction. Reception works in both directions.

A2: This is most likely a hardware malfunction. Try to establish a radio link with another identical unit. For example, a base station talking to another base station and/or a remote key fob talking to another key fob. The antenna needs a middle connection to the $V_{DD}$ line. Check if this is present.

Q3: What are the minimum test/measurement tools that I need in order to develop a system like the one described here?

A3: You shouldn't need any special RF tool to get it working. If it still doesn't work, go through this document again.

## APPENDIX A: SOURCE CODE

Due to size considerations, the complete source code for this application note is not included in the text. A complete version of the source code, with all required support files, is available for download as a Zip archive from the Microchip web site at:

www.microchip.com

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