Powering a UNI/O$^{®}$ Bus Device Through SCIO

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INTRODUCTION

As embedded systems become smaller, a growing need exists to minimize I/O pin usage for communication between devices. Microchip has addressed this need by developing the UNI/O$^{®}$ bus, a low-cost, easy-to-implement solution requiring only a single I/O pin for communication.

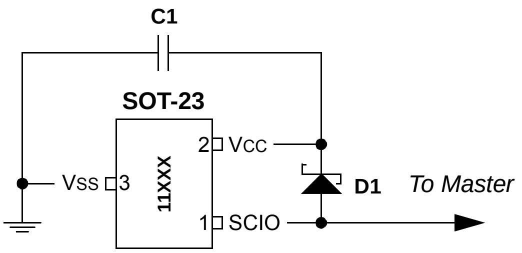
The standard configuration for a UNI/O bus combines the serial clock, data, address, and control signals onto the SCIO signal. This allows UNI/O devices to enhance any application facing restrictions on available I/O stemming from connectors, board space, or the master device. But some applications can benefit from a further reduction in connections.

This application note describes how a standard half-wave rectifier and capacitor circuit can be added to allow power to be extracted parasitically from the SCIO signal. Guidance is offered for selecting the capacitor value and diode based on application parameters such as voltage and serial frequency. No modifications to the standard UNI/O bus protocol are necessary. It is assumed that the reader is already familiar with the basic terms and operation of the UNI/O bus.

Within this application note, equations shown with a heavy outline around them are critical equations used to calculate an important parameter. The other equations are provided to show the steps necessary in deriving the final equations.

Figure 1 shows the half-wave rectifier and capacitor circuit connected to a UNI/O serial EEPROM.

FIGURE 1: CIRCUIT FOR EXTRACTING POWER FROM SCIO



DESCRIPTION OF OPERATION

The circuit shown in Figure 1 allows power to be extracted from SCIO by storing energy on the capacitor, C1. This energy can then be used to power the UNI/O slave during times when the master is not driving the bus.

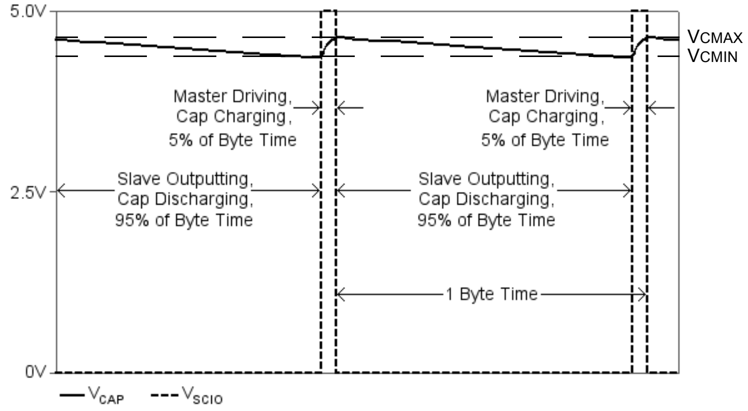
When the master drives SCIO high, the diode, D1, becomes forward-biased and allows current to flow through to the UNI/O slave, as well as to charge the capacitor. Charge will continue to build until the capacitor's voltage equals the master's high output voltage minus the voltage drop across the diode.

When the master drives SCIO low, the diode becomes reverse-biased and prevents the capacitor from discharging back through SCIO. In this situation, as well as when the slave is driving SCIO, the capacitor will discharge by powering the slave directly.

Because the UNI/O bus uses Manchester encoding, a high signal on SCIO must occur every bit. But since the capacitor can only be charged by the master, the worst-case situation is when reading data from the slave. This effectively results in a square wave input into the rectifier circuit with a pulse width of 4-6%, depending on input jitter. This is because the master will only be driving SCIO high during 40-60% of 1 in every 10 bits. Note that this is a very short period of time, and so it is critical that the proper components are selected to ensure correct operation.

Figure 2 shows an example of how the capacitor cyclically charges and discharges every byte during a read operation, assuming a constant current consumption by the slave. The solid line is the voltage on the capacitor, and the dotted line represents the voltage on SCIO when the master is driving, which only occurs during the MAK bit for a read operation.

FIGURE 2: EXAMPLE CAPACITOR CHARGING AND DISCHARGING DURING READ



SELECTING THE RIGHT DIODE

Due to their low forward voltage drop and fast reverse recovery, it is recommended that a Schottky diode be used. But even after limiting to only Schottky diodes, there are still many different ones from which to choose. When selecting a diode, the following parameters should be considered:

- Reverse Leakage Current (I_R)
- Reverse Recovery Time (T_{RR})
- Reverse Voltage (V_R)
- Forward Current (I_F)
- Forward Voltage (V_F)

Reverse Leakage Current (I_R)

Although Schottky diodes generally have higher reverse leakage currents than their P-N junction counterparts, this parameter can typically be considered negligible for the purposes of this application note. Even leakage currents around 10 µA will not significantly affect the results of the calculations. However, minimizing leakage current when selecting a diode is still recommended.

Reverse Recovery Time (T_{RR})

Reverse recovery time is the amount of time necessary for a diode to change from forward bias to reverse bias. During this time, excess reverse current is allowed to flow backwards through the diode. For this application, this means the capacitor will discharge back through the diode during this time. However, for Schottky diodes, reverse recovery time is very fast, usually less than 15 ns. This typically results in a charge loss, during the reverse recovery time, of less than 1% compared to the loss experienced when the slave is outputting and so is considered negligible for the purposes of this application note.

Reverse Voltage (VR)

The selected diode should be able to withstand, at a minimum, a reverse voltage equal to 2*VCC of the master. This is for times when the capacitor is fully charged and the bus is driven low, and will provide adequate guardband to ensure the diode is not damaged by excess reverse voltage.

Forward Current (IF)

During both read and write operations, the capacitor is being discharged for more time each byte than it is being charged. Because of this, more current must flow on average into the capacitor during charge than is flowing on average out of the capacitor during discharge. Read operations are the worst-case, because the master only charges the capacitor during the high time of the MAK bit every byte. This means that a large amount of current must flow through the diode into the capacitor while it is being charged to account for the loss during discharge. It is very important that the selected diode is able to withstand this elevated level of current.

At the beginning of a new command, the capacitor will be charged nearly to VCC. However, within a command, the capacitor will begin to discharge until the system achieves a point of stability. This point is where the charge removed from the capacitor during discharge is equal to the charge added to the capacitor during charging. The charge loss during discharge is dependent upon the current being consumed, ICCR, by the slave device and so it follows that the charge gain during charging also depends on ICCR. The following equation shows how to calculate the charge current based on ICCR and the amount of time charging vs. discharging.

EQUATION 1: CAPACITOR CHARGING CURRENT

$$I_{CHG} = \frac{Q}{t_{CHG}}$$

$$I_{DCHG} = \frac{Q}{t_{DCHG}} = I_{CCR}$$

$$\Rightarrow I_{CHG} = I_{CCR} \cdot \frac{t_{DCHG}}{t_{CHG}}$$

The average current, ID, flowing through the diode during capacitor charge is the combination of the current flowing into the capacitor and the current flowing into the UNI/O slave. This current value can be calculated using Equation 2.

EQUATION 2: AVERAGE DIODE CURRENT DURING CHARGE

$$I_D = I_{CHG} + I_{CCR}$$

$$\boxed{\Rightarrow I_D = I_{CCR} \cdot \left(\frac{t_{DCHG}}{t_{CHG}} + 1\right)}$$

Forward Voltage (VF)

When the system achieves stability, the voltage on the capacitor will oscillate between VCMAX and VCMIN, as described in **Section "Description of Operation"**. The value of VCMAX can be determined by Equation 3, where VMOH is the high-level output voltage of the master device while sourcing the average diode current level, ID, calculated by Equation 2.

EQUATION 3: MAXIMUM CAP VOLTAGE

$$V_{CMAX} = V_{MOH} - V_F$$

VCMAX and VCMIN are the VCC values seen by the UNI/O slave. VCMIN must be above the minimum operating voltage of the slave device, and also high enough to ensure that the slave's high-level output voltage (VSOH) exceeds the master's high-level input voltage (VMIH).

The value of VCMIN depends on the chosen size of the capacitor as well as VCMAX, and is calculated in **Section "Sizing the Capacitor"**. Because of this dependency, VCMIN is affected by both the forward voltage drop across the diode and the capacitor value.

The absolute maximum ratings for the UNI/O slave specify that SCIO must not go above the slave's VCC by more than 1.0V. This means that the only requirement for forward voltage drop of the diode is that it is less than 1.0V, which is very easily met by Schottky diodes. However, since the forward voltage also affects the capacitor value, then the forward voltage should still be minimized as much as possible.

SIZING THE CAPACITOR

If the slave's high-level output voltage does not reach the master's high-level input voltage (VMIH), the master may not detect high levels correctly on SCIO.

Equation 4 is the standard equation for calculating current when charging or discharging a capacitor.

EQUATION 4: CAPACITOR CURRENT

$$i(t) = C\frac{dv(t)}{dt}$$

Applying Equation 3 and Equation 4 to discharging the capacitor yields Equation 5, which shows how to calculate VCMIN based on a particular capacitor value, C.

EQUATION 5: MINIMUM CAP VOLTAGE

$$I_{CCR} = C\frac{dv(t)}{t_{DCHG}}$$

$$\Rightarrow dv(t) = \frac{I_{CCR} \cdot t_{DCHG}}{C}$$

$$V_{CMAX} - V_{CMIN} = dv(t)$$

$$\Rightarrow V_{CMIN} = V_{CMAX} - \frac{I_{CCR} \cdot t_{DCHG}}{C}$$

$$\boxed{\Rightarrow V_{CMIN} = V_{MOH} - V_F - \frac{I_{CCR} \cdot t_{DCHG}}{C}}$$

Applying the requirement that VSOH be higher than VMIH to Equation 5 and solving for C yields the following equation:

EQUATION 6: MINIMUM CAP VALUE

$$V_{SOH} \geq V_{MIH}$$

$$\Rightarrow V_{CMIN} - 0.5V \geq V_{MIH}$$

$$\boxed{\Rightarrow C \geq \frac{I_{CCR} \cdot t_{DCHG}}{V_{MOH} - V_F - V_{MIH} - 0.5V}}$$

Note that the minimum capacitor value is directly proportional to the amount of time spent discharging, which is inversely proportional to the bus frequency. As the discharge time increases, the capacitor value must also increase. Therefore, operating at a faster bus frequency will actually allow for the use of a smaller capacitor.

Once the minimum capacitor value is calculated using Equation 6, VCMIN must be calculated using Equation 5 to ensure that it is above the minimum operating voltage of the UNI/O slave. If it is not, then a larger capacitor value must be used.

OTHER CONSIDERATIONS

Power-Up Timing

Before initiating any communication with the UNI/O slave, including the low-to-high edge to release the device from POR and the standby pulse, the capacitor must be charged to the minimum operating voltage of the slave. The amount of time necessary to charge the capacitor depends on the capacitor value and the impedance of the device performing the charging. If a pull-up resistor is being used to charge, Equation 7 can be used to calculate the amount of time necessary to charge the capacitor.

EQUATION 7: CAPACITOR CHARGING

$$V_{MIN} = V_{CC}(1 - e^{-t/(RC)})$$

$$\Rightarrow t = -(RC)\ln\left(1 - \frac{V_{MIN}}{V_{CC}}\right)$$

Alternatively, the master output driver can be used to charge the capacitor. This will typically offer a significantly faster charging time. However, the charging time is dependent upon the master output driver impedance which varies both by master device and output voltage. For this reason, it is much simpler to characterize the amount of time needed for the specific application by measuring the charge time using the final components. This measurement should be guardbanded to ensure a robust design.

Pull-Up Resistor

A pull-up resistor on SCIO is recommended for a standard UNI/O bus configuration. This is to ensure bus idle during times when the UNI/O slave is being powered but no device is driving the bus (for example, when the master is held in Reset). But when power is being extracted from SCIO parasitically, this condition will not occur and so is not a concern.

When the UNI/O slave is driving SCIO high, a path for current flow is created through the slave output driver to the slave's V_{CC} connection. If a pull-up resistor is used, then it will provide a small amount of current that flows through the output driver to help power the slave when the slave is driving high. This effectively raises V_{CMIN} since the capacitor is having to provide less current to power the slave. However, because the current through the pull-up is very small, it does not have a significant effect on the results of the calculations provided above.

The pull-up will also raise the slave's high-level output voltage by creating a voltage divider with the output driver. This results in additional guardband which will provide for a more robust design.

Because of the guardband provided, the use of a pull-up resistor is recommended, but not required. The pull-up value should be selected in the same manner as for standard UNI/O bus applications (20 KΩ is typical).

WIP Polling

The WIP polling feature offers a simple method of maximizing data throughput, but requires the consumption of additional current. During the write cycle, the write operating current (I_{CCW}) is drawn to operate the charge pump which allows data to be stored in the array. WIP polling adds the read operating current level to this, which results in a current draw higher than a normal read operation.

It is recommended that the master power the slave device during the write operation by driving SCIO high for the full write cycle time, T_{WC}. But if WIP polling is necessary, the procedures described previously for selecting the capacitor value and diode can be performed using the combined I_{CCR} + I_{CCW} current value. Otherwise, the serial EEPROM will likely lose power before the write cycle has completed, causing the data being written to be corrupted.

EXAMPLE CALCULATIONS

The following example shows how to use the equations described above to select the correct components. Table 1 lists the important parameters for the example.

TABLE 1: EXAMPLE PARAMETERS

Parameter	Value	Units
I_{CCR}	3.0	mA
T_{DCHG}	237.5[1]	µs
T_{CHG}	12.5[1]	µs
V_{MOH}	4.35	V
V_{MIH}	2.0	V
V_F	0.33[2]	V

Note 1: T_{DCHG} and T_{CHG} based on bus frequency of 40 kHz with no input jitter.

2: Based on diode selected after calculating I_D.

Note that V_F will vary depending on the selected diode, and V_{MOH} and V_{MIH} will vary depending on the master device.

For this example, Equation 2 yields an average diode current of 60 mA. Knowing this value allowed for the selection of the diode.

Applying the parameters to Equation 6 results in a minimum capacitor value of 0.469 µF. Also, Equation 5 yields a V_{CMIN} value of 2.50V, which is within the valid operating voltage range for UNI/O slave devices.

FIGURE 3: OSCILLOSCOPE PLOT OF EXAMPLE READ OPERATION

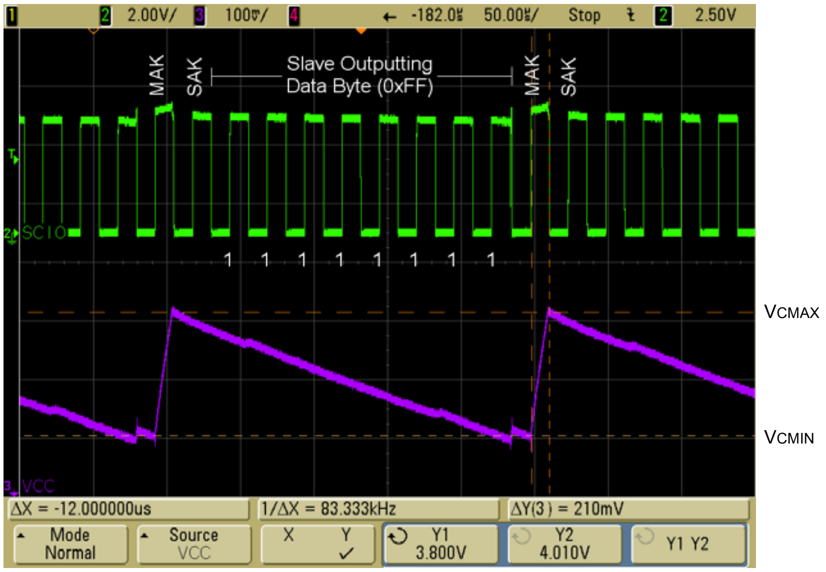


Figure 3 shows an oscilloscope plot in the middle of a read operation after VCC has reached its stable oscillating range. The cursors mark the second half of the MAK bit, while the master is charging the capacitor. The components used were selected as described above. Note that VCMIN is not as low as predicted by the equations. This is because the equations assume the UNI/O slave will consume the maximum specified current, ICCR, but the device consumed less than the maximum in this example.

SUMMARY

This application note offered details and examples of combining power and SCIO over a single connection for a UNI/O bus application. This provides for fewer required connections, leading to smaller and lower costing system designs. The procedures described require a small amount of additional effort over a standard UNI/O bus implementation, but following them will allow for a more robust design.

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