

Interfacing Baseline PIC[®] MCUs with UNI/O[®] Bus-Compatible Serial EEPROMs

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INTRODUCTION

As embedded systems become smaller, a growing need exists to minimize I/O pin usage for communication between devices. Microchip has addressed this need by developing the UNI/O[®] bus, a low-cost, easy-to-implement solution requiring only a single I/O pin for communication.

UNI/O bus-compatible devices can be used to enhance any application facing restrictions on available I/O. Such restrictions can potentially stem from connectors, board space or from the master device itself.

The 11XXX family is the newest addition to Microchip Technology's broad serial EEPROM product line and is compatible with the newly developed UNI/O bus.

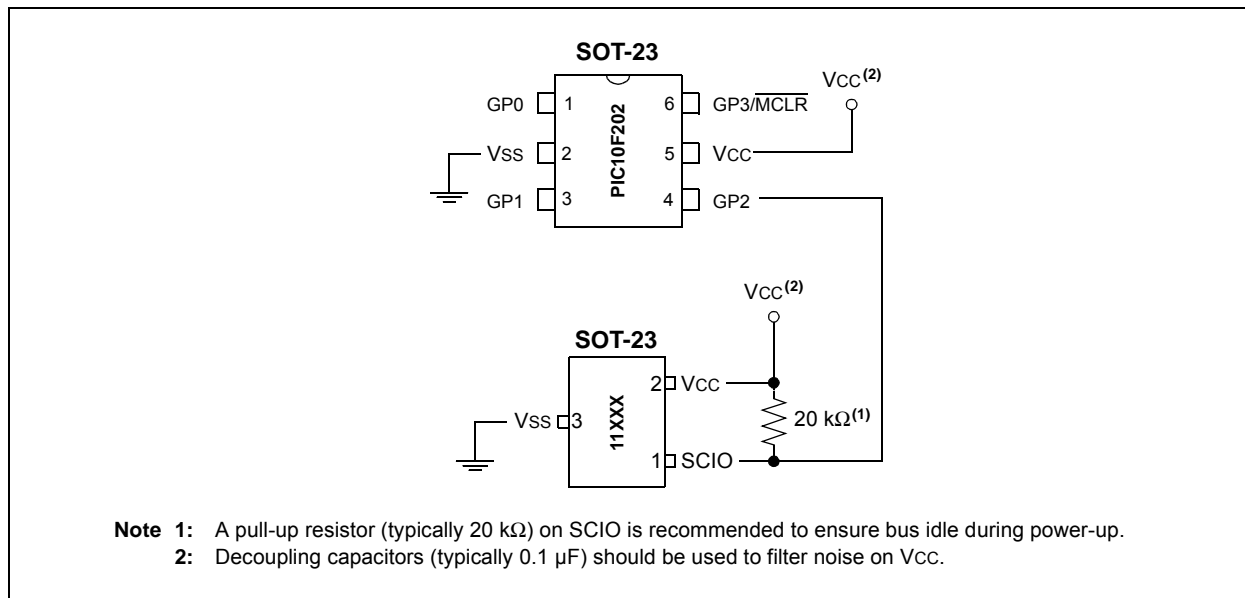
The main features of the 11XXX devices are:

- Single I/O pin used for communication
- EEPROM densities from 1 Kb to 16 Kb
- Extremely small packages
- Bus speed from 10 kHz to 100 kHz
- Voltage range from 1.8V to 5.5V
- Low-power operation
- Temperature range from -40°C to +125°C
- Over 1,000,000 erase/write cycles

This application note is part of a series that provide source code to help the user implement the protocol with minimal effort.

Figure 1 describes the hardware schematic for the interface between the Microchip 11XXX series of UNI/O bus-compatible devices and the PIC10F202 microcontroller. Figure 2 shows the schematic for the PIC12F508, and Figure 3 shows the schematic for the PIC16F505. The schematics show the connections necessary between the microcontroller and the serial EEPROM as tested. The software was written assuming these connections. The single I/O connection between the microcontroller and the serial EEPROM includes a recommended pull-up resistor.

FIGURE 1: CIRCUIT FOR PIC10F202 AND 11XXX SERIAL EEPROM



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FIGURE 2: CIRCUIT FOR PIC12F508 AND 11XXX SERIAL EEPROM

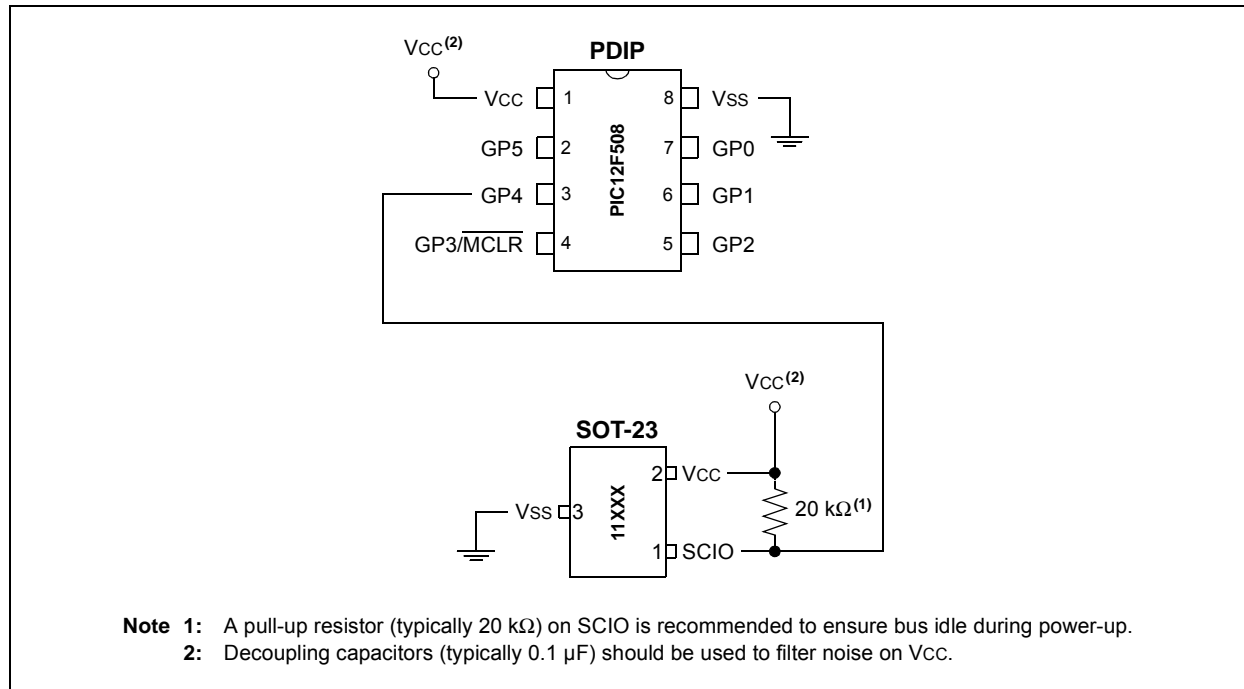
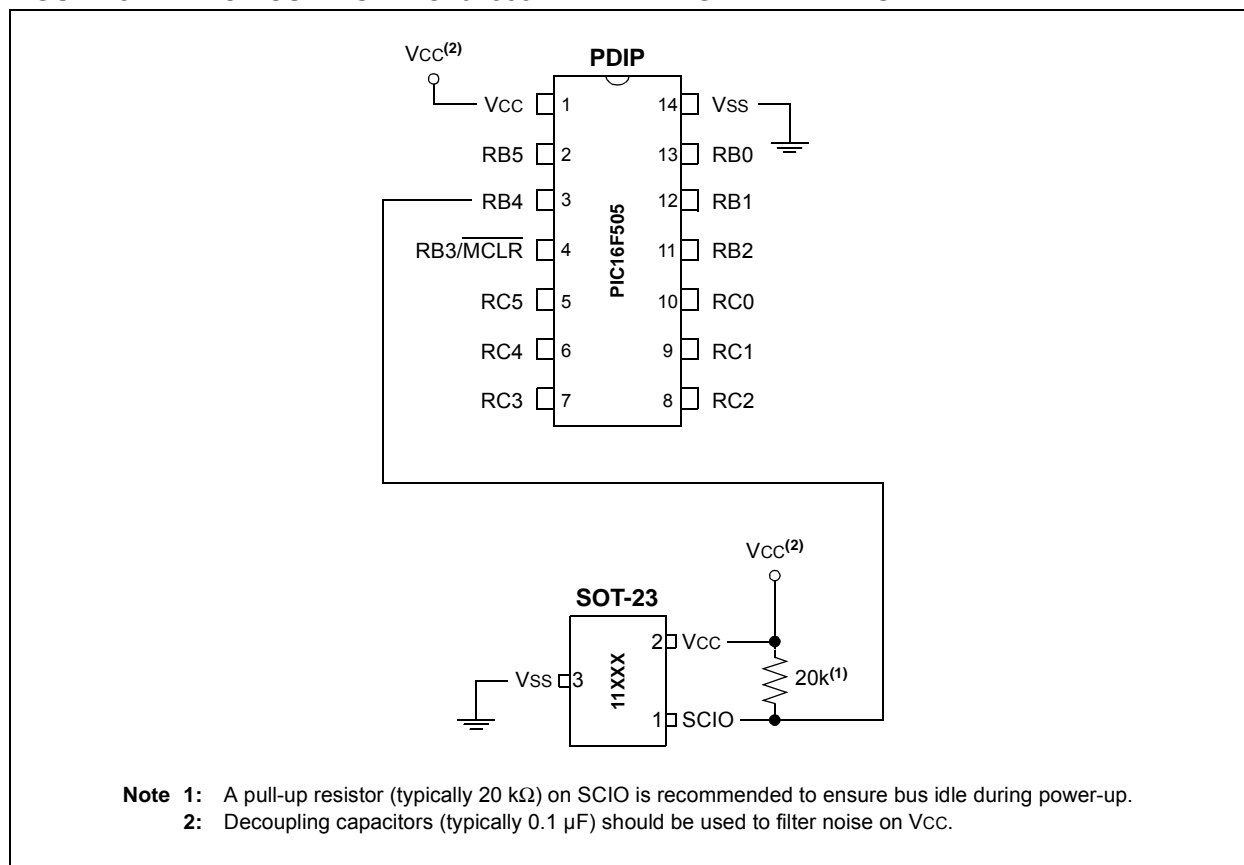


FIGURE 3: CIRCUIT FOR PIC16F505 AND 11XXX SERIAL EEPROM



FIRMWARE DESCRIPTION

The purpose of the firmware is to show how to generate specific UNI/O bus transactions using a general I/O pin on the microcontroller. The focus is to provide the designer with a strong understanding of communication with the 11XXX serial EEPROMs, thus allowing for more complex programs to be written in the future. The firmware was written in assembly language using the Microchip PICkit™ 2 development tool. The code can easily be modified to use any I/O pin that is available.

No additional libraries are required with the provided code. Separate projects are provided for the PIC10, PIC12, and PIC16. Within each project, the firmware consists of three files, and the main program for each is organized into five sections:

- Initialization
- Write Enable
- Page Write
- WIP Polling
- Page Read

The program utilizes the WIP polling feature for detecting the completion of the write cycle after the page write operation. The read operation allows for verification that the data was properly written. No method of displaying the input data is provided, but an oscilloscope can be used.

The code was tested using the 11LC160 serial EEPROM. This device features 2K x 8 (16 Kbits) of memory and 16-byte pages. Oscilloscope screen shots are labeled for ease in reading. The data sheet versions of the waveforms are shown below the oscilloscope screen shots. The internal 4 MHz RC oscillator is used to clock the microcontroller. If a different clock is used, the code must be modified to generate the proper timings. All values represented in this application note are hex values unless otherwise noted.

EXAMPLE 1: SUCCESSIVE SUBROUTINE CALLS

```

CALL      OutputByte      ; Output byte
MOVLW    WRITE_CMD       ; Load command into WREG (1 inst)
GOTO     $+1              ; Delay to ensure 3 insts. between calls (2 insts)
CALL     outputByte       ; Output byte
    
```

BIT PERIOD TIMING

Subroutine Overhead

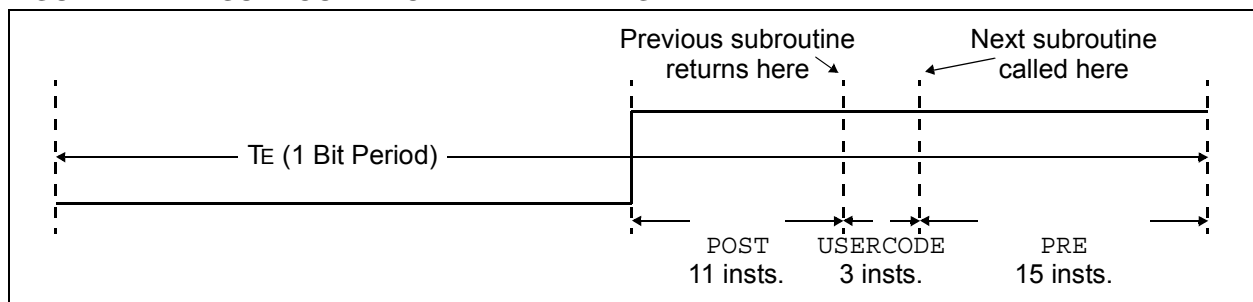
For this application note, a timer module on the PIC microcontroller was not used. Therefore, in order to maintain accurate timing, all instructions executed during communications must be taken into account. All of the provided subroutines have been designed to have the same amount of overhead. This means that the same number of instructions must be used between calls to each subroutine. The necessary number of instructions is defined as a constant named 'USERCODE', located within the 'UNIO PIC1x.inc' file. The constants 'PRE' and 'POST' specify the overhead within the subroutines, and should not be modified unless the subroutines themselves are changed. In Example 1, 'USERCODE' is set to 3, and so a GOTO instruction is required to ensure 3 instructions are executed between subroutine calls.

Figure 4 shows how the 'PRE', 'USERCODE', and 'POST' constants determine the bit period, and Equation 1 shows how to calculate the bit period based on these constants. In this example, because each half of the period must be balanced, one period contains 58 instructions. With $T_{CY} = 1 \mu s$, this equates to $58 \mu s$ per bit period, or 17.24 kbps. If additional instructions are needed between subroutine calls, then the 'USERCODE' constant can be modified. It is important that the proper number of instructions, as defined by 'USERCODE', are always used between subroutine calls within a command. Note that changing the number will also affect the bit period.

EQUATION 1: BIT PERIOD

$$T_E = 2 \cdot (PRE + POST + USERCODE) \cdot T_{CY}$$

FIGURE 4: SUBROUTINE OVERHEAD TIMING



Achieving Necessary Delays

In order to ensure the proper timings are met, loops have been placed at the necessary locations within the code. A simple macro, shown in Example 2, was developed to achieve these loops.

The total number of instructions necessary for the desired delay is passed as the 'numinsts' argument, while a unique label is passed as the 'looplabel' argument. The macro will calculate the number of loops

necessary to achieve the specified delay, and will also generate an additional NOP or GOTO instruction to account for errors in rounding.

To enable the constants shown above to be modified easily, equations have been used for each location where the macro is called. These equations should not be modified unless the subroutine code has been changed and a different delay is needed.

EXAMPLE 2: DELAYLOOP MACRO

```
DELAYLOOP    MACRO numinsts, looplabel
MOVLW       (numinsts+.1)/.3           ; Load count into WREG
MOVWF       delayCount                 ; Copy WREG to delayCount
looplabel    ; Each loop is 3 inst. (2 for last loop)
DECFSZ      delayCount,F               ; Decrement delayCount, check if 0
GOTO        looplabel                  ; If not 0, keep looping

; Now account for miscalculations by adding instructions. This also accounts
; for the loop executing only 2 instructions for the last count value.
#if (numinsts%.3)==.0                   ; Account for 1-inst miscalculation nop
#else
#if (numinsts%.3)==.1                   ; Account for 2-inst miscalculation
    goto    $+1
#endif
#endif
#endif
    endm
```

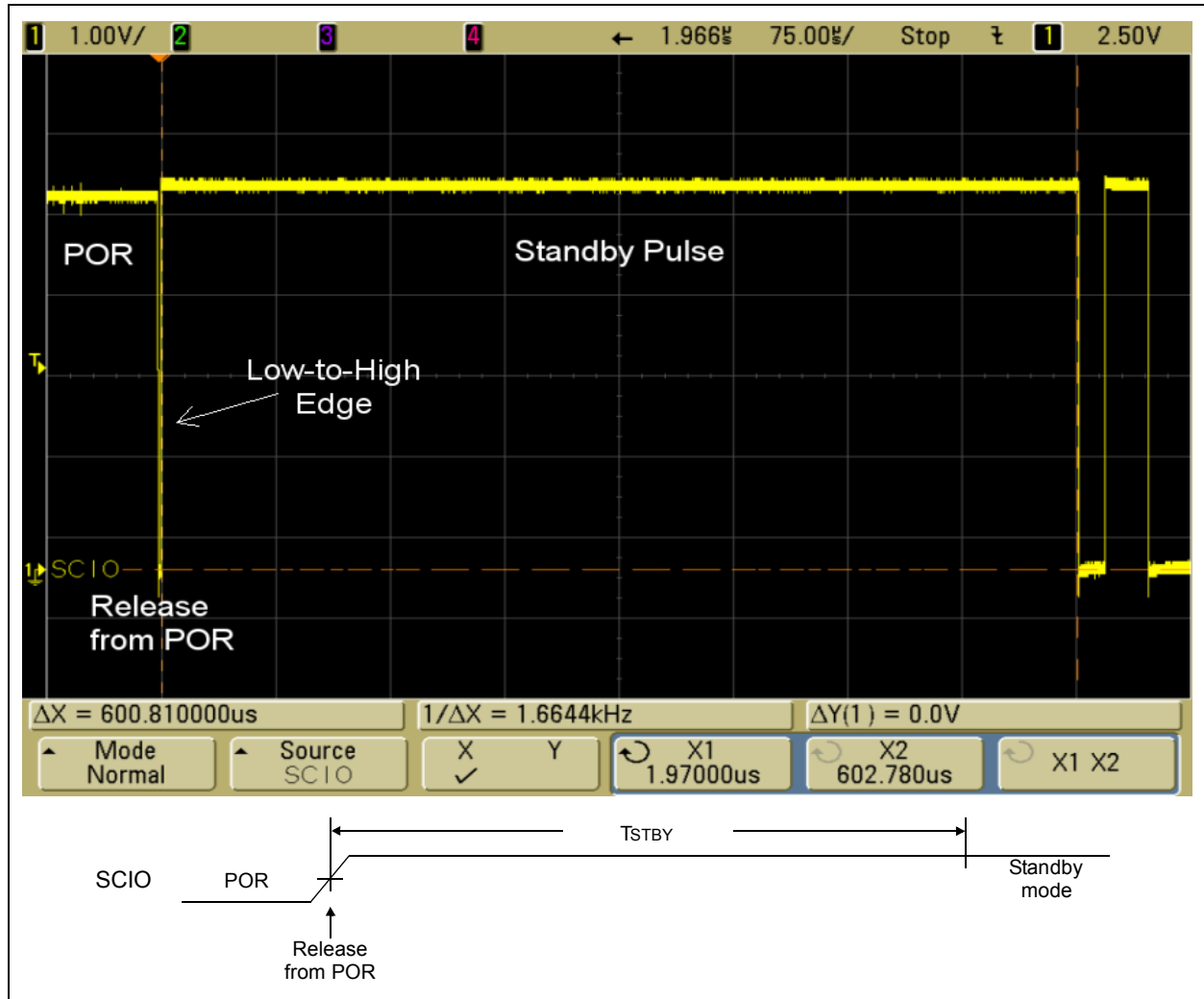
INITIALIZATION

Before initiating communication with the 11XXX, a low-to-high edge on SCIO must be generated to release the device from POR. Because bus idle is high, this is performed by creating a high-low-high pulse on SCIO.

Once the device has been released from POR, a standby pulse with a minimum timing of TSTBY is performed to place the device into Standby mode.

Note that once a command has been executed successfully (indicated by the reception of a SAK following the NoMAK), the device will enter Standby mode immediately and a standby pulse will not be necessary. In this case, only a period of TSS must be observed before initiating another command to the same device.

FIGURE 5: STANDBY PULSE



WRITE ENABLE

Before a write operation to the array or the STATUS Register can occur, the Write Enable Latch (WEL) must be set. This is done by issuing a Write Enable (WREN) instruction.

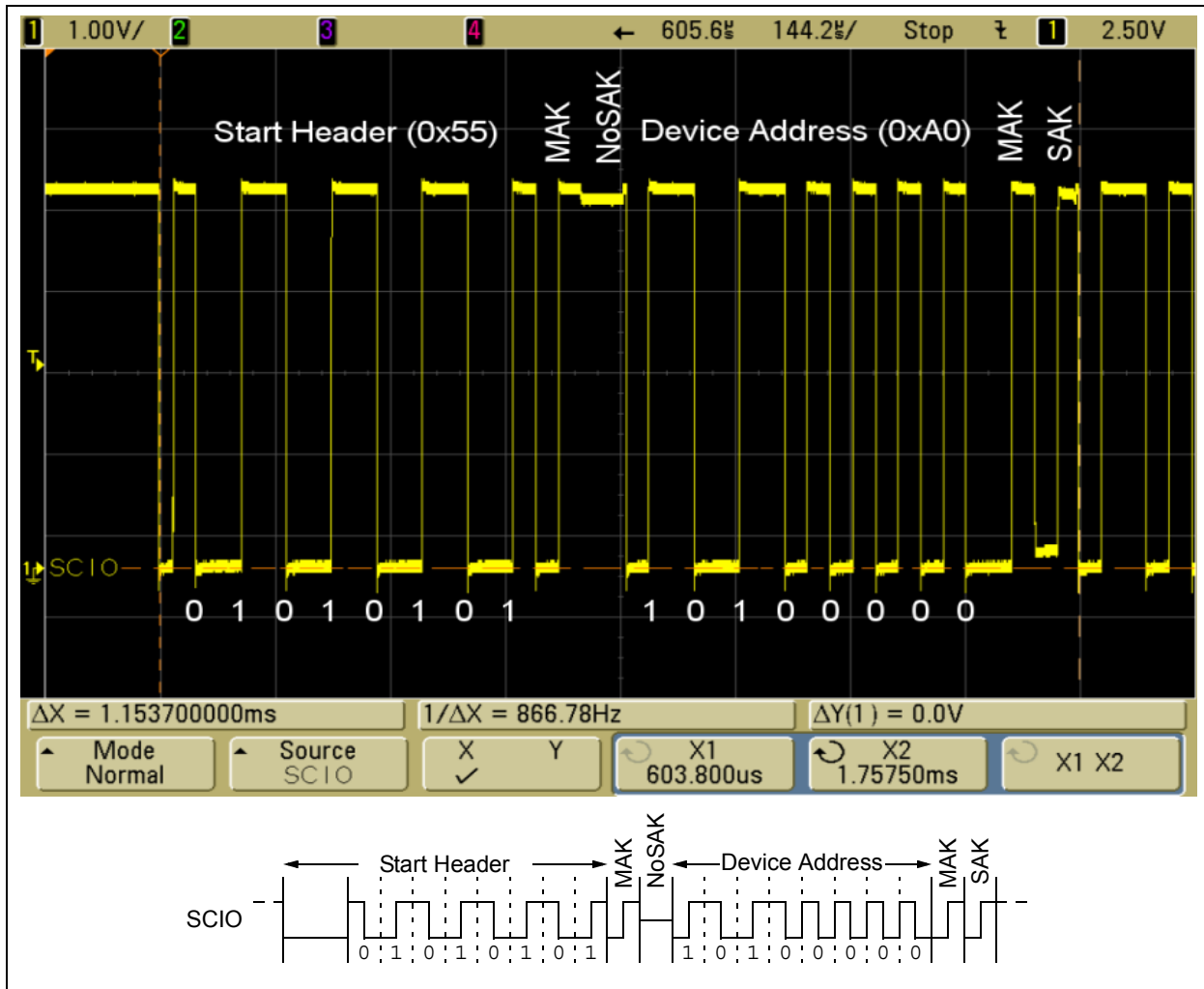
The WEL can be cleared by issuing a Write Disable (WRDI) instruction. It is also cleared upon termination of a write cycle to either the array or STATUS register, and upon POR.

The Write Enable operation has been broken down into the following components: the start header followed by the device address and the command byte.

Start Header and Device Address

To issue a WREN instruction, the master transmits the start header. This consists of a low pulse (THDR), followed by '01010101', and a Master Acknowledge (MAK), followed by a NoSAK. Next, the master transmits the device address ('10100000') and another MAK. The 11XX then responds with a SAK if the start header and device address were received correctly. Figure 6 shows an example of the start header and device address.

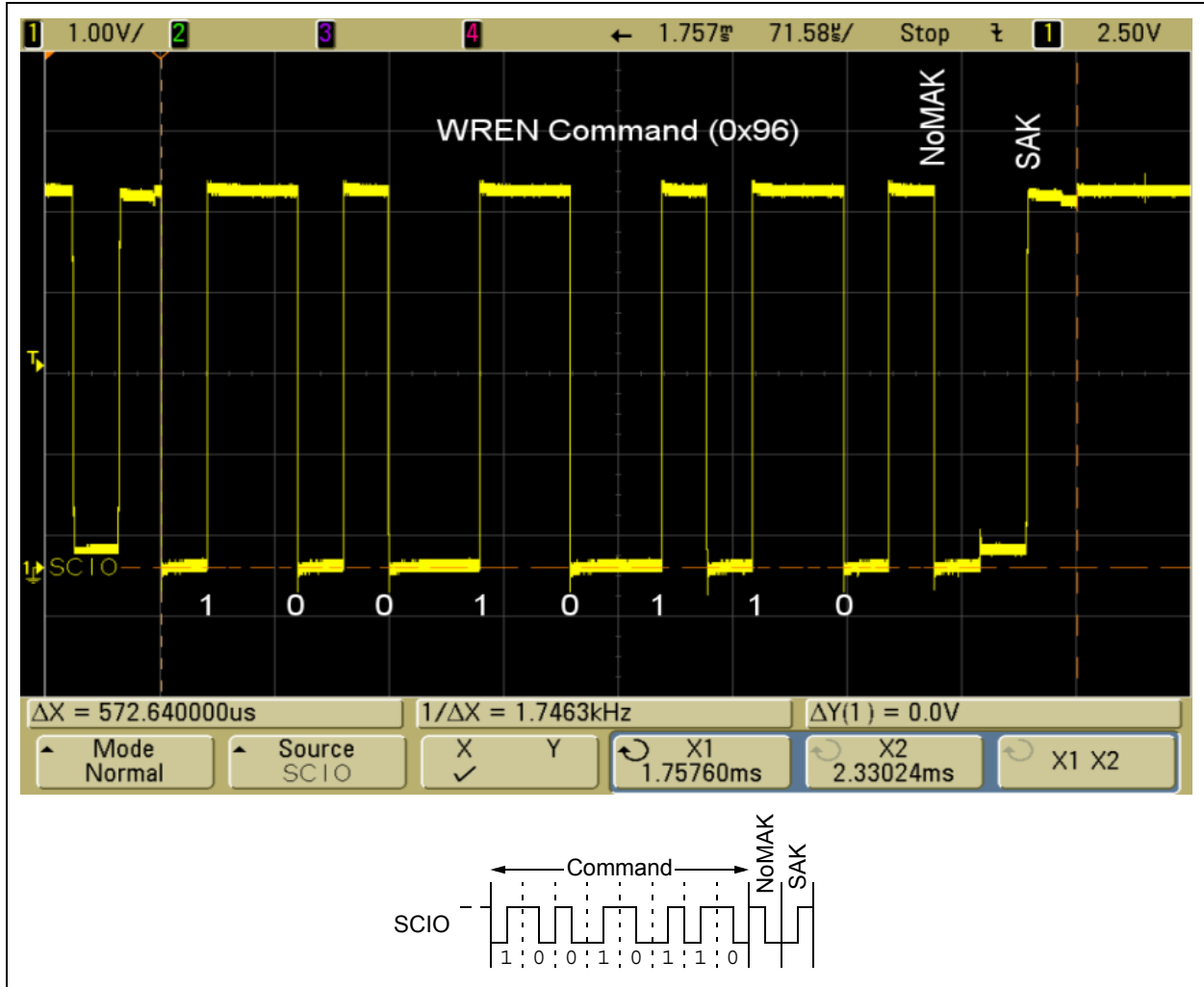
FIGURE 6: START HEADER AND DEVICE ADDRESS



Write Enable Command Byte

Once the SAK is received following the device address, the master transmits the WREN command byte and performs a final Acknowledge sequence. During this last sequence, a NoMAK must be sent to signal the end of the operation. Once again, the 11XXX responds with a SAK indicating it received the byte successfully. Figure 7 shows an example of the WREN command byte.

FIGURE 7: WRITE ENABLE (WREN) – COMMAND BYTE



PAGE WRITE

Once the `WREN` instruction has been performed, a page write operation can be executed to write data to the array. The 11XXX features a 16-byte page, so up to 16 bytes of data can be written within a single operation.

The page write operation has been broken down into the following components: the Write command followed by the word address and the data bytes. Note that the start header and device address are not illustrated in this section but are still required to initiate the operation.

Before beginning the `WRITE` instruction, a period of `Tss` must be observed following the `WREN` operation. This period can be used in place of the standby pulse after a command has been executed successfully when addressing the same slave device.

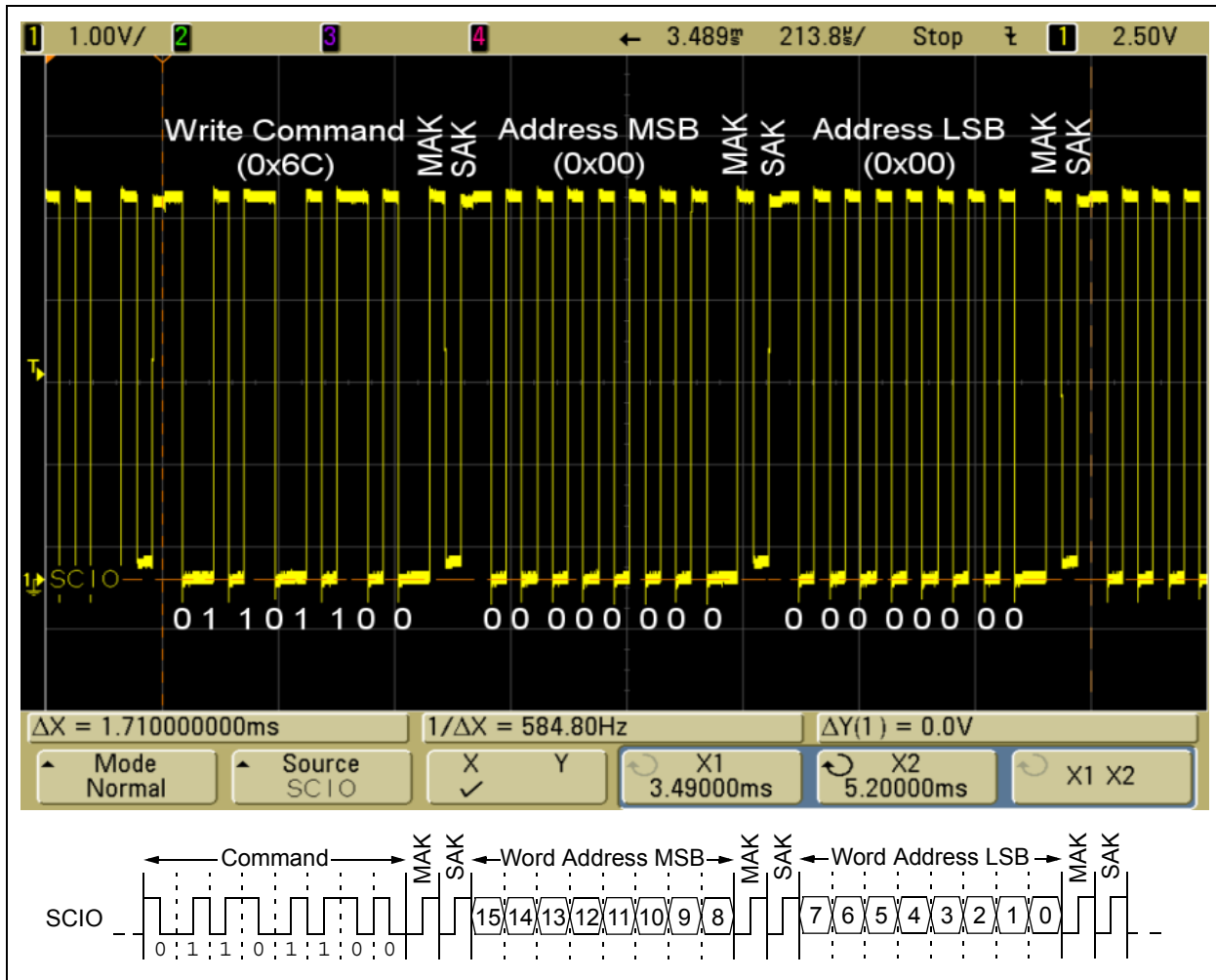
After the `Tss` period, the start header and device address are transmitted as described on page 6.

Write Command Byte and Word Address

After the start header and device address have been sent, the master transmits the Write command ('01101100' or 0x6C) and the word address. The 11XXX uses a 16-bit word address to access the array, so two bytes must be transmitted for the entire word address, with the Most Significant Byte sent first. After every byte, the master must transmit a `MAK` and the slave will respond with a `SAK`.

Figure 8 shows an example of the Write command byte and the word address.

FIGURE 8: WRITE – COMMAND BYTE AND WORD ADDRESS



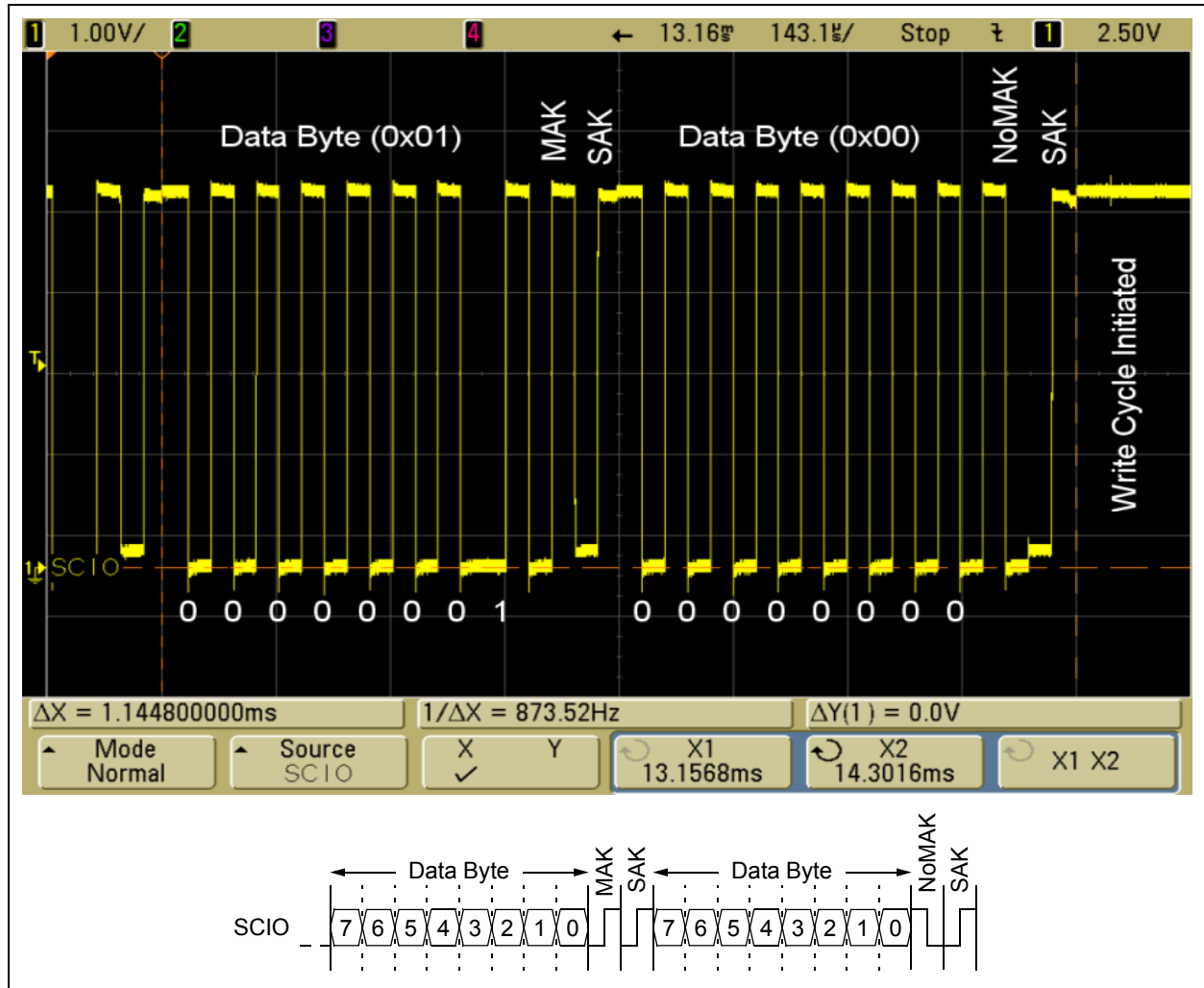
Data Bytes

Once the word address has been transmitted and the last SAK has been received, the data bytes can be sent. Up to 16 bytes of data can be sent within a single operation. After each byte is transmitted, the master sends a MAK and the slave responds with a SAK. If at any point a NoSAK is received, this indicates an error occurred and the operation must be restarted, beginning with a standby pulse.

Once all data bytes have been sent, the master terminates the command by generating a NoMAK in place of the MAK, and the slave device will again respond with a SAK. This will also initiate the internal write cycle.

Figure 9 shows the final two data bytes sent by the master as well as the NoMAK and SAK.

FIGURE 9: WRITE – FINAL TWO DATA BYTES



WRITE-IN-PROCESS POLLING

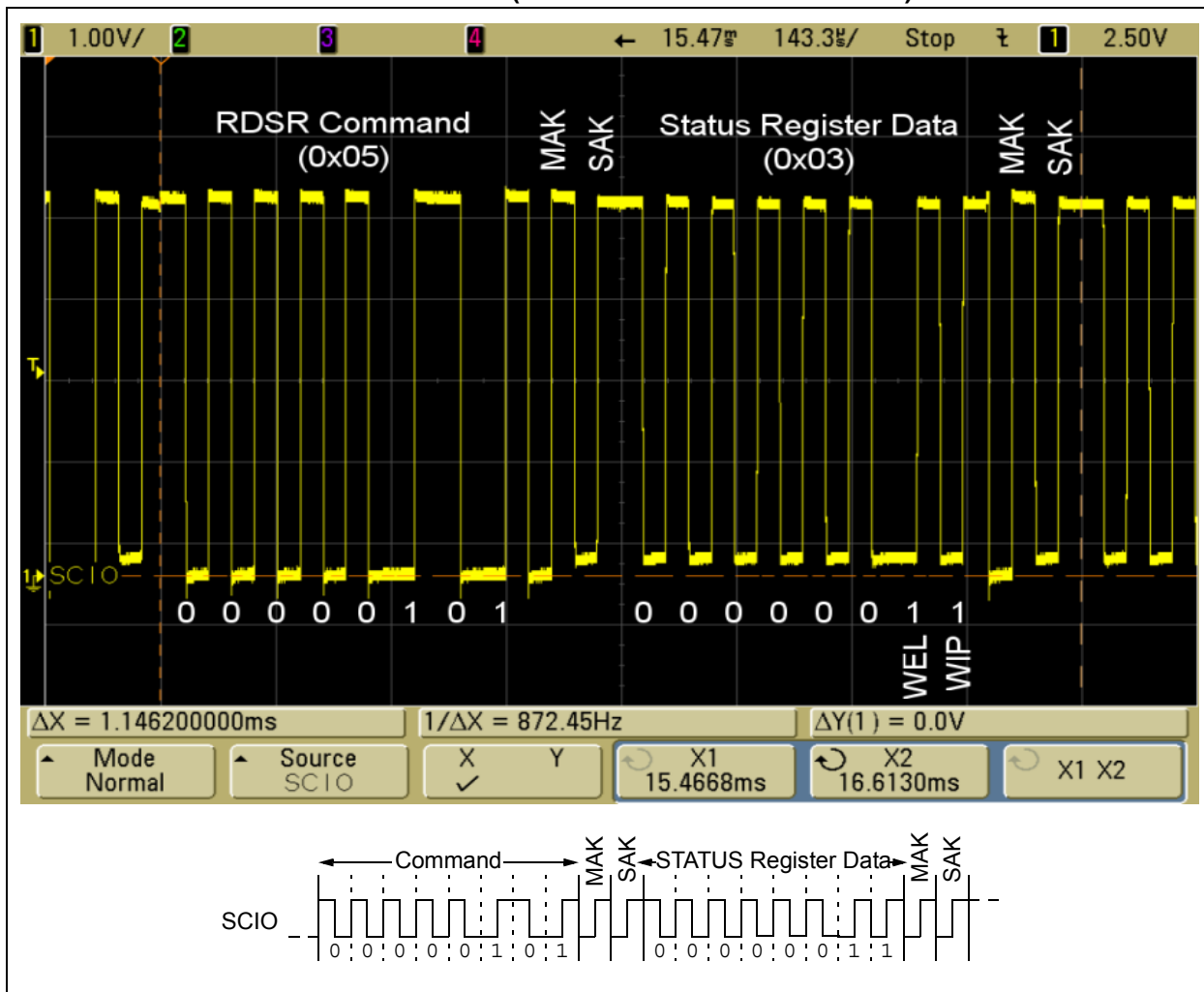
After an array or STATUS register WRITE instruction is executed, a write cycle time (TWC) must be observed. This time is a maximum, and so the actual time required is typically less. Therefore, in order to transfer data as efficiently as possible, it is highly recommended to use the WIP polling feature, similar to that available on Microchip SPI serial EEPROMS. Since the STATUS register can be read during a write cycle, the Write-In-Process (WIP) bit can be continuously monitored to determine the completion of the write cycle.

Write-In-Process Polling Routine

The process of WIP polling consists of sending a start header and device address, after observing the Tss period, as described on page 6, followed by the Read Status Register (RDSR) command ('00000101' or 0x05). After the subsequent SAK, the 11XXX will transmit the STATUS register. At this point, the STATUS register can be requested again by sending a MAK. The WEL and WIP values sent are updated automatically, and so the master can continue to read the STATUS register value until the WIP is cleared. Sending a NoMAK terminates the command.

Figure 10 shows an example of WIP polling to check if a write operation has finished. In this example, the WIP bit is set ('1'), which indicates that the write cycle has not yet completed.

FIGURE 10: WIP POLLING ROUTINE (SHOWING WRITE-IN-PROCESS)



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PAGE READ

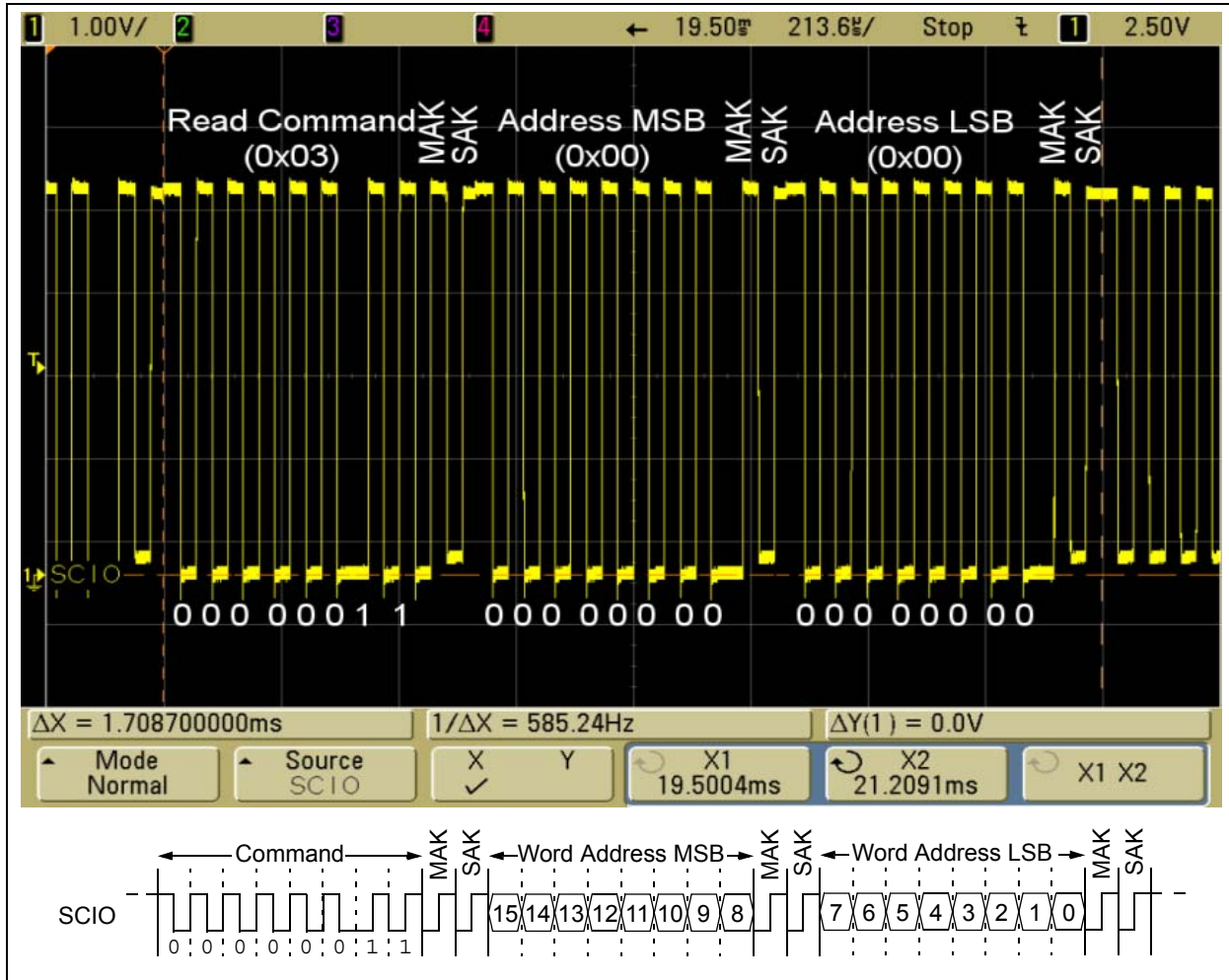
The 11XXX device allows data to be read from the array in a random access manner. Reading data from the array is very similar to the write operation, except that the read is not limited to a single page.

In order to read from the array, the start header and device address must first be sent after observing the Tss period. The Read command byte and word address bytes are transmitted next. The master must generate MAK after every byte, and the slave will respond with a SAK if no errors occurred.

Command and Word Address for Read

Figure 12 shows an example of the Read command ('00000011' or 0x03) followed by the word address.

FIGURE 12: READ – COMMAND BYTE AND WORD ADDRESS



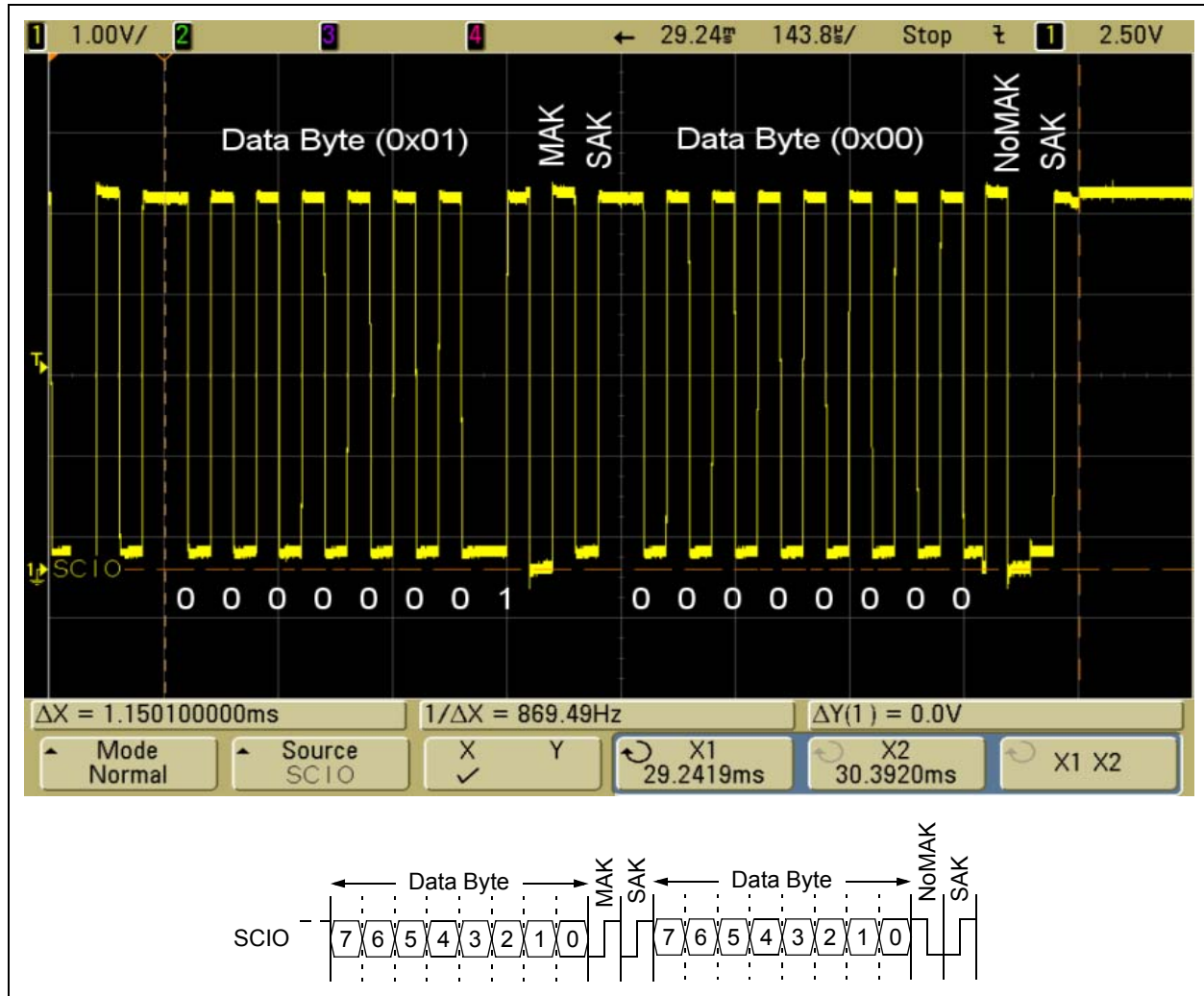
Reading Data Back

After the command and word address have been sent and acknowledged, the 11XXX sends the first data byte from the array, starting at the address specified.

In order to continue the read, the master must send a MAK after each data byte. The slave responds with a SAK if there are no errors. After each data byte has been sent, the 11XXX will automatically increment the internal word address to output the next data byte. The read operation is not limited to a single page, and so the entire array can be read within a single operation if the master continues to request data. At the end of the array, the internal word address will automatically be reset back to '0x000'. A NoMAK terminates the operation.

Figure 13 shows the master reading the final two bytes of data. A NoMAK is sent after the last byte to indicate that no more data is requested and to terminate the command.

FIGURE 13: READ – FINAL TWO DATA BYTES



CONCLUSION

This application note provides examples of the basic commands for communicating with the UNI/O bus-compatible family of devices. These functions are designed to be used in an end application with very little modification. The code generated for this application note was tested using the PICkit™ 2 Low Pin Count Demo Board with the connections shown in Figure 1, Figure 2 and Figure 3.

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