AN1115

Implementing Digital Lock-In Amplifiers Using the dsPIC® DSC

Author: *Darren Wenn*
Microchip Technology Inc.

INTRODUCTION

Lock-in amplifiers use phase-sensitive detection to measure the presence of small signals buried in large amounts of noise. By measuring the coherent system response from an incoming AC signal, the digital lock-in amplifier can detect even minute changes. Both magnitude and phase can be used to characterize the system.

Conventionally, lock-in amplifiers use complicated (and expensive) analog circuitry to perform the phase-sensitive detection and filtering. However, modern Digital Signal Controllers (DSCs), such as the dsPIC30F and dsPIC33F families, can be used to remove large amounts of the analog circuitry by performing the necessary operations in software. This capability provides a number of additional benefits including increased reliability, resistance to temperature and aging effects, and the ease with which the system can be modified in the field. By using the built-in signal processing capabilities of the dsPIC33F, it is possible to perform high-speed, high-accuracy measurements on sensors such as strain gauges. The same technique can be applied to other noisy systems such as capacitive sensors or the measurement of modulated light levels.

While the basic process is conceptually simple, there are a number of possible ways of implementing it in a microcontroller, and the implementation details are frequently missing from existing published material.

This application note provides information on practical ways in which a digital lock-in amplifier can be implemented in software using the dsPIC33FJ256GP710 on an Explorer 16 board. This application note also considers a number of performance enhancements that can dramatically reduce the processing requirements. Source code is provided that will execute on the Explorer 16 board (see **Appendix A: "Source Code"**).

THEORY

A lock-in amplifier can measure small AC signals of only a few nanoVolts even in the presence of noise sources of much greater amplitude. They do this by using a Phase Sensitive Detection (PSD) circuit that can discriminate a single frequency of interest by comparing the incoming signal's phase and amplitude to a reference signal. Signals from interfering sources that do not have the same frequency and phase relationship to the reference are rejected by the PSD.

To illustrate why this technique is useful, consider the example of a 100 nV sine wave with a frequency of 40 kHz. It would be difficult to measure this signal directly, so some amplification is necessary. Equation 1 shows the resulting output signal, assuming that the amplifier has a gain of 1000.

EQUATION 1:

$$1000 \times 100nV = 100\mu V$$

However, any amplifier adds noise to the signal. A good circuit will add around $5nV/\sqrt{Hz}$.

Assuming the amplifier in this example has a bandwidth of 200 kHz, the circuit will also add broadband noise equal to that of Equation 2.

EQUATION 2:

$$5nV \times 1000 \times \sqrt{200kHz} = 2.2mV$$

In other words, after amplification, the noise level will be 22 times the signal level at the desired frequency.

It is possible to precede the amplifier with a band pass filter centered at 40 kHz. But even a very high quality analog filter will only have a Q factor of 100.

Note:	Q, which is referred to as the quality factor, is equal to the center frequency of a signal divided by its bandwidth at the half power point and describes how 'tight' a filter is.

Such a Q factor would still give a noise signal as shown in Equation 3.

EQUATION 3:

$$5nV \times 1000 \times \sqrt{40kHz/Q} = 100\mu V$$

where Q = 100

This 100 µV signal is still difficult to measure relative to the noise. However, because a Phase Sensitive Detector can have a Q as high as 10,000, the noise signal in our example could be reduced to only 10 µV, making it possible to perform measurements on the original signal.

Phase Sensitive Detectors

Phase Sensitive Detectors are common signal processing elements that are often used to demodulate a signal's frequency from its fixed-frequency carrier. If two signals are multiplied together, basic physics dictates that the result will be a signal consisting of the sum and difference of the two original signals, as expressed by the following derivation shown in Equation 4.

EQUATION 4:

$$V_{output} = V_{in}\cos\langle\omega t\rangle \times V_{ref}\cos(\omega t + \theta)$$

where θ is the phase difference between the two signals.

Based on this, V_{output} is then equal to that of Equation 5.

EQUATION 5:

$$\begin{aligned} V_{output} &= V_{in}V_{ref}(\cos 2\omega t\cos\theta - \cos\omega t\sin\omega t\sin\theta) \\ &= \frac{V_{in}V_{ref}}{2}(\cos\theta + \cos 2\omega t\cos\theta - \sin 2\omega t\sin\theta) \\ &= \frac{V_{in}V_{ref}}{2}\cos\theta + \frac{V_{in}V_{ref}}{2}\cos(2\omega t + \theta) \end{aligned}$$

If we call the second signal the reference and set it equal to the frequency of interest, the output will be proportional to the magnitude of the input signal and the phase relationship between the input and the reference. It will also be modulated at twice the reference frequency.

By then passing the output signal through a low-pass filter, the 2ωt signal can be removed, leaving the final DC signal.

By adjusting the response of the low-pass filter, any interfering signals with a varying phase relationship and, consequently, any varying frequency, can be removed from the final result. It is useful to consider the basic operation of the analog lock-in amplifier before moving on to a digital solution.

Analog Lock-In Amplifiers

The block diagram of a conventional analog lock-in amplifier is shown in Figure 1. The system consists of an input amplifier stage that amplifies the signal to a suitable level for further manipulation, perhaps performing an impedance conversion in the process. A band-pass filter is then used to remove any signal components that are either at the DC level or at harmonics of the signal to be measured.

The next stage is the Phase Sensitive Detector, also known as a synchronous demodulator or mixer. This circuit can take many forms, from a logarithmic amplifier to dedicated four-quadrant multipliers. The input signal is multiplied by a reference signal derived from the system being measured. Since the reference signal must maintain a fixed-phase relationship to the input signal, it is often locked to the reference signal using a Phase-Locked Loop (PLL).

A further refinement commonly found on commercial devices is the dual channel function. In this case the input is mixed with the reference, and is also mixed with a 90 degree phase-shifted version of the reference. This channel function has the useful property that it is then quite simple to directly calculate the magnitude of the input and its phase relationship to the reference. These two separate channels are normally called the In-Phase component and the Quadrature component, or I and Q, respectively.

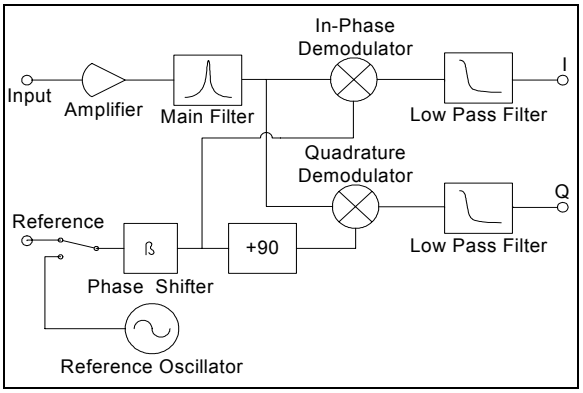
Finally, the output from the mixers is fed into low-pass filters, which effectively remove any non-coherent signals, leaving a final DC signal proportional to the amplitude and phase of the input signal.

There are a number of problems with analog lock-in amplifiers. For the highest accuracy, the reference signal must have a very low harmonic content. In other words, it must be a very pure sine wave since any additional harmonic content will cause distortion at the output. Analog sine wave generators can also suffer from amplitude variations due to temperature drift.

Temperature drift and component tolerances elsewhere in the system can cause further problems in the analog system. Real world op amps have offsets associated with them that need careful trimming to prevent errors in the DC output.

Finally, any non-linearity in gain and phase will lead to further errors in the final output. While these problems are not insurmountable, the result is that analog lock-in amplifiers tend to be expensive pieces of equipment and are more often used if high-input bandwidths are required.

FIGURE 1: ANALOG LOCK-IN AMPLIFIER



Digital Lock-In Amplifiers

In the case of a digital lock-in amplifier, most of the processing is performed in the digital domain using software and dedicated Digital Signal Processing (DSP) hardware. The basic block diagram for a digital lock-in amplifier is shown in Figure 2. The system still features a front-end amplifier; however, this is then followed by an anti-aliasing filter to remove any signal components higher than half the sampling frequency.

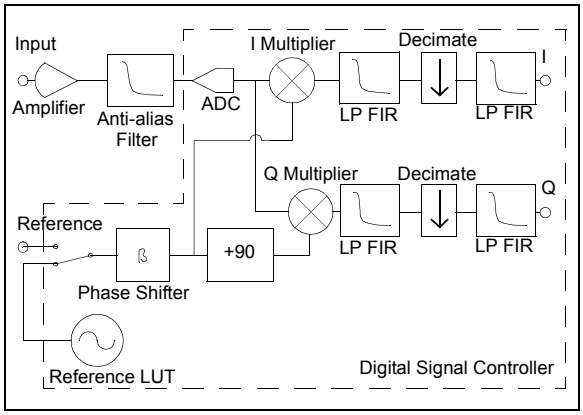
For a dsPIC® DSC-based solution, the sampling would be performed in 12-bit resolution at up to 400 kHz, so the anti-aliasing filter needs to be set to attenuate any signals above 200 kHz. In practice, the filter may have a much narrower band than this, and for a signal of interest at 25 kHz, the filter may be set as low as 40 kHz.

The reference signal is generated internally or can be derived from sampling an external signal. In the case of internally generated signals, the individual sample points of the reference signal can be calculated to a high degree of accuracy, and therefore do not suffer from the typical errors found in the analog Lock-In. The reference signal is also phase-shifted by 90 degrees by either a table lookup or simple mathematical operations. Next, the reference and phase-shifted reference values are multiplied directly by the DSP to generate the intermediate I and Q signals. Finally, these signals are passed through digital low-pass filters to generate the final output values. Interestingly, it is the digital low-pass filter stage that can cause the most implementation problems for the software engineer. The data being sampled is arriving at a high rate, and even though the output filters could be operating at only a few Hertz, the Finite Impulse Response (FIR) filters typically used may require many thousands of taps. The amount of RAM required for the implementation can become prohibitively large and result in a costly implementation. However, as is shown later, some clever DSP techniques can be used which reduce these requirements.

Once the input signal has been quantized by the analog-to-digital converter, there is no further loss of signal quality. Furthermore, since the reference signal can be digitally computed, it can be made to have a very low harmonic content. In the case of the 16-bit dsPIC DSC processor, any harmonics will be at the -90 dB level.

Most importantly, the deviations due to non-linear gain and phase of the analog components are removed in the digital lock-in amplifier and there will be no variations due to temperature drift or component aging. Similarly, the offsets associated with real analog components are removed and the limitation on intermediate accuracy is purely down to the resolution of the processor and DSP engine.

FIGURE 2: DIGITAL LOCK-IN AMPLIFIER



APPLICATION

Although the amplifier can be used in many areas, it typically is found where high-resolution, high-accuracy measurements are required at relatively low data rates. So, having examined how the digital lock-in amplifier works, let us now consider how it can be used to improve the performance of an important application, such as weight measurement using the Wheatstone Bridge.

The Wheatstone Bridge

Commercial weighing scales are made from four similar value resistors, or strain gauges, connected to form a Wheatstone Bridge. Typically, this bridge arrangement is stimulated by applying a 10V DC signal. Small deflections cause a voltage to appear on the output of the circuit.

Noise Sources

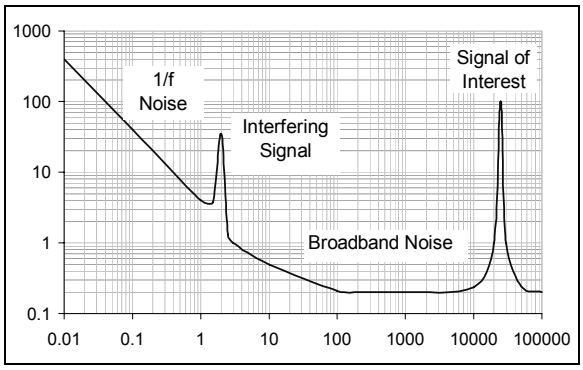
One reason to use a bridge arrangement is that error sources, such as temperature drift, can be made to cancel each other out. However, since the nominal output is half the drive voltage, it can be difficult to measure small µV signals at the output. Any form of induced noise in the system can easily be picked up by the high-impedance amplifiers that are used. A high Common-Mode Rejection Ratio (CMRR) is required because of the high input voltage at the amplifier stage. Any junctions between dissimilar metals in the system can result in noise induced by the thermoelectric effect, so this condition must also be accounted for.

In fact, any electronic system will be subject to internally generated noise and, if we consider the more general situation, it is apparent that interference can come from any number of sources. Interference from the local main power supply can be seen on DC measurements, but a lock-in amplifier can be harmonically linked to this noise source and, therefore, provide complete rejection of the interfering signal.

Resistors in a measurement system generate Johnson noise across their terminals. This generated noise is proportional to temperature and bandwidth. In general, the noise spectrum of any electronic system follows a 1/f relationship. It is for this reason that a lock-in amplifier can yield such good performance.

Figure 3 shows the typical noise spectrum found in many electronic circuits with a general broadband component covering all frequencies, 1/f noise located at the lower end of the spectrum and individual interfering signals. As indicated by locating the reference signal at a higher frequency, it will be subject to a much lower noise floor than if the measurement had been made at DC levels.

FIGURE 3: ELECTRONIC NOISE SPECTRUM

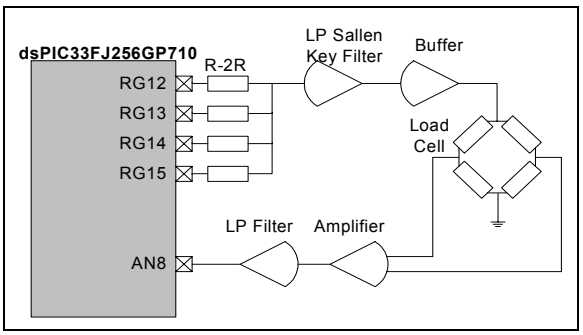


IMPLEMENTATION

The basic requirement for the hardware is that it should be able to sample a single analog channel at high speed. The data should be collected and analyzed in real time, and the calculated I and Q values should be output via an RS-232 serial channel or displayed directly on an LCD. As we shall see later, the magnitude and phase relationship between the signals can be simply calculated and it should be possible to display these values as well. A further enhancement, described in the next section, is for the hardware to be able to generate the reference signal that is applied to the application circuit.

The implementation of a digital lock-in amplifier has been achieved using the Explorer 16 development board. This multipurpose unit can be used to test out a number of different Microchip 16-bit processors and digital signal controllers and, in this case, a dsPIC33FJ256GP710 DSC was used. The processor is set to derive its main clock from an external crystal, such that it will operate at its maximum speed of 40 MIPS, which results in an instruction cycle time of 25 nS. While other values could be chosen, it would normally be selected so that the majority of timings in the rest of the system are integer multiples of the instruction cycle time. A simplified block diagram is shown in Figure 4.

FIGURE 4: EXPLORER 16 IMPLEMENTATION



The application circuit, consisting of an R-2R ladder, low-pass filters and amplifiers, was designed and constructed on a small PCB designed to fit into the PICtail™ Plus connector of the Explorer 16 board. The circuit is fairly simple and could also be easily constructed within the prototyping area of the board if required. The load cell is a commercial device capable of measuring up to 10 kg loads connected to the circuit via leads.

The built-in digital signal processing capabilities of the dsPIC DSC allow for high-speed sampling and manipulation of the data coming from the sensor. The majority of the software was developed in C using the MPLAB® C30 compiler and MPLAB IDE. Writing the program in C enables the DSP libraries supplied with MPLAB C30 to be used to implement the signal processing operations required by the algorithm.

The Reference Signal

The lock-in amplifier requires a reference signal to perform the phase sensitive detection. This reference signal could be derived from the system being measured. For instance, a common application is low-light level measurement in spectroscopy. In these systems, minute changes in a light beam are detected by first modulating the light using a rotating slotted wheel. This chops the light beam, which is then passed through the rest of the system to the detector. At the same time, the reference signal can be derived by placing a photo detector next to the wheel measuring the output from an index hole.

In this application, it is necessary to generate an AC signal to drive the bridge circuit and thus the strain gauges. Therefore, it is convenient to use the DSC to generate an output at the desired frequency. There are a number of techniques that can be used including PWM sine wave generation, overlapping the outputs from a number of Capture/Compare/PWM (CCP) modules, or simply using an R-2R ladder circuit. In this application, the latter technique has been used.

The multi-way connector on the Explorer 16 gives access to the port lines and these outputs are used to drive a resistor network and buffer amplifier providing an output sine wave with 16 discrete levels. The output

waveform is generated at 400 kHz with 16 output codes per wave, thereby generating an AC signal at 25 kHz. To smooth the output and remove unwanted harmonics, the signal is fed through a low-pass Sallen-Key filter with a corner frequency of 40 kHz.

Basic operation

This section will go on to describe the operation of the software detailing how the hardware is initialized, how the modules interact and also how the calculations were performed to generate the desired performance.

Since the ideal Wheatstone Bridge contains only resistive elements, there should not be any additional phase errors introduced by the sensor itself. Instead, all measured phase changes are solely due to the generation and measurement system. However, since this technique is applicable to a number of fields, including those where it is required to measure substantial phase changes, the software and discussion will be kept generic, and both I and Q will be calculated.

The initial description relates to the first iteration of the software, and the reader should note that a number of optimizations are possible that can improve the performance. It is only the final, optimized version of the code that is provided as source code along with this application note (see **Appendix A: "Source Code"**).

OUTPUT GENERATION

As previously mentioned, the reference signal can be externally derived or generated internally within the measuring device. In this case, we use a Timer to generate an interrupt every 2.5 µS. The source code for the initialization can be found in the file `init_timers.c`. Since it is essential that this routine never be interrupted or delayed, it is assigned a high priority level. Each time, through the Interrupt Service Routine (ISR), a simple circular counter moves through a table of values that are output on port pins RG<12:15>. The digital outputs are fed through the R-2R ladder and summed and filtered to form a sine wave with an amplitude of 3.3 Volts.

SAMPLING

The dsPIC33F family of devices features a 12-bit high-speed Analog-to-Digital Converter (ADC) module. This module can be configured at run time to operate in either 10-bit mode at up to 1 MSPS, or 12-bit mode at up to 500 kSPS. The ADC can take its conversion signal from a number of sources including self-timing, external triggers, timers or Motor Control (MC) PWM controllers.

For this application, it is important that all sampling and signal generation clocks are synchronized and that it is possible to change the phase relationship of the signals by changing the timings. For this reason, the ADC conversion is derived from Timer3 and is set to produce the convert signal every 2.5 µS (a rate of 400 kHz). The result is that there will be 16 sample points per cycle of the 25 kHz waveform. It should be noted that this is at the high end of the conventional 4-10 times sampling rates that are often selected by engineers, and as we shall see later, faster is not always most efficient.

Since the processor is simultaneously generating the output waveform, it would be difficult to directly sample and manipulate the data points as they arrive. For this reason, they are collected automatically and transferred into system RAM using the Dynamic Memory Access (DMA) controller on the dsPIC DSC. This flexible peripheral allows up to eight independent channels to be set up and can perform automatic data moves between configured peripherals and system memory or vice versa without processor intervention. In this case, DMA Channel 0 is set to transfer 32 samples into dual port memory using a ping-pong transfer mode. After the transfer, and while the next 32 samples are being collected, a `VectorMultiply` operation will perform the PSD multiplication generating initial I and Q data sets. Because the dsPIC DSC is generating the drive signal, it is not necessary to reconstruct the reference signal; therefore, the two multiply operations use idealized copies of the reference and 90 degree phase shifted reference signals.

SAMPLE SYNCHRONIZATION

Since the data is arriving at such a high rate, it is not possible to complete the entire signal processing task between batches of the arriving samples. For this reason, the software collates the results of 1024 multiply operations in memory and only then performs the low-pass filtering.

After having collected this many samples, the results of any subsequent data points are ignored until the current data has been processed. This introduces a problem if the restart of sampling occurs at a different point in the waveform than was previously being sampled because it will show up as a phase change and an error in the final output. To overcome this problem, the sampling is resynchronized to the start of the output waveform for each batch. Since some of the slower filters will use data from many batches of 1024 samples, they will, to a crude approximation, ignore the intervening gap and treat the data stream as if it had arrived in a continuous fashion. The problem this creates is that it can introduce significant noise into the final result, especially if the interfering signals have a low frequency and are synchronous with the batched sampling rates.

FILTERING AND DECIMATION

If we consider that a first attempt would be to filter the data using a low-pass FIR filter with a cut-off frequency of 10 Hz, a filter with over 55,000 taps would be required. This would imply that it would be necessary to use a device with access to very large amounts of RAM (up to 250 kBytes) to perform the required calculations. In addition to this, even with the highly efficient DSP engine in the dsPIC DSC, this would take over 5.6 million instruction cycles to compute, assuming it could be performed. This would effectively prevent the system from operating in anything like a real-time manner. To overcome the problem of filters with a large number of taps, the data is decimated (literally N-1 samples in N discarded) to reduce the effective data rate in a number of stages.

The decimation is performed by first low-pass filtering the data using a filter with a corner frequency less than half the desired final sample rate, and then discarding N-1 of the N original samples. For example, if we decimate a signal sampled at 400 kHz by a factor of 10, the final output will have a sample rate of just 40 kHz. However, to prevent aliasing, the original data must first be low-pass filtered using a 20 kHz filter to remove unwanted components. Finally, for every 10 data points in the original data stream just one output is produced.

If required, the output can then be filtered again but now using filters designed for the lower rate. This multi-stage technique allows considerable gains in efficiency over the brute force approach and can significantly reduce the computational load. The dsPIC DSC library includes the dedicated function, `FIRDecimate`, to perform these operations.

In the file `isr_DMAC.c`, the DMA Channel 0 ISR function takes 1024 sample points and decimates these samples down by a factor of 64, resulting in an effective sample rate of 6.25 kHz. This result is then FIR filtered again to yield a final pair of I and Q values. The pre-decimation filter contained 512 taps and the final 20 Hz low-pass filter contained 493 taps. In addition to the coefficient storage, each filter requires its own delay line storage so the total RAM requirement is just over 6 kBytes which is an improvement over the single filter.

OUTPUT DATA

Each time a new pair of results is generated, a global flag is set and the main program loop will convert the values to ASCII strings and display them on the Explorer 16 LCD display. The final I and Q data values can also be used by a higher level algorithm, or they can be directly converted into two values describing the magnitude and phase of the source signal using the following relationships shown in Equation 6.

EQUATION 6:

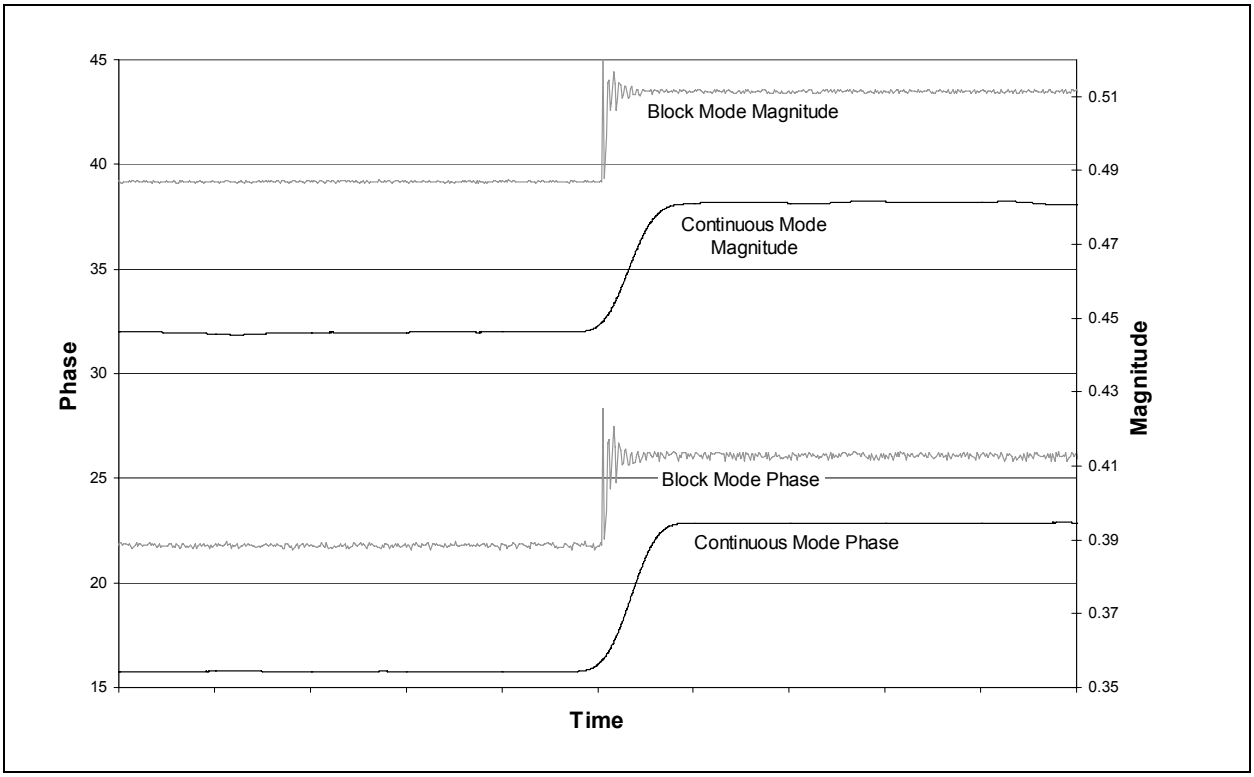
$$Magnitude = \sqrt{I^2 + Q^2}$$

$$Phase = \tan^{-1}(\frac{Q}{I})$$

The final output data can be seen in Figure 5, where the block mode curves indicate the output from this iteration of the software. Notice that the curves have a rapid response time. However, this response comes at the expense of considerable overshoot and large amounts of noise in the output.

One area where the application example differs from a normal digital lock-in amplifier is its ability to tune the phase offset to zero. If this were done, the output would consist purely of a single value, proportional to the force applied to the load cell. This capability could easily be incorporated by adjusting the starting values in the sampling and signal generation timers (TMR2 and TMR3) thereby affecting the phase relationship.

FIGURE 5: OUTPUT CURVES FOR 1 KG LOAD PLACED ON CELL



Faster

Having discussed the main features of the software, it is worthwhile to consider how its operation can be improved. If a timing analysis is performed, it can be seen that a significant amount of time must be spent performing the PSD multiplications and FIR routines. As previously mentioned, the amount of time required for these activities prevents the complete set of calculations from being performed before another set of 1024 samples arrive. Consequently, the sampling has to be halted and restarted each time, which can lead to discontinuities and ultimately noise in the final output.

A simple technique to improve the overall response of the system is to actually slow down the sampling rate. If we consider the operation of the PSD, it simply performs a sequence of multiplications. One argument is the sample value from the ADC. The other argument is mathematically derived from the value of the ideal wave at that discrete point in the sampling sequence. For example, the Q signal is derived from multiplying the incoming data, one sample point at a time, by the cosine value of the ideal wave at that sample point. A 25 kHz signal sampled at 400 kHz would give 16 points per cycle. Equation 7 shows the sequence of numbers.

EQUATION 7:

$$Q(n) = x(n) \times \cos\left(2 \times \pi \times \frac{n}{16}\right)$$

Of course, the cosine terms can be precalculated. In this case, the series would have the values: 0.000, 0.383, 0.707, 0.924, 1.000, 0.924, 0.707, 0.383, 0.000, -0.383, -0.707, -0.924, -1.0, -0.924, -0.707, -0.383, 0.000. The DSP core of the dsPIC DSC can efficiently calculate these product terms; however, it is the high rate with which the data arrives that causes more problems.

A useful technique is to use fs/4 frequency translation. This is a complicated term to describe a simple mathematical trick. If instead of sampling at 400 kHz we only sample at 4x the carrier frequency, 100 kHz in this case, then there will only be 4 points in each of the reference signal sequences. The sequence of numbers to multiply for I is then (1, 0, -1, 0) and Q is (0, -1, 0, 1). Consequently, the frequency translation performed by the PSD is reduced to a sequence of moves and negations without requiring any multiplications saving an entire processing step.

It is now possible to perform the mixing as the data is being collected rather than waiting until a complete batch of data has been collected. Additionally, since the sample rate is now 100 kHz, the FIR filtering and decimation can also take place in between batches of samples being collected without stalling the sampling. Effectively every sample point in the original signal is processed with none being omitted.

Faster Still

The general purpose `FIRDecimate` routine provided by the dsPIC DSC libraries is designed to operate on generic data sets with relatively unrestricted data sizes. Therefore, if it is passed 60 input values and decimated by a factor of 10, 6 output samples will be generated. This can be improved upon by applying additional restrictions on the incoming data. If it is assumed that the number of input values to the function is equal to the decimation factor rather than calculating multiple outputs, the new data can just be written into the delay buffers and a single pass of the FIR filter will generate one output value.

A final enhancement involves the FIR filters themselves. It can be seen that alternating samples in the I and Q data sets will have the value '0' and will not be affected by the FIR filter tap weights at those sample points, and will not be accumulated into new output values. By mathematically analyzing the behavior of the FIR filters, it is possible to deduce that if the zero value entries are discarded, and the remainder passed through a filter designed for half the original sampling frequency, the output will be identical. In other words, by only storing the alternating non-zero elements, a filter designed for a sampling rate of 50 kHz can be used.

The reduction in effective sampling rate is important since it will require many fewer taps to achieve the desired low-pass response. By reducing the number of taps, the group delay of the filter can be reduced thereby improving the system response. Alternately, the length of the filter can be kept at a similar number but the shape of its response curve can be sharpened.

The output of the system for a unit step input can be seen in Figure 5, where the continuous mode curves represent the data from the improved algorithm. While it has a slower response, the overall performance and results are much improved over the first version of the software.

CONCLUSION

The digital lock-in amplifier is a useful tool for measuring small signals. By translating the signal measurement to a high frequency, it is possible to avoid noise introduced at DC and low frequencies.

Since it is possible to detect both amplitude and phase changes using the lock-in amplifier, it is possible to measure signal changes caused by devices with complex impedances, such as capacitive sensors.

When implementing any DSP algorithm, it is important to understand the fundamental processes involved; however, in addition, it is necessary to consider how the chosen processor architecture can best be used to arrive at an optimal solution. The dsPIC33F is a powerful digital signal controller and its capabilities are well suited to both the signal generation and processing tasks in this application. The high-speed ADC and DMA allow for a high data throughput, while the efficient DSP engine can perform the multiple filtering stages with ease.

The supplied source code (see **Appendix A: "Source Code"**) can easily be modified by the reader to perform measurements in similar applications where high accuracy signals are required at low final output rates.

REFERENCES

Lyons, R., "*Understanding Digital Signal Processing*", Prentice Hall, ISBN 0131089897

Microchip Technology Inc., "*dsPIC30F/33F Programmer's Reference Manual*" (DS70157)

Microchip Technology Inc., "*dsPIC® DSC Language Tools Libraries*" (DS51456)

APPENDIX A: SOURCE CODE

The the libraries and source files associated with this application note are available for download as a single archive file from the Microchip corporate Web site at:

www.microchip.com

NOTES:

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