



Using the C30 Compiler to Interface Serial EEPROMs with dsPIC33F

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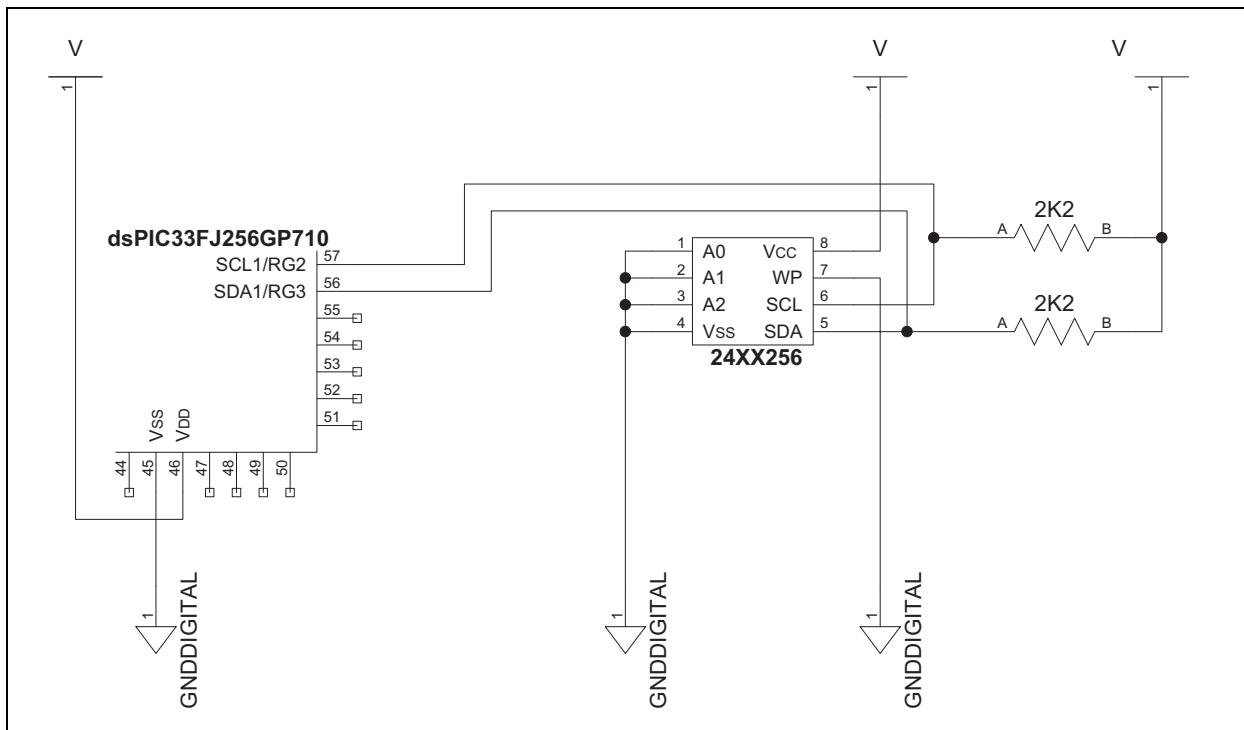
INTRODUCTION

The 24XXX series serial EEPROMs from Microchip Technology are I²C™ compatible and have maximum clock frequencies ranging from 100 kHz to 1 MHz. The I²C module available on the dsPIC33F family of Digital Signal Controllers (DSC) provides a very easy-to-use interface for communicating with the 24XXX series devices. However, there are instances when the Hardware Peripheral cannot be used.

This application note is intended to serve as a reference for communicating with Microchip's 24XXX series of serial EEPROMs using the dsPIC33F family of devices when the I²Cx module is not available. This applications note describes a software implementation to use any two I/O pins for I²C Communications. Source code for common data transfer modes is also provided. The source code is easily transferable to the PIC24 family of devices.

Figure 1 describes the hardware schematic for the interface between Microchip's 24XXX series devices and the dsPIC33F DSC. The schematic shows the connections necessary between the DSC and the serial EEPROM as tested, and the software was written assuming these connections, however, they may be changed in the final application. The SDA pin is switched between an output and a digital input so a pull-up resistor is required to VCC (typically 10 kΩ for 100 kHz, and 2 kΩ for 400 kHz and 1 MHz). The SCL pin is a driven output, however, it is recommended to use a pull-up to ensure correct operation. Also, the WP pin is tied to ground because the write-protect feature is not used in the examples provided.

FIGURE 1: CIRCUIT FOR dsPIC33F AND 24XXX SERIES DEVICE



FIRMWARE DESCRIPTION

The purpose of the firmware is to show how to generate specific I²C transactions using software and standard I/O Pins on a dsPIC® DSC. The focus is to provide the designer with a strong understanding of communication with the 24XXX series serial EEPROMs using software implemented I²C. The firmware was written in C language using the C30 compiler. The code can easily be modified to use any of the I/O pins available in the application.

No additional libraries are required with the provided code. The firmware consists of two .c files (main.c, i2c_Func.c and i2c.h), organized into nine sections:

- Initialization
- Low Density Byte Write
- Low Density Byte Read
- Low Density Page Write
- Low Density Sequential Read
- High Density Byte Write
- High Density Byte Read
- High Density Page Write
- High Density Sequential Read

The program also includes the Acknowledge polling feature for detecting the completion of write cycles after the byte write and page write operations. Read operations are located directly after each write operation, thus allowing for verification that the data was properly written. No method of displaying the input data is provided, but an oscilloscope or a Microchip MPLAB® ICD 2 could be used.

The code was tested using the 24LC256 serial EEPROM. This device features 32K x 8 (256 Kbit) of memory and 64-byte pages. The 24LC256 also features a configurable, 3-bit address via the A2, A1 and A0 pins. For testing, these pins were all grounded for a chip address of '000'. Oscilloscope screen shots are labeled for ease in reading. The data sheet version of the waveforms are shown below the oscilloscope screen shots. All timings are designed to meet the 100 kHz specs, and an 8 MHz crystal oscillator is used to clock the dsPIC DSC. If a faster clock is used, the code must be modified for the SSP module to generate the correct clock frequency. All values represented in this application note are hex values unless otherwise noted. The firmware for this application note was developed using the Explorer 16 Development Board with the dsPIC33FJ256GP710 device.

INITIALIZATION

In order to configure the dsPIC33F for software I²C, the TRIS bits for the I/O pins on the used port should be set accordingly (Examples in C using RG2 as SCL and RG3 as SCL).

SCL pin should be set for Output:

TRISGbits.RG2 = 0;

SDA Pin should be set for Input:

TRISGbits.RG3 = 1;

Byte Write

The Byte Write operation has been broken down into the following components: the Start condition and control byte, the word address, and the data byte and Stop condition. Note that, due to the size of the 24LC256, two bytes are used for the word address. However, 16 Kb and smaller 24XXX series devices use only a single byte for the word address.

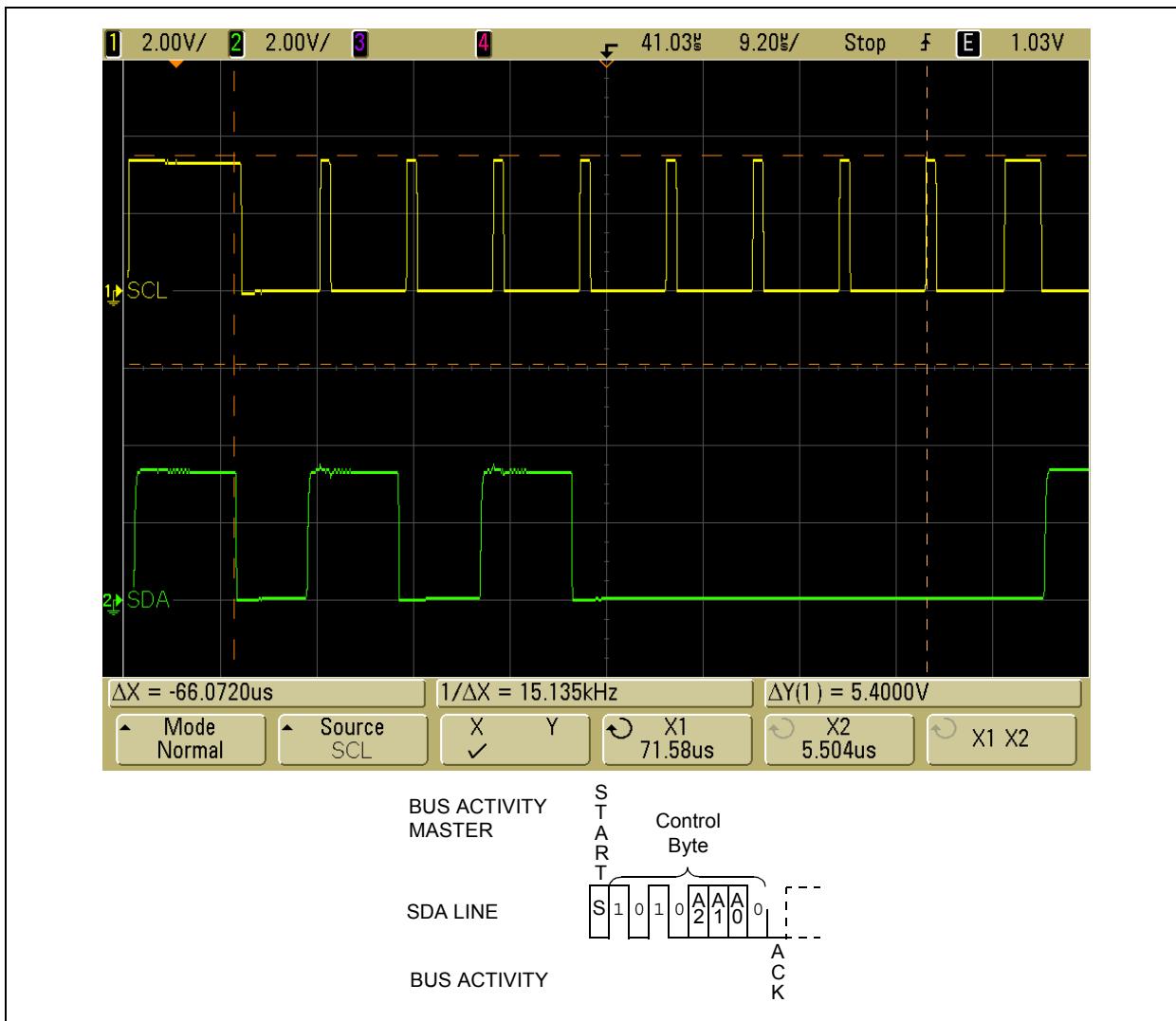
All I²C commands must begin with a Start condition. This consists of a high-to-low transition of the SDA line while the clock (SCL) is high. After the Start condition, the 8 bits of the control byte are clocked out, with data being latched in on the rising edge of SCL. The device code (0xA for the 24LC256), the block address (3 bits), and the R/W bit make up the control byte. Next, the EEPROM device must respond with an Acknowledge bit by pulling the SDA line low for the ninth clock cycle.

After the Start bit has been sent, the control byte can be transmitted. A function called byteout() is provided to send 8-bits of data onto the bus. This function is called as part of many of the High-Level functions.

Start Bit and Control Byte Transmission

Figure 2 shows the details of the Start condition and the control byte. The left marker shows the position of the Start bit, whereas the right marker shows the ACK bit.

FIGURE 2: START BIT AND CONTROL BYTE



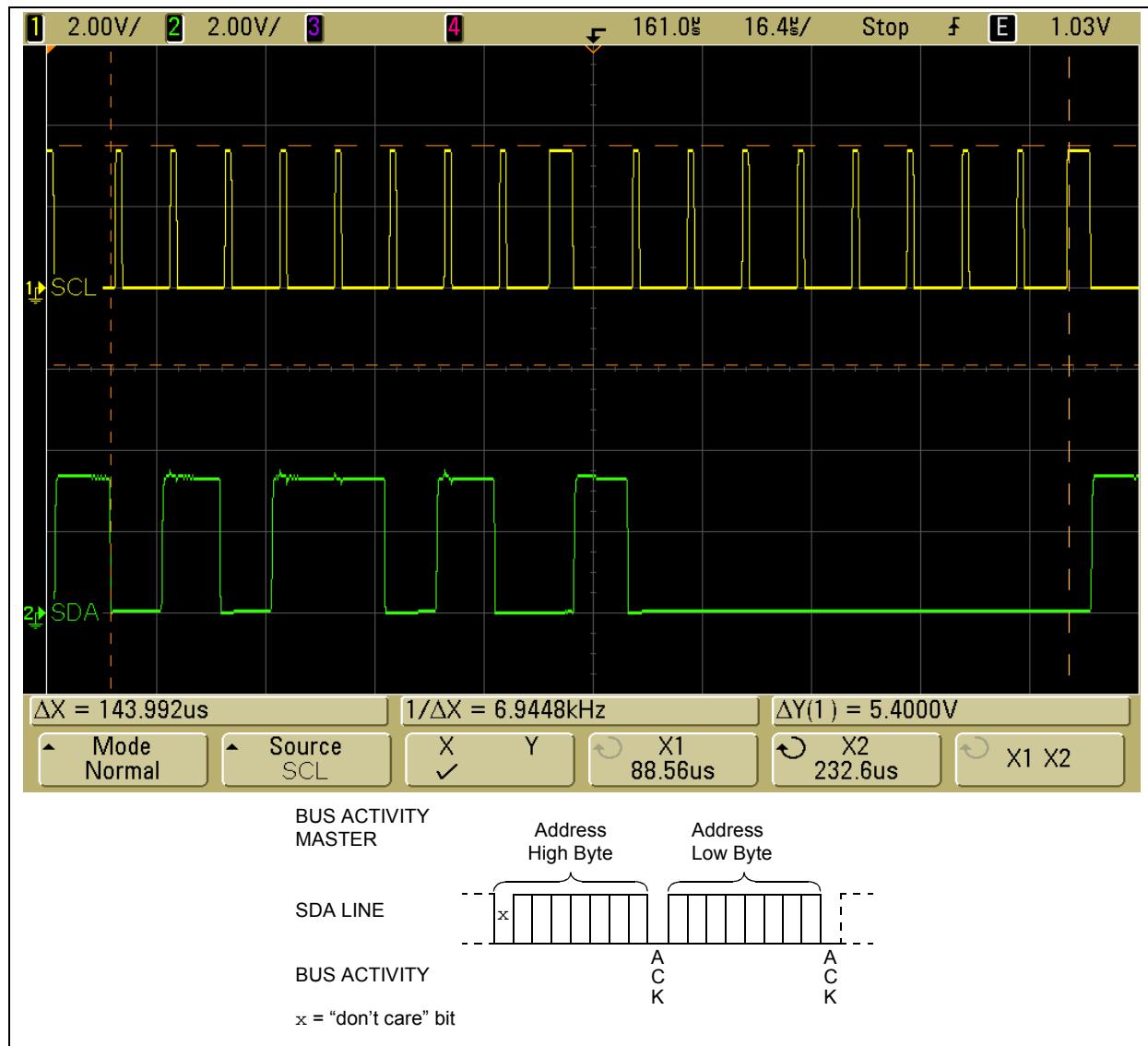
Sending the Word Address

After the EEPROM device has acknowledged receipt of the control byte, the master (dsPIC33F) begins to transmit the word address. For the 24LC256, this is a 15-bit value, so two bytes must be transmitted for the entire word address (the MSb of the high byte is a “don’t care”), with the Most Significant Byte sent first (note that 16 Kb and smaller 24XXX series devices only use a 1-byte word address).

After each byte of the word address has been transmitted, the slave device must respond with an Acknowledge bit.

Figure 3 shows the two address bytes and corresponding ACK bits. For reference, the previous ACK bit (in response to the control byte) is shown by the left marker. Note that the word address chosen for this application note is 0x5A00.

FIGURE 3: WORD ADDRESS

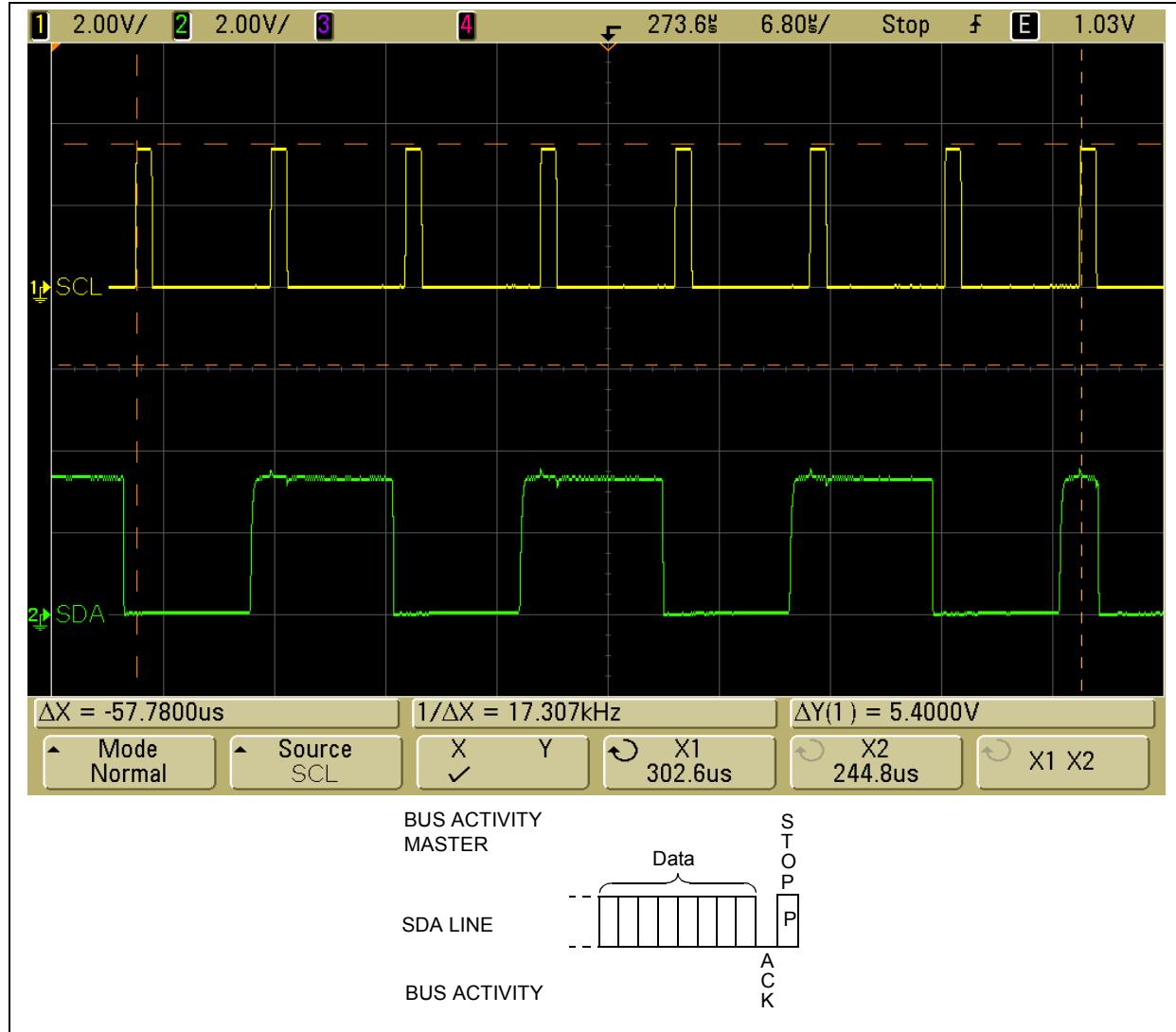


Data Byte and Stop Bit Transmission

Once the word address has been transmitted and the last ACK bit has been received, the data byte can be sent. Once again, the EEPROM device must respond with another ACK bit. After this has been received, the master generates a Stop condition. This consists of a low-to-high transition of SDA while the clock (SCL) is high. Initiating a Stop condition is done by calling bstop() function.

Figure 4 shows the transmission of the data byte, as well as the Stop condition indicating the end of the operation. The right marker denotes the Stop condition.

FIGURE 4: DATA BYTE AND STOP BIT



ACKNOWLEDGE POLLING

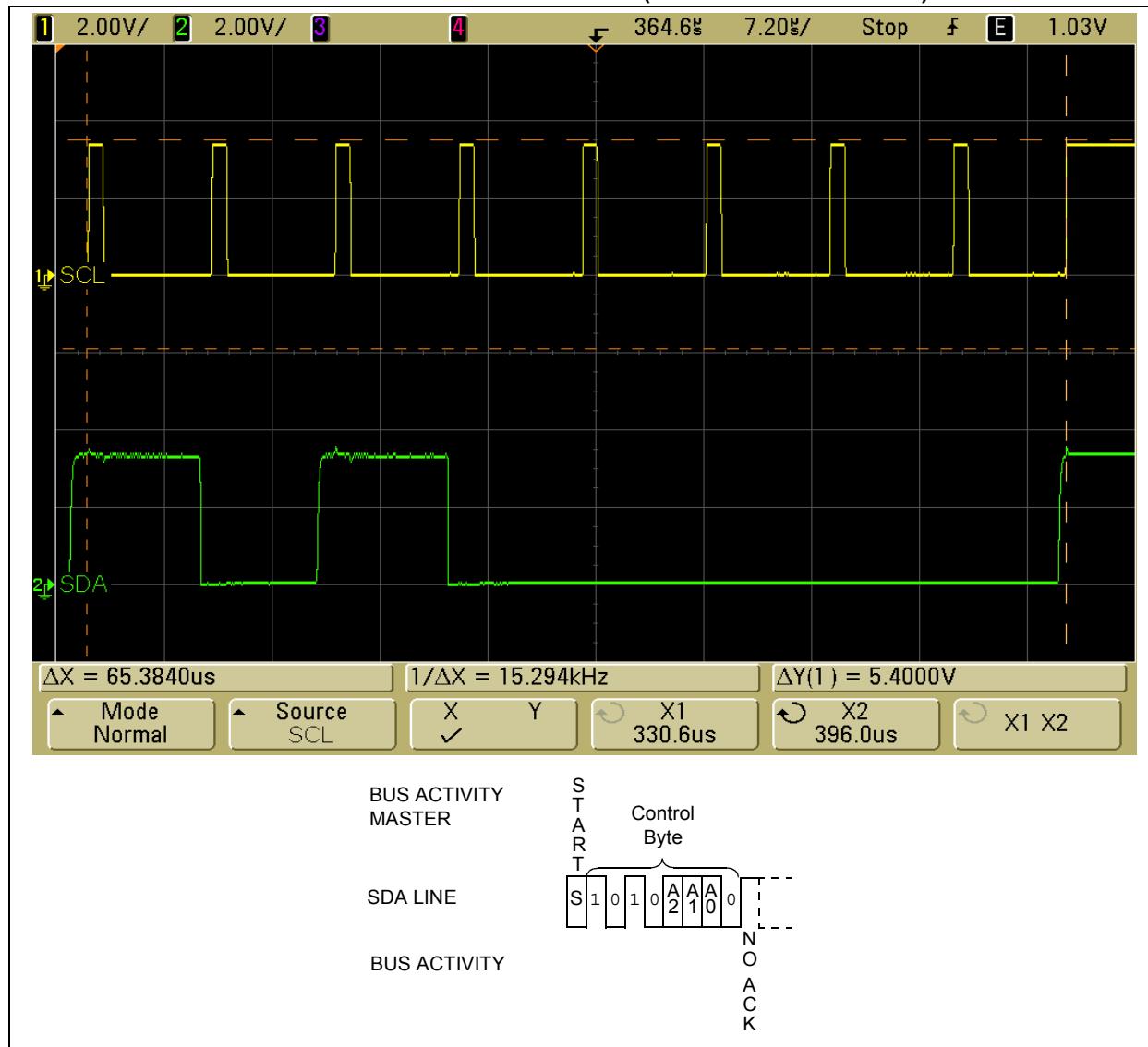
The data sheets for the 24XXX series devices specify a write cycle time (T_{WC}), but the full time listed is not always required. Because of this, using a measured write cycle delay is not always accurate, which leads to wasted time. Therefore, in order to transfer data as efficiently as possible, it is highly recommended to use the Acknowledge polling feature. Since the 24XXX series devices will not acknowledge during a write cycle, the device can continuously be polled until an Acknowledge is received. This is done after the Stop condition takes place to initiate the internal write cycle of the device.

Acknowledge Polling Routine

The process of Acknowledge polling consists of sending a Start condition and then a Write command to the EEPROM device, then simply checking to see if the ACK bit was received. If it was not received, then the device is still performing its write cycle.

Figure 5 shows an example of Acknowledge polling to check if a write operation has finished. In this example, the device did not acknowledge the poll (the ACK bit is high), which indicates that the write cycle has not yet completed.

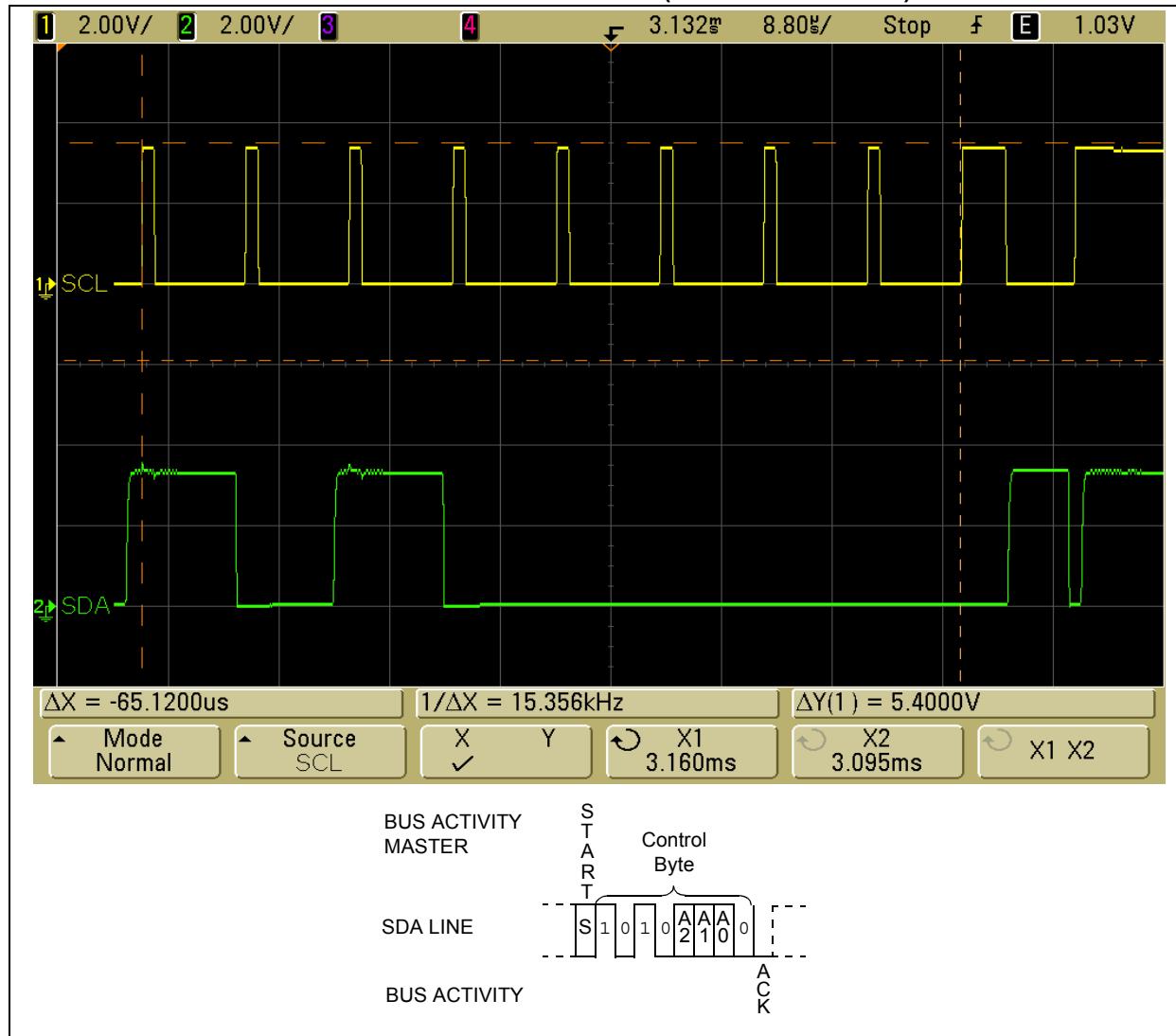
FIGURE 5: ACKNOWLEDGE POLLING ROUTINE (SHOWING NO ACK BIT)



Response to Acknowledge Polling

Figure 6 shows the final Acknowledge poll after a write operation, in which the device responds with an ACK bit, indicating that the write cycle has completed and the device is ready to continue.

FIGURE 6: ACKNOWLEDGE POLLING FINISHED (SHOWING ACK BIT)



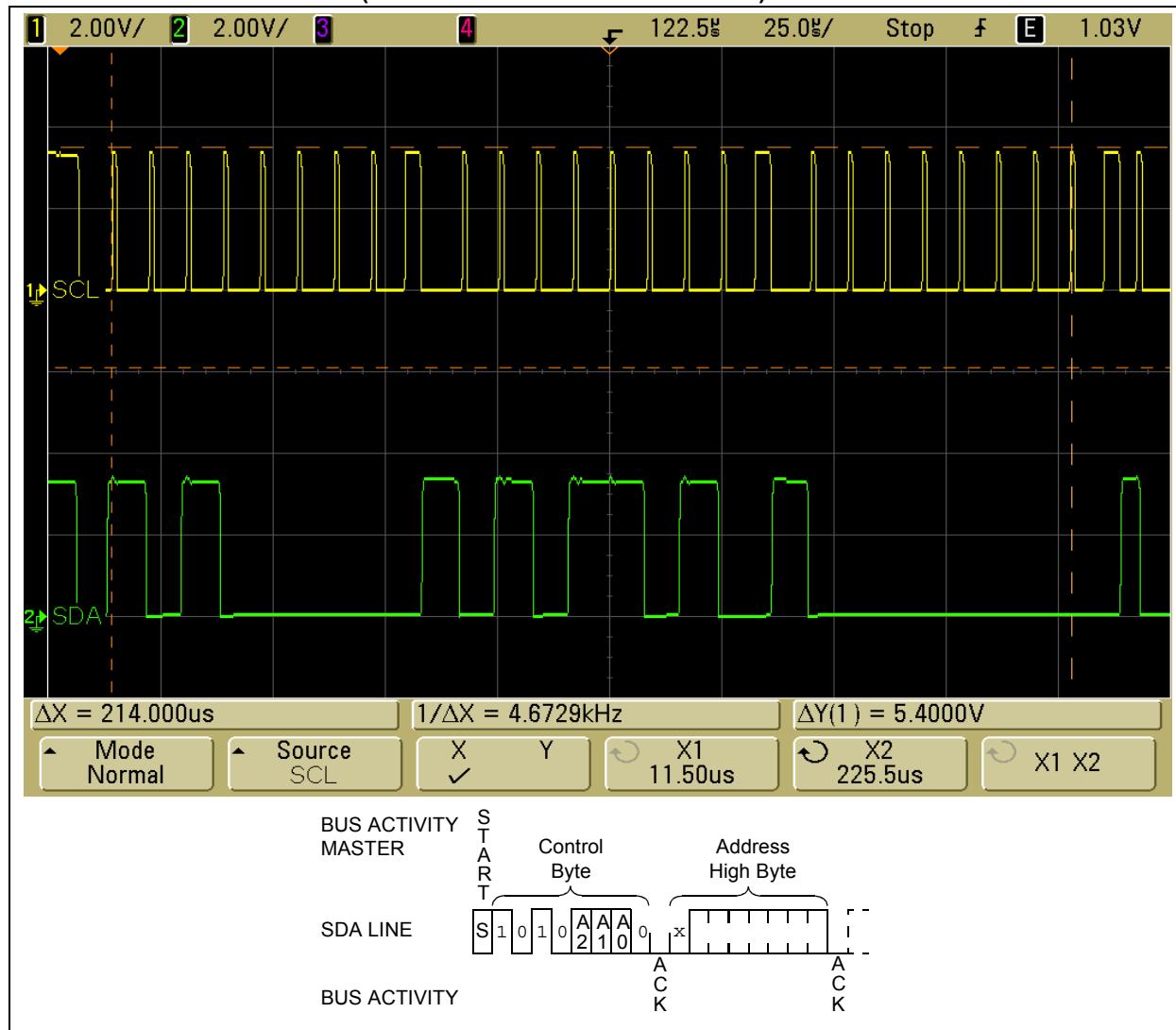
BYTE READ

The byte read operation can be used in order to read data from the 24XXX series devices in a random access manner. It is similar to the byte write operation, but slightly more complex. The word address must still be transmitted, and to do this, a control byte with the R/W bit set low must be sent first. However, this conflicts with the desired operation, that is, to read data. Therefore, after the word address has been sent, a new Start condition and a control byte with R/W set high must be transmitted. Note that a Stop condition is not generated after sending the word address.

Writing Word Address for Read

Figure 7 shows an example of the first control byte and the word address of a byte read operation. The left marker indicates the Start bit and the right marker indicates the ACK bit after receipt of the word address (0x5A00 in this example). Once again, the R/W bit must be low in order to transmit the word address.

FIGURE 7: BYTE READ (CONTROL BYTE AND ADDRESS)

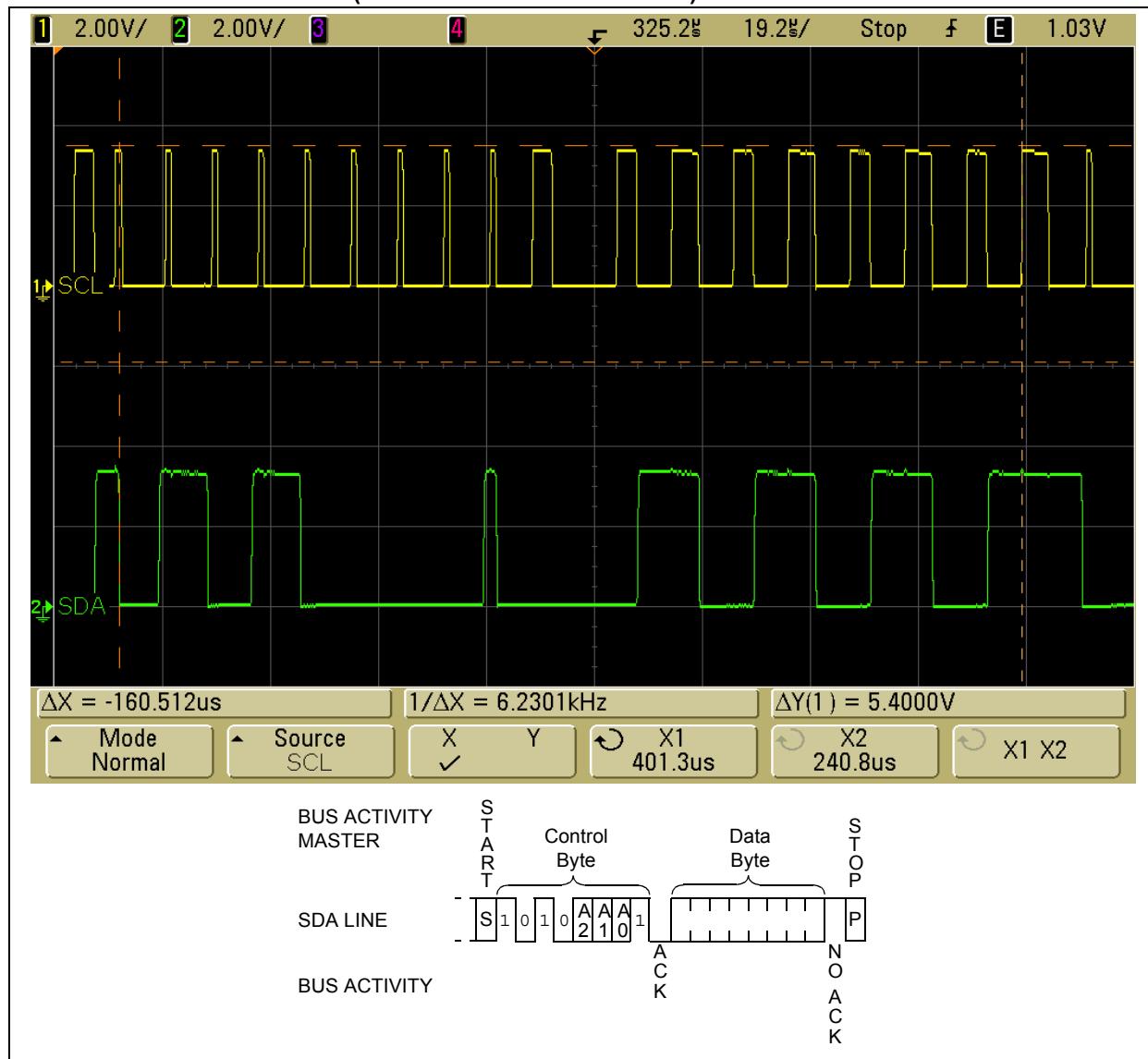


Reading Data Byte Back

After the word address has been transmitted, the bstart() function is used to initiate a Restart condition. Note that a Restart is very similar to a Start, except that a Restart does not first check for a valid bus condition (this is important since either SCL or SDA may be low at this point, which would cause an error during an attempted Start condition). The second control byte (with the R/W bit set) is then transmitted as normal. This is not an issue with the bstart() function as this does not check the bus first.

Figure 8 shows the control byte and data byte during the actual read part of the operation. A Restart condition is generated immediately after receipt of the previous ACK bit and is marked with the left marker. At the end of the transfer, the master indicates that no more data will be read by the use of the NO ACK bit (holding SDA high in place of an ACK bit); this is shown by the right marker. After the NO ACK bit has been sent, the master generates a Stop condition to end the operation.

FIGURE 8: BYTE READ (CONTROL BYTE AND DATA)



PAGE WRITE

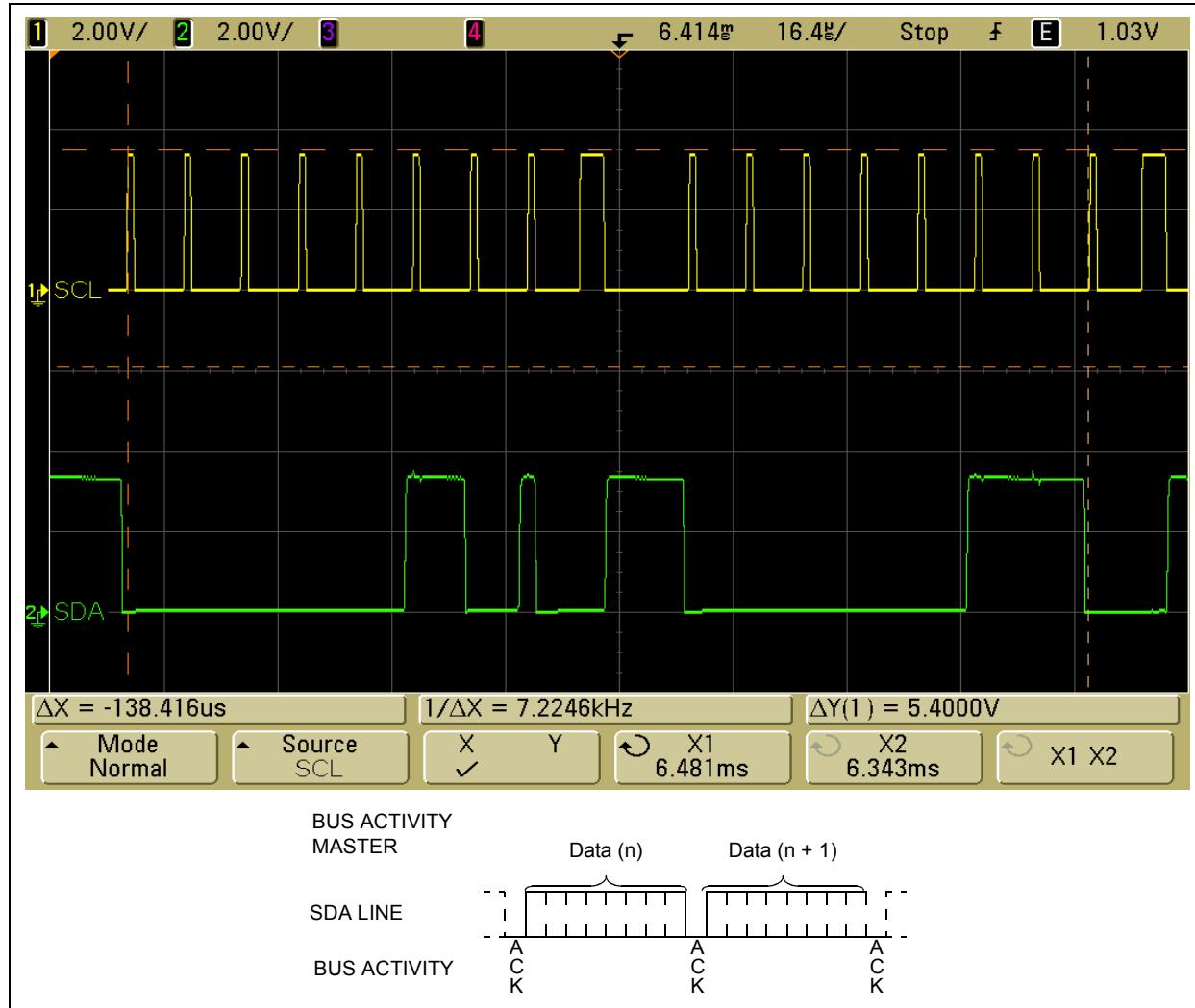
A very useful method for increasing throughput when writing large blocks of data is to use page write operations. All of the 24XXX series devices, with the exception of the 24XX00, support page writes, and the page size varies from 8 bytes to 128 bytes. Using the page write feature, up to 1 full page of data can be written consecutively with the control and word address bytes being transmitted only once. It is very important to point out, however, that page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses which are integer multiples of the page size, and end at addresses which are [integer multiples of the page size] minus 1. Any attempts to write across a page boundary will result in the data being wrapped back to the beginning of the current page, thus overwriting any data previously stored there.

The page write operation is very similar to the byte write operation. However, instead of generating a Stop condition after the first data byte has been transmitted, the master continues to send more data bytes, up to 1 page total. The 24XXX will automatically increment the internal Address Pointer with receipt of each byte. As with the byte write operation, the internal write cycle is initiated by the Stop condition.

Sending Multiple Bytes Successively

Figure 9 shows two consecutive data bytes during a page write operation. The entire transfer cannot be shown legibly due to length, but this screen shot shows the main difference between a page write and a byte write. Notice that after the device acknowledges the first data byte (0x05 in this example), the master immediately begins transmitting the second data byte (0x06 in this example).

FIGURE 9: PAGE WRITE (TWO CONSECUTIVE DATA BYTES)



SEQUENTIAL READ

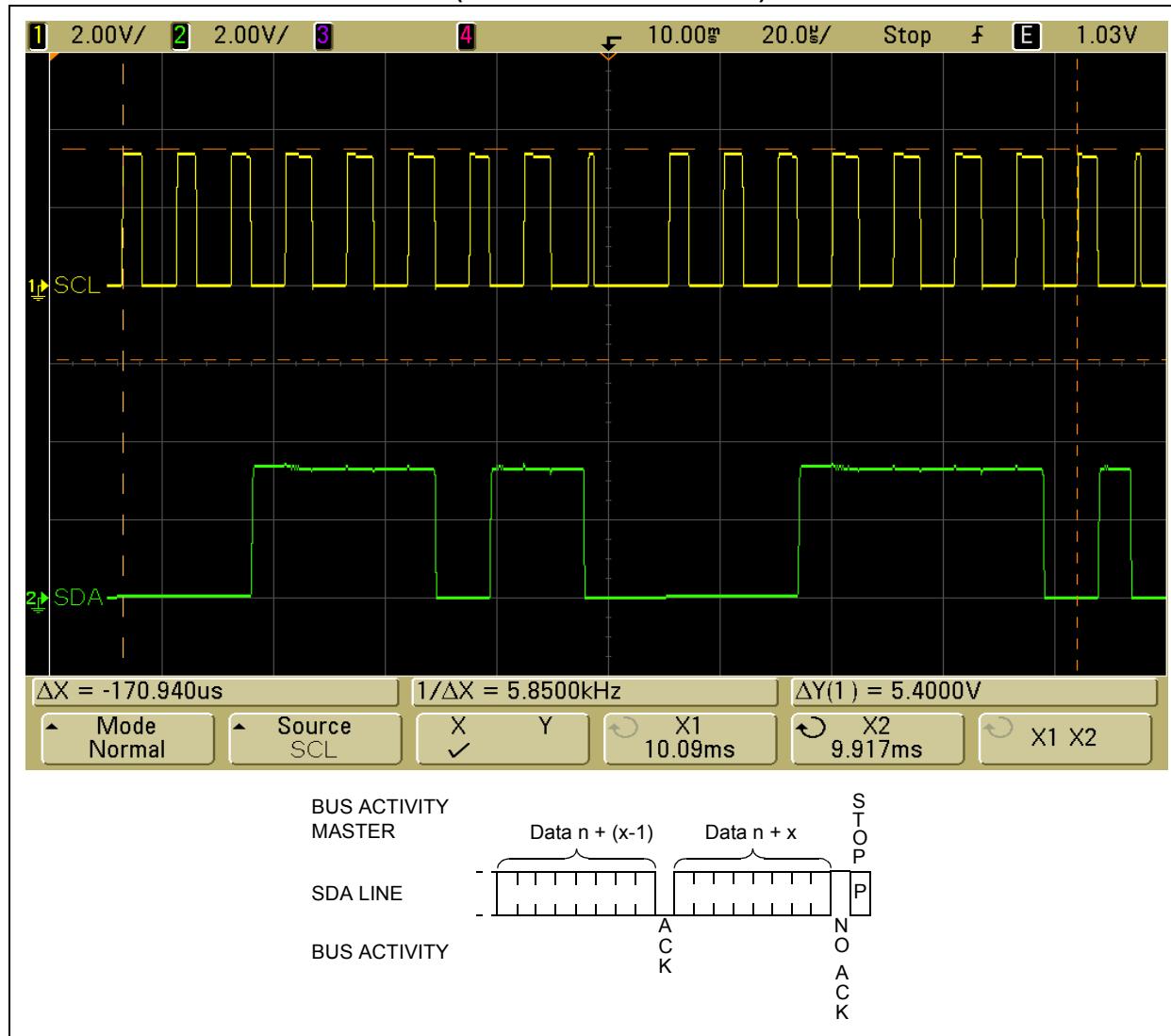
Just as the page write operation exists to allow for more efficient write operations, the sequential read operation exists to allow for more efficient read operations. While the page write is limited to writing within a single physical page, the sequential read operation can read out the entire contents of memory in a single operation.

The sequential read operation is very similar to the byte read operation, except that the master must pull SDA low after receipt of each data byte to send an Acknowledge bit back to the 24XXX series device. This ACK bit indicates that more data is to be read. As long as this ACK bit is transmitted, the master can continue to read back data without the need for generating Start/Stop conditions or for sending more control/word address bytes.

Reading Data Bytes Successively

Figure 10 shows the last two bytes of a 16-byte sequential read operation. Note that the master pulls SDA low to transmit an ACK bit after the first data byte, but leaves SDA high to transmit a NO ACK bit after the final data byte. And as with all other operations, a Stop condition is generated to end the operation.

FIGURE 10: SEQUENTIAL READ (LAST TWO DATA BYTES)



CONCLUSION

When communicating with the 24XXX series EEPROM devices, there are many benefits of using a software method of I²C communicating. One of the obvious advantages is that any two I/O pins can be used. In most cases speed is not an issue so a software method offers a good compromise between speed and flexibility.

This application note illustrated the main characteristics of I²C communications with Microchip's 24XXX series serial EEPROM devices with the use of the dsPIC33F. The C30 code provided is highly portable and can be used with only minor modifications on the PIC24 family of microcontrollers and dsPIC30F DSC. The code was tested on Microchip's Explorer 16 Demonstration Board with the connections shown in Figure 1.

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NOTES:

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