MICROCHIP

AN1069

Using C30 Compiler and the SPI Module to Interface EEPROMs with dsPIC33F and PIC24F

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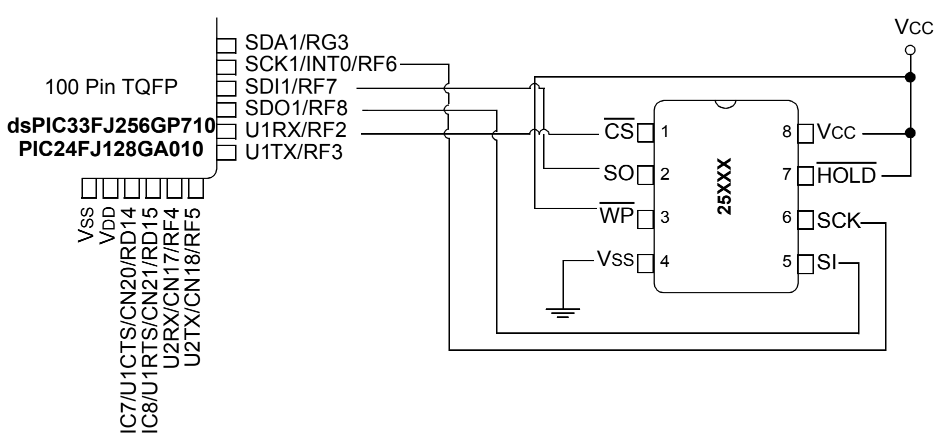
INTRODUCTION

The 25XXX series serial EEPROMs from Microchip Technology are SPI compatible and have maximum clock frequencies ranging from 3 MHz to 20 MHz. The SPI module available on dsPIC33F Digital Signal Controller and PIC24F microcontroller provide a very easy-to-use interface for communicating with the 25XXX series devices. The largest benefit of using the SPI module is that the signal timings are handled through hardware rather than software. This allows the firmware to continue executing while communication is handled in the background. This also means that an understanding of the timing specifications associated with the SPI protocol is not required in order to use the 25XXX series devices in designs.

This application note is intended to serve as a reference for communicating with Microchip's 25XXX series serial EEPROM devices with the use of the SPI module featured on many dsPIC33F and PIC24F family devices. Source code for common data transfer modes is also provided.

Figure 1 describes the hardware schematic for the interface between Microchip's 25XXX series devices and the dsPIC33F DSC or the PIC24F MCU. The schematic shows the connections necessary between either controller and the serial EEPROM as tested, and the software was written assuming these connections. The $\overline{\text{WP}}$ pin is tied to VCC because the STATUS register write-protect feature is not used in the examples provided.

FIGURE 1: CIRCUIT FOR dsPIC33FJ256GP710, PIC24FJ128GA010 AND 25XXX SERIES DEVICE



Note: $\overline{\text{CS}}$, $\overline{\text{WP}}$ and $\overline{\text{HOLD}}$ pins should all have pull-up resistors (~10k-ohms).

FIRMWARE DESCRIPTION

The purpose of the program is to show individual features of the SPI protocol and give code samples of the opcodes so that the basic building blocks of a program can be shown. The firmware was written in C and the Microchip C30 compiler was used. The opcodes used in the program are Write Enable (WREN), Write, Read, and Read Status Register (RDSR) (used in the program for WIP polling). The oscilloscope pictures have markers that are shown from $\overline{CS}$ enable to $\overline{CS}$ disable for ease in reading. The data sheet version of the waveform is below the actual oscilloscope picture. The SPI module is set up for Mode 0,0 operation. The code is written in modules and commented so changing modes, speeds, and modifying commands such as sequential reads and page writes is simple. The values represented in this application note are all hex values unless otherwise noted.

Besides the standard SPI libraries supplied with the C30 compiler, the firmware consists of two .c files (AN1069.c and AN1069_spi.c), organized into nine sections.

- Initialization
- Low Density Byte Write
- Low Density Byte Read
- Low Density Page Write
- Low Density Page Read
- High Density Byte Write
- High Density Byte Read
- High Density Page Write
- High Density Page Read

The low density routines are intended for use with the 4K and smaller density devices that use only one byte of address (25XX010A, 25XX020A, and 25XX040A) 1, 2, and 4 Kbit devices. The Most Significant bit (A8) for the 25XX040A device resides in the control code, please refer to the individual data sheet for particulars. The high density routines are intended for use with 8 Kbit and higher density devices that use two bytes of address. This program also exhibits the WIP polling feature for detecting the completion of write cycles after the byte write and page write operations. Read operations are located directly after each write operation, thus allowing for verification that the data was properly written. No method of displaying the input data is provided, but a SEEVAL® 32 evaluation system, an oscilloscope, or a Microchip MPLAB® ICD 2 could be used.

The code was tested using a 25LC256 serial EEPROM. This device features 32k x 8 (256 Kbit) of memory and 64-byte pages.

INITIALIZATION

In order to configure the SPI module for SPI mode `0,0`, several key registers on the dsPIC33F DSC or PIC24F MCU need to be properly initialized.

SPI1STAT STATUS Register (SPI1STAT)

SPI1STAT holds all of the Status bits associated with the SPI module. The SPI Enable bit (SPIPEN) must be set in order to enable the serial port.

SPI1 Control Register (SPI1CON1)

SPI1CON1 is one of the Configuration registers for the SPI module. In SPI mode `0,0`, the SMP bit of the register needs to be set for data to be sampled at the end of the output time. The Clock Polarity Select bit (CKP) needs to be cleared for Idle state of the clock to be a low level. The MSTEN bit needs to be set for “Master” mode. Finally, the Secondary Prescale bits (SPRE) and the Primary Prescale bits (PPRE) are configured, in this case, 2:1 (Secondary) and 1:1 (Primary). SPI1CON2 is used for “framed” SPI support, is not used in the code here and, therefore, is cleared during initialization.

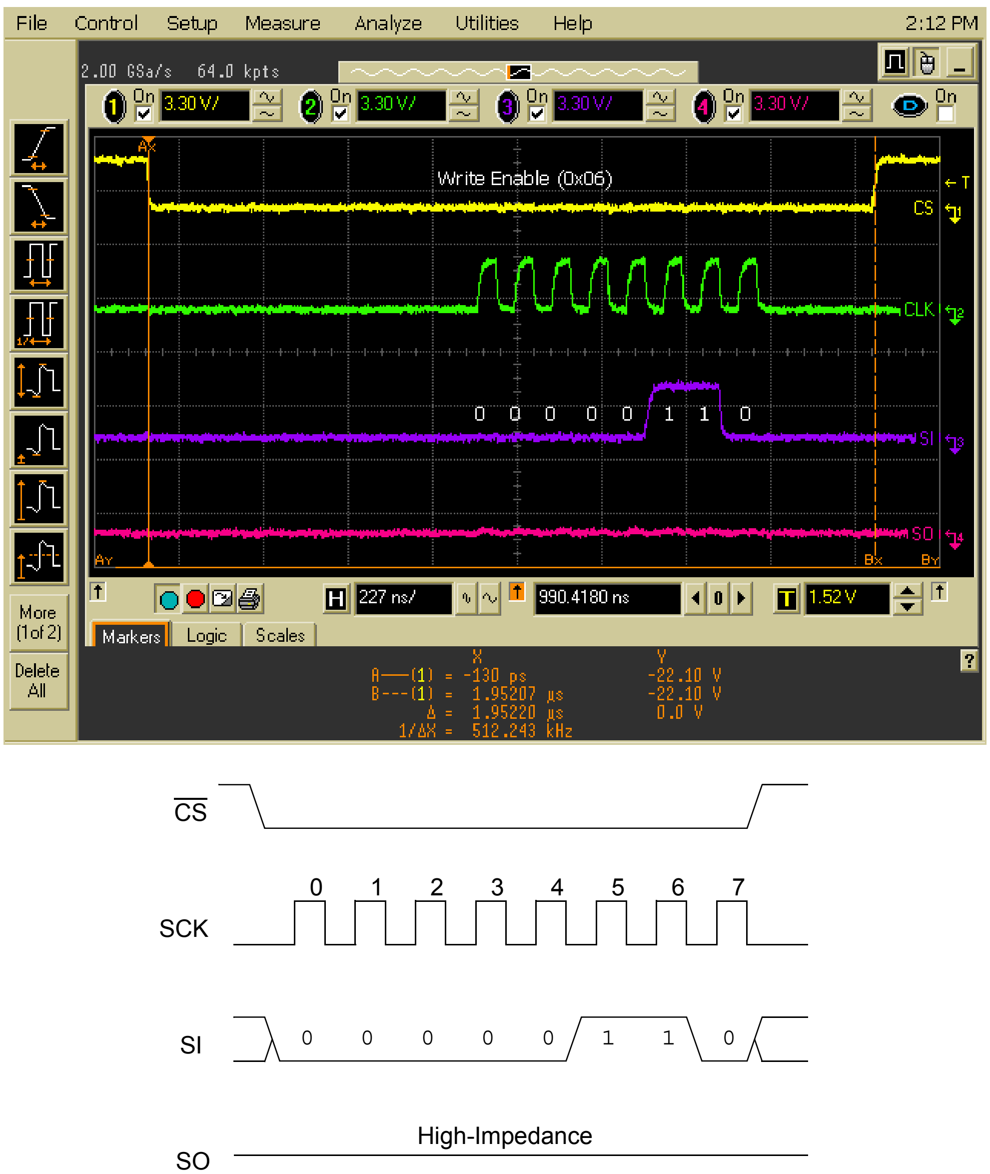
TRISF Register

In order to be properly controlled the $\overline{\text{CS}}$ pin must be configured as an output. This is done by setting the respective bit in TRISF to ‘`0`’ for output. The SCK, SDI and SDO pins will automatically be configured when the SPI Enable bit is set.

WRITE ENABLE

Figure 2 shows an example of the Write Enable command. Chip Select is brought low (active) and the opcode is sent out through the SPI port. The Write Enable command must be given before a write is attempted to either the array or the STATUS register. The WEL bit can be cleared by issuing a Write Disable command (WRDI) or it is automatically reset if the device is powered down or a write cycle is completed.

FIGURE 2: WRITE ENABLE (WREN)

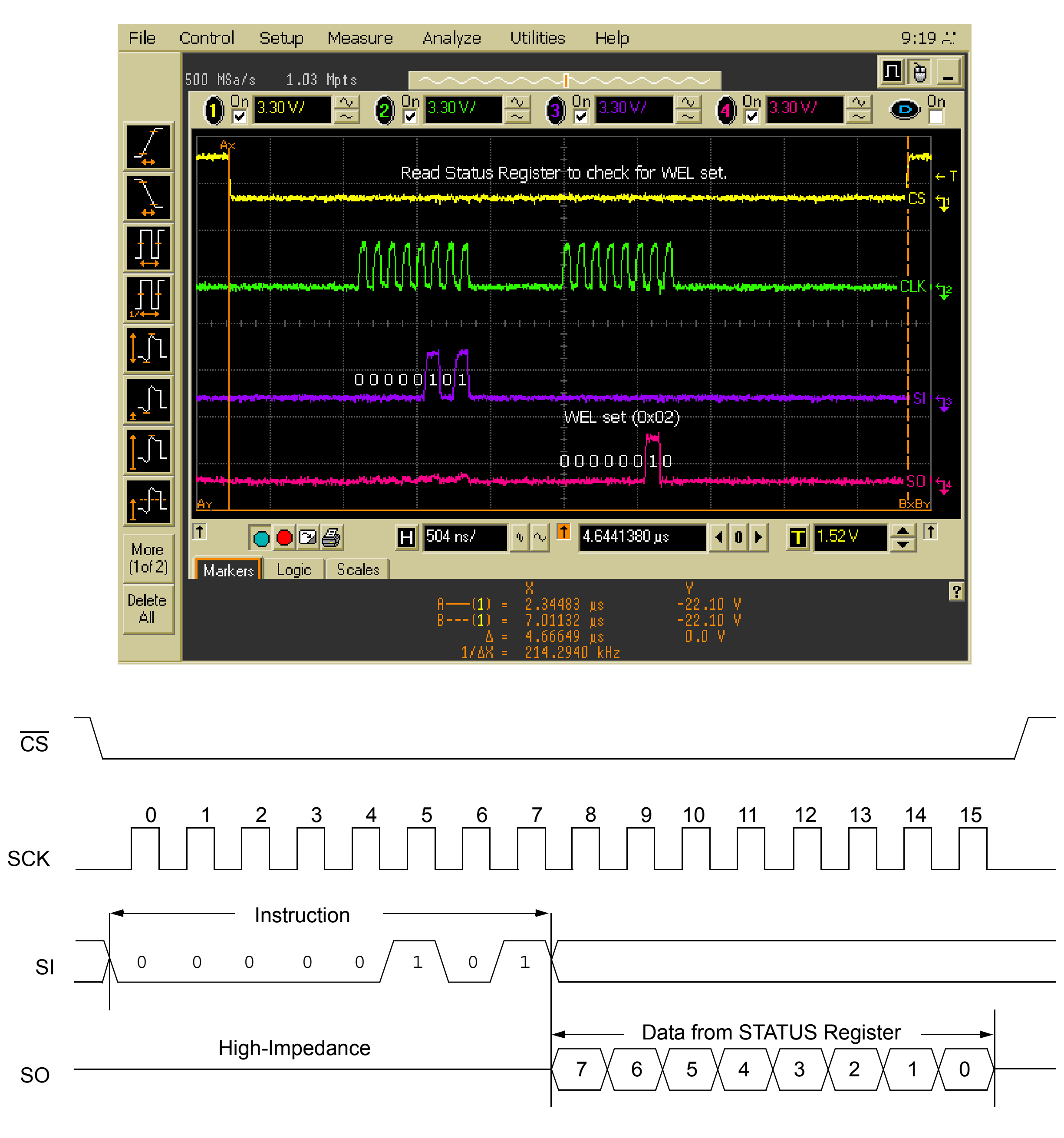


READ STATUS REGISTER TO CHECK FOR WEL BIT

Figure 3 shows an example of the Read Status Register command to check for the WEL bit. The WEL bit must be set before a write is attempted to either the STATUS register or the array. It is good programming practice to check whether this bit is set before attempting the write.

Once again the device is selected and the opcode, 0x05, is sent. The STATUS register is shifted out on the Serial Out pin. A value of 0x02 shows that the WEL bit in the STATUS register has been set. The device is now ready to do a write to either the STATUS register or the array.

FIGURE 3: READ STATUS REGISTER TO CHECK FOR WEL BIT (RDSR)

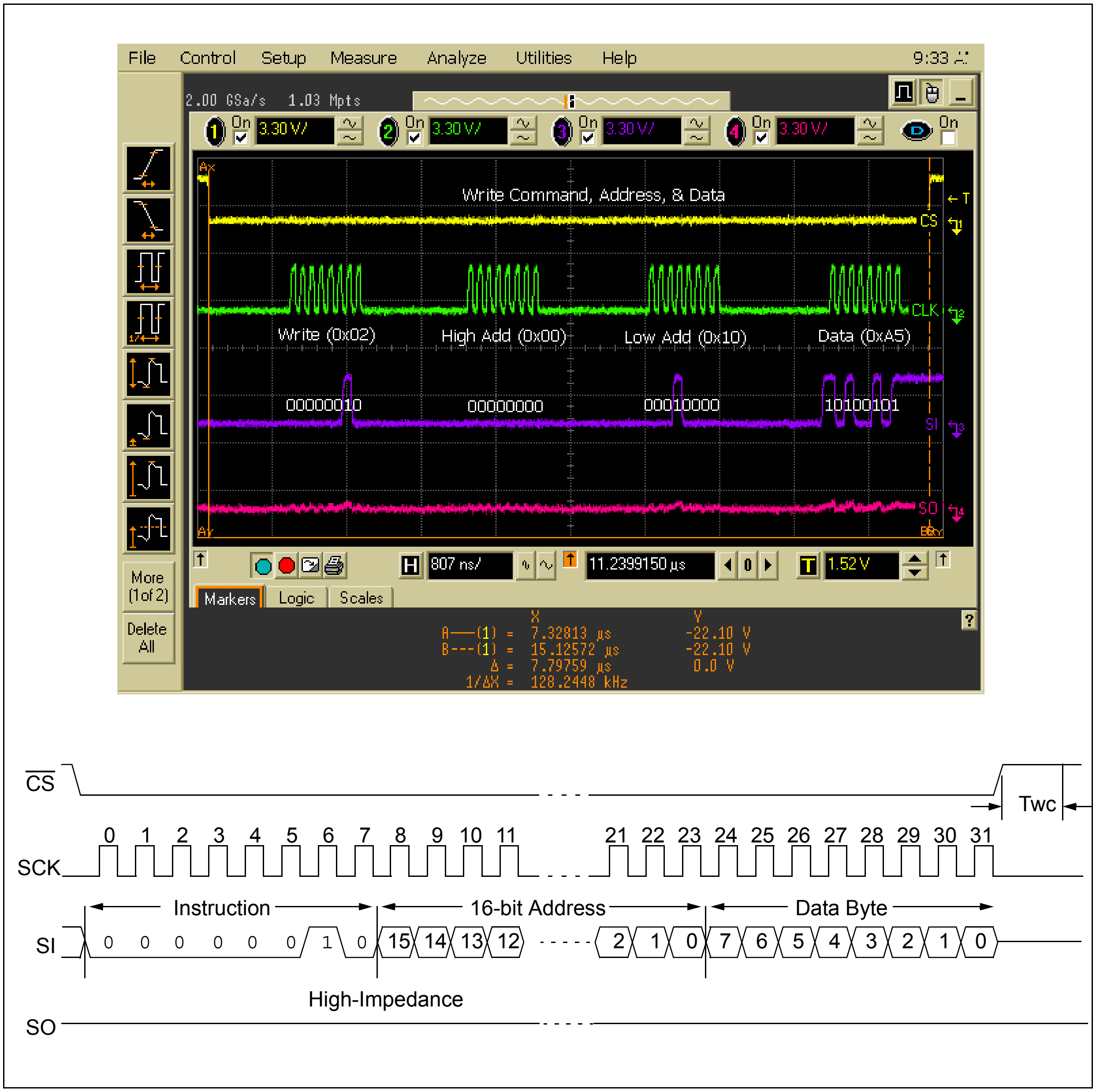


BYTE WRITE COMMAND (OPCODE, ADDRESS AND DATA)

Figure 4 shows an example of the Write command. For this, the device is selected and the opcode, 0x02, is sent. The High Address byte is given 0x00, followed by the Low Address byte, 0x10. Finally, the data is clocked in last, in this case, 0xA5. Once the Chip Select is toggled at the end of this command, the internal write cycle is initiated. Once the internal write cycle has begun, the WIP bit in the STATUS register can now be polled to check when the write finishes or a delay needs to be added (~5ms), if the WIP bit is not being polled. This code uses WIP polling.

A page write can be accomplished by continuing to give data bytes to the device without toggling $\overline{CS}$. Up to one full page (64 bytes for the 25XX256) can be written before a write cycle is needed. Once $\overline{CS}$ is brought high after the data bytes have been transmitted, then the write cycle timer will begin and normal polling can be initiated. The included page write function programs all 64 bytes of data in the first page. Since the starting address is 0x0010, the last 16 bytes of data will wrap from address 0x003F to address 0x0000 and complete the page. Caution should be taken when initiating writes in this manner so that previously stored data doesn't get overwritten.

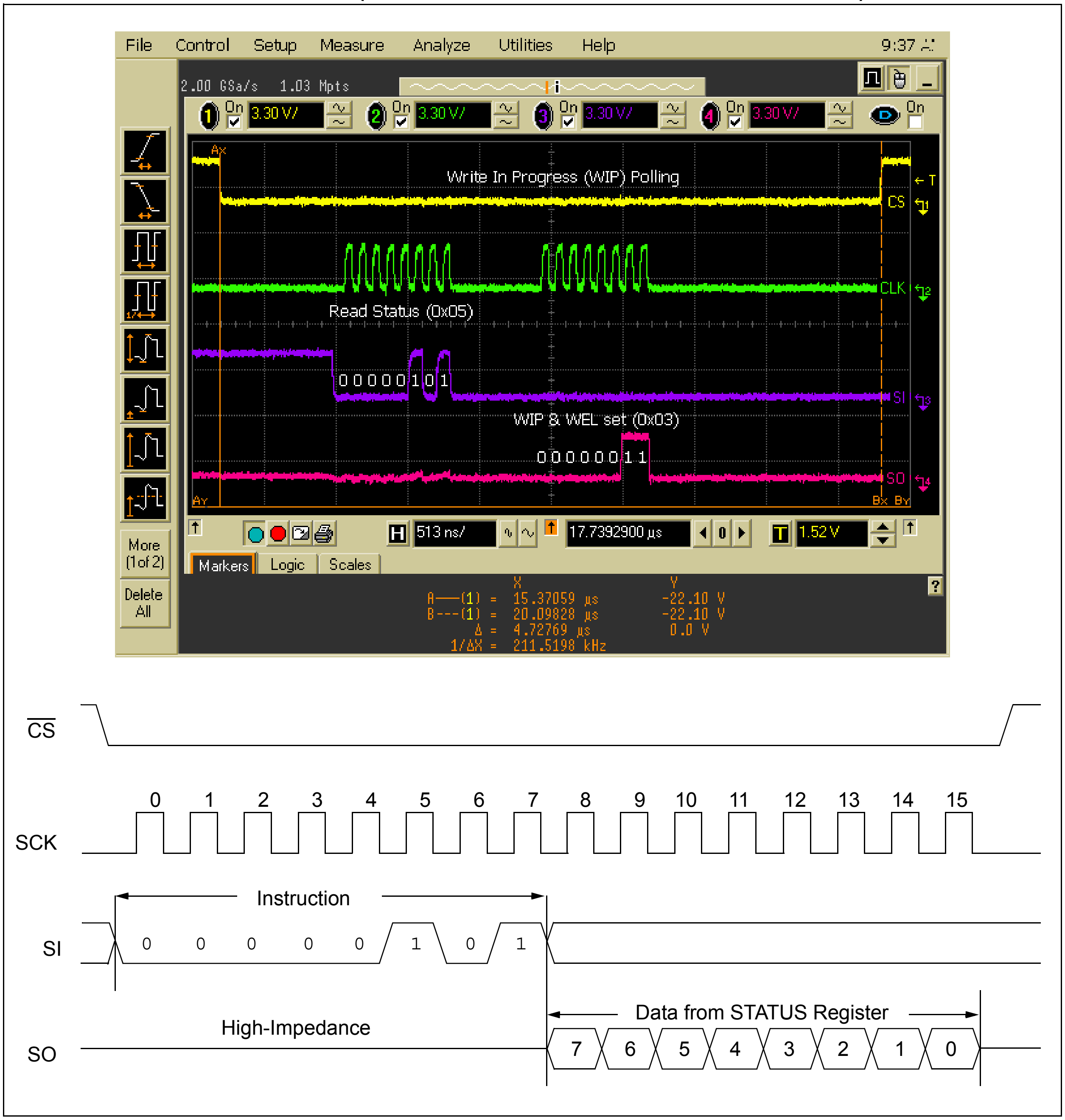
FIGURE 4: BYTE WRITE COMMAND, ADDRESS AND DATA



DATA POLLING (RDSR – CHECK FOR WIP SET)

After a valid Write command is given, the STATUS register can be read to check if the internal write cycle has been initiated, and it can continuously be monitored to look for the end of the write cycle. In this case, the device is selected and the opcode, 0x05, is sent. The STATUS register is then shifted out on the Data Out pin, resulting in a value of 0x03. Figure 5 shows that both the WEL bit (bit 1) and the WIP bit (bit 0) are set, meaning the write cycle is in progress.

FIGURE 5: DATA POLLING (READ STATUS REGISTER TO CHECK WIP BIT)

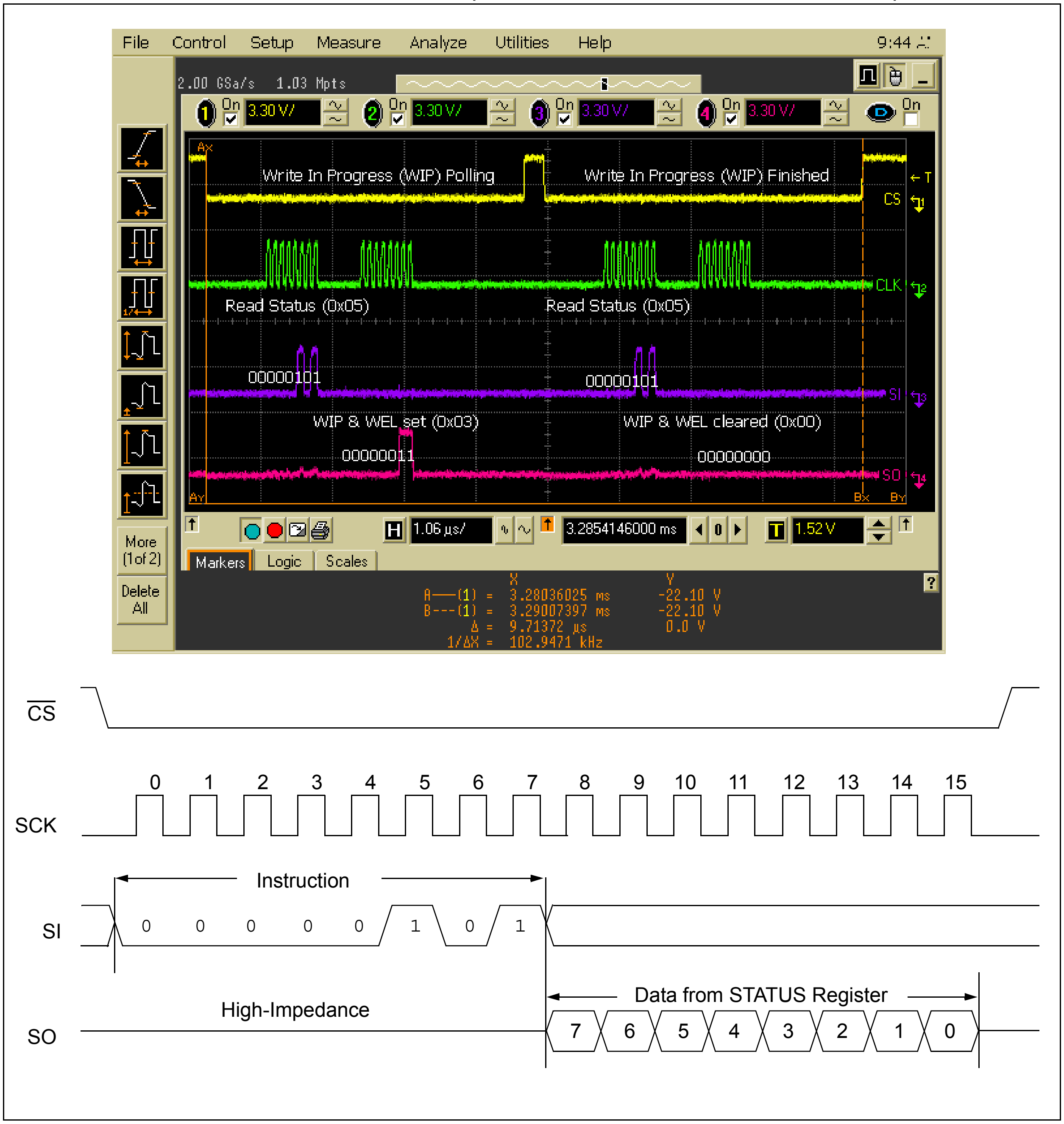


DATA POLLING FINISHED (RDSR – WIP BIT CLEARED)

The part remains in a continuous RDSR loop and the WIP status is evaluated until the bit is cleared. Figure 6 shows the Status Register Read command followed by a value of 0x00 being shifted out on the Data Out pin.

This indicates that the write cycle has finished and the device is now ready for additional commands. The WEL bit is also cleared at the end of a write cycle, which serves as additional protection against unwanted writes.

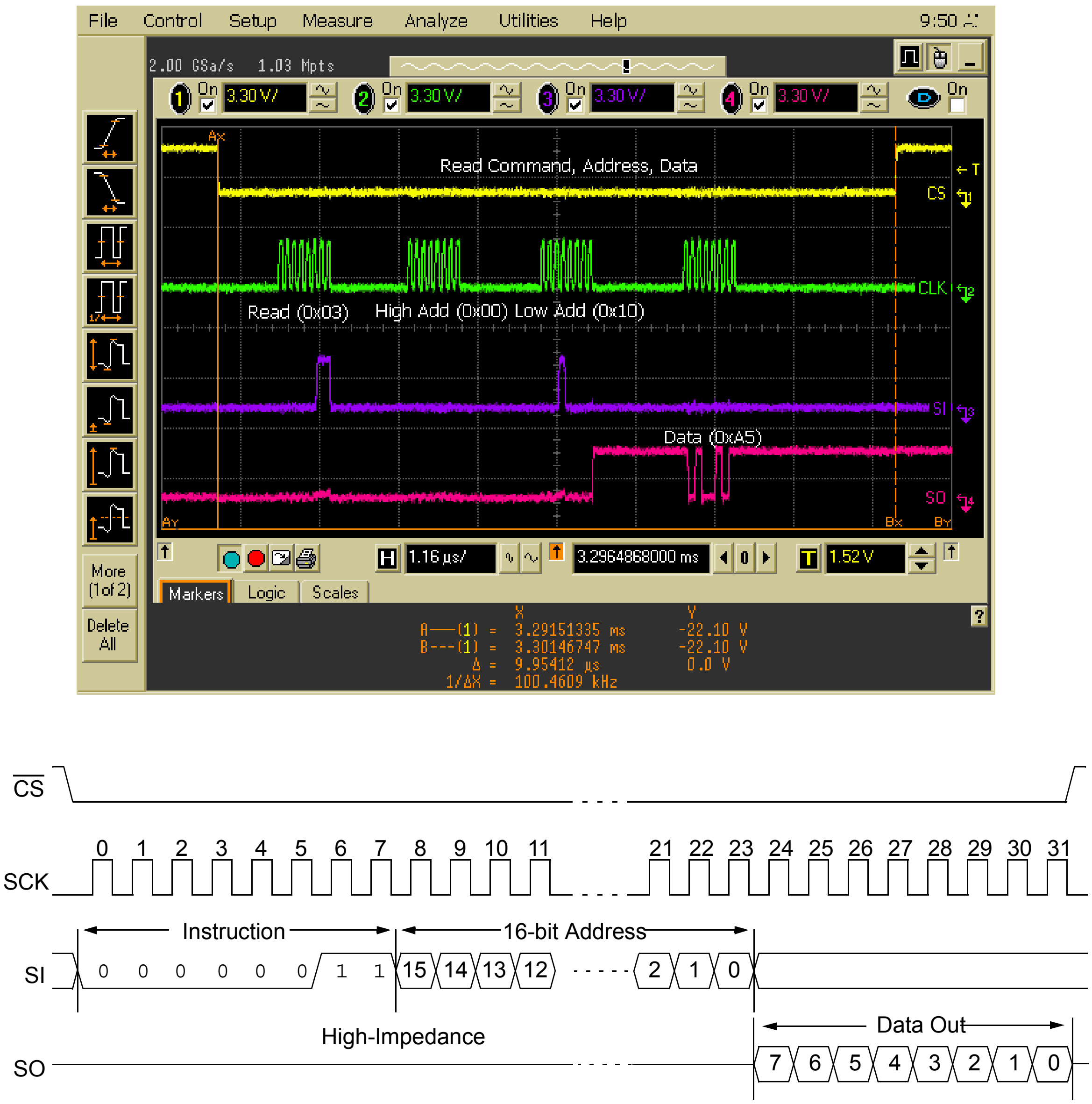
FIGURE 6: DATA POLLING FINISHED (RDSR – WIP AND WEL BITS CLEARED)



READ COMMAND (OPCODE, ADDRESS AND DATA)

Figure 7 shows an example of the Read command. For this, the device is selected and the opcode, 0x03, is sent. The High Address byte is given 0x00, followed by the Low Address byte, 0x10. Finally, the data is clocked out on the Serial Out pin, in this case, 0xA5. In order to do a sequential read, more clocks need to be generated. It is possible to read the entire chip by continuing to provide clocks to the device. Once the end of the array is reached, the data will wrap to the beginning of the array (Address 0x0000) and keep reading out until $\overline{CS}$ is deselected or clocks stop being provided.

FIGURE 7: READ COMMAND, ADDRESS AND DATA



CHANGING PROCESSORS

This application note code was written to simplify changing between processors. There are, however, a couple of steps that need to be taken in order to do this. This application note was tested with two specific processors, the dsPIC33FJ256GP710 and the PIC24FJ128GA010. If you are going to use processors that are different from these two, please consult the device-specific data sheet to check for any other potential issues when using this code. As mentioned previously, the Explorer 16 development board was used for this application note with the connections shown in Figure 1. In order to change between these processors there are four steps:

1. The current processor module currently on the Explorer 16 board must be physically replaced with the processor module desired. Be sure to disconnect power during this procedure.
2. The #define statements on lines 30 and 31 in the an1096.h file must be commented in/out for the desired processor.
3. The new processor needs to be selected in the MPLAB® IDE by going to Configure>Select Device...
4. The linker file needs to be added/removed for the desired processor. If this is not done, it will not prevent the code from compiling but will remove some undesired warnings from the compiler.

CONCLUSION

These are some of the basic features of SPI communications using the SPI module on one of Microchip’s dsPIC33F devices. The code is highly portable and can be used on many devices that have the SPI module with very minor modifications. Using the code provided, designers can begin to build their own SPI libraries to be as simple or complex as needed. The code was tested on Microchip’s Explorer 16 Development Board with the connections shown in Figure 1.

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