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Recommended Usage of Microchip Microwire Serial EEPROM Devices

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INTRODUCTION

The majority of embedded control systems require nonvolatile memory. Because of their small footprint, byte level flexibility, low I/O pin requirement, low-power consumption, and low cost, serial EEPROMs are a popular choice for nonvolatile storage. Microchip Technology has addressed this need by offering a full line of serial EEPROMs covering industry standard serial communication protocols for two-wire (I^2C™), three-wire (Microwire), and SPI communication. Serial EEPROM devices are available in a variety of densities, operational voltage ranges, and packaging options.

In order to achieve a highly robust application when utilizing serial EEPROMs, the designer must consider more than just the data sheet specifications.
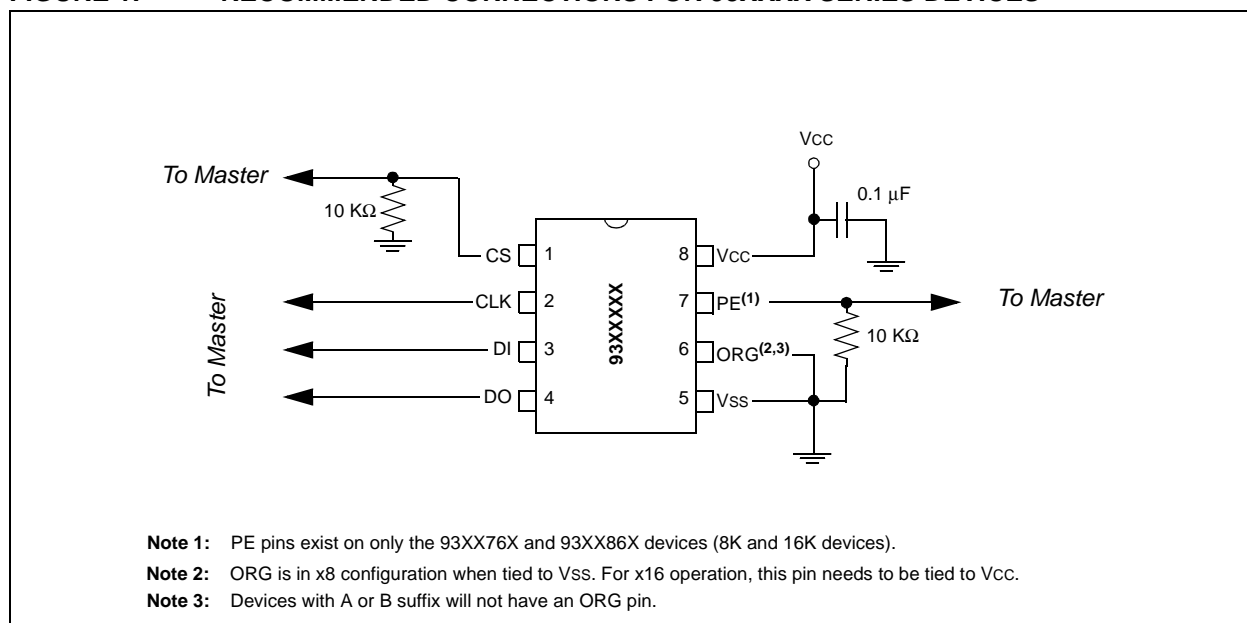
There are a number of conditions which could potentially result in nonstandard operation. The details of such conditions depend greatly upon the serial protocol being used.

This application note provides assistance and guidance with the use of Microchip Microwire serial EEPROMs. These recommendations are not meant as requirements; however, their adoption will lead to a more robust overall design. The following topics are discussed:

• Chip Select and Program Enable Inputs
• Proper Write Sequence
• Resetting the State Machine
• Using a Hardware SPI port for Microwire communication
• Tying DI and DO together
• Power-up/Power-down

Figure 1 shows the suggested connections for using Microchip Microwire serial EEPROMs. The basis for these connections will be explained in the sections which follow.

FIGURE 1:   RECOMMENDED CONNECTIONS FOR 93XXXX SERIES DEVICES

Note 1:   PE pins exist on only the 93XX76X and 93XX86X devices (8K and 16K devices).
Note 2:   ORG is in x8 configuration when tied to Vss. For x16 operation, this pin needs to be tied to Vcc.
Note 3:   Devices with A or B suffix will not have an ORG pin.

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CHIP SELECT AND PROGRAM ENABLE INPUTS

During power-up and power-down routines, most microcontrollers have a period of time in which they float I/O lines before the processor is fully initialized. It is during this time that any external device controlled by the microcontroller may be able to recognize and react to spurious commands or line noise. Therefore, a pull-down resistor should be used on the CS line to keep the EEPROM de-selected during power-up/power-down cycles or any event where the EEPROM is not intended to be selected. Furthermore, a pull-down resistor should be used on the PE pin of the 93XX76X and 93XX86X devices to prevent any unwanted writes during similar power-up/power-down events.

PROPER WRITE SEQUENCE

Microwire serial EEPROMs do not give you the ability to monitor whether or not the device is enabled for writes. Also, the 1-4K Microwire devices do not have a Program Enable pin to allow hardware to control when writes are allowed. It is up to the user to control exactly when the device is able to be written to and also protect the device after a write has been completed. Therefore, a Write command should not be considered complete until the Erase/Write Disable (EWDS) command has been issued following a Write command. So, all Write commands should begin with an Erase/Write Enable (EWEN), followed by the desired write sequence, and end with an Erase/Write Disable (EWDS). The EWDS command cannot be issued during the write cycle, any commands issued while a write is in progress will be ignored by the device.

This practice has two benefits. First, it protects the device further against unwanted writes in the event of a Reset or other system interruption. Second, by issuing a Start bit at the beginning of the Erase/Write Disable command, the device will reset the Ready/busy status on the DO line and return the device to a true Standby mode where the device will consume its least amount of current.

RESETTING THE STATE MACHINE

A Reset of the state machine can be accomplished by deselecting the device as long as the required number of clock cycles for a given command has not been reached. However, once the required clock cycles have been met, the command will execute upon completion of that command even if additional clocks are given

after a valid command. Any additional clocks given to the device after a valid command are treated as "don't cares".

Additionally, if the device is suspected of having any type of power loss (POR or BOR) event, then once V_{CC} is restored, it is recommended that the CS line be toggled Low (inactive), High (Active), Low (inactive). This will allow for the state machine to have a better Reset and possibly be able to recover from a short or spurious power interruption. See Power-up/Power-down section for further details on POR/BOR events.

USING A HARDWARE SPI PORT FOR MICROWIRE COMMUNICATION

Many of today's popular Microcontrollers offer a module that can be used to send SPI commands. The Microwire structure is set up in such a manner that many of these hardware protocol ports can be used to control the Microwire protocol by setting up the module correctly. The particulars of how to set up the port depend greatly on manufacturer, individual data sheets should be referenced for details. Microchip has Application Notes available on how to set this up for PICmicro® Microcontrollers.

THEORY OF OPERATION

To use an SPI port (MSSP) to communicate with Microchip's Microwire Serial EEPROMs, the bytes to be output to the 93XXX must be aligned such that the LSB of the address is the 8th bit (LSB) of a byte to be output. From there the bits should fill the byte from right to left consecutively. If more that 8 bits are required, then two bytes will be required to be output. This same method will work for any 93XXX series device but the data sheet must be referenced for these because density and organization will change the number of bits sent for each command. We will use the 93LC66C organized in x16 format as an example below. Since more than 8 bits are required to control a 93LC66C, two consecutive bytes are required as shown in Figure 2.

High Byte (Where the Start bit, opcode bits and address MSb reside)

The High Byte is configured in the following format: SB is the Start bit. OP1 is the MSb of the op code and OP0 is the opcode LSb. The CS line can be set before the byte is output because the leading 0's output to the 93XXX prevent a Start bit from being recognized by the 93XXX until the first high bit is sent.

Low Byte (8 Address bits)

The Low Byte contains A7-A0, which are the address bits required to access 256 bytes in x16 mode.

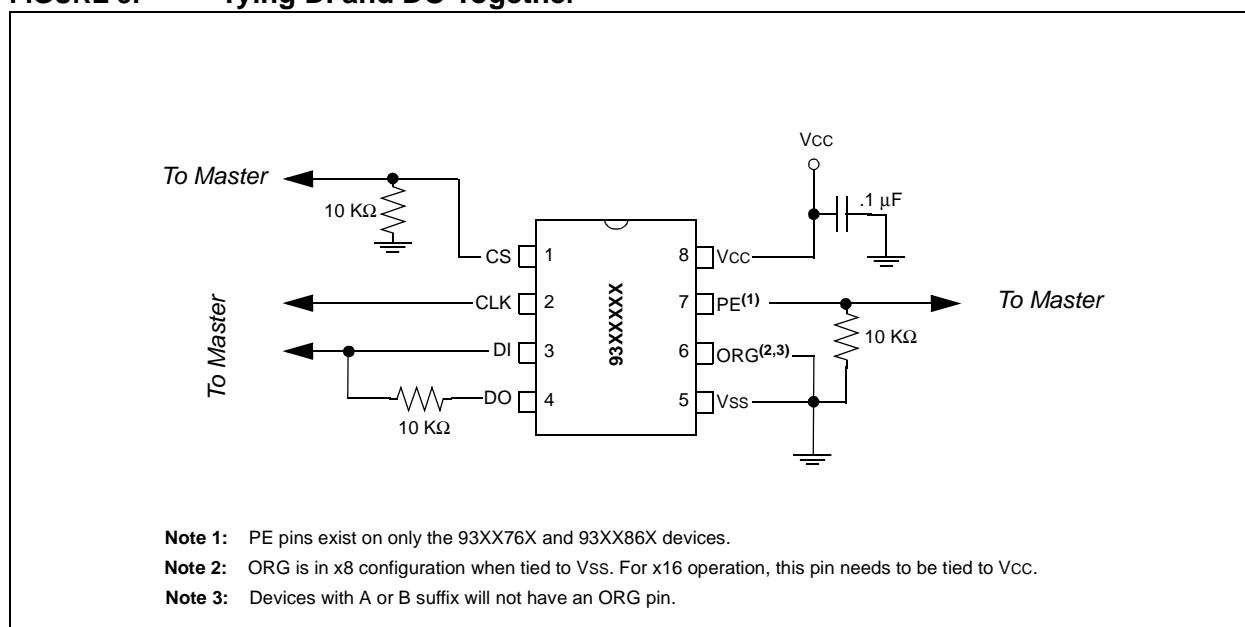### FIGURE 2: COMMAND ALIGNMENT

High Byte								Low Byte							
0	0	0	0	0	SB	OP1	OP0	A7	A6	A5	A4	A3	A2	A1	A0

TYING DI AND DO TOGETHER

Many customers inquire about making the Microwire protocol truly 3-wire by tying the DI and DO lines together. However, a potential for bus contention exists if the microcontroller attempts to drive the DI pin while the memory is driving DO. This is especially true when using an SPI port on the microcontroller and you rely on dummy zeros to be driven on the bus before the Start bit gets issued (since DO drives high for Ready until the next Start bit). To prevent this bus contention issue, it is necessary to use a series resistor (~10K Ohm) on the DO line from the DI line instead of a direct connection, as shown in Figure 3.

Another potential problem with tying DI and DO together occurs as CS is brought high after the write cycle has been initiated and valid clock transitions occur on the CLK line during the write cycle. This can cause the device to see an inadvertent Start condition when the write cycle ends (and the DO line drives high to signal the Ready state). This is caused by the fact that the T_{WC} of the device is variable (depending on process, voltage and temperature) and, therefore, causes the write cycle to end in an asynchronous fashion with respect to the clock. For example, if CS is high when the write cycle ends and DO goes high (thereby pulling DI high), then a low-to-high transition on the CLK will be seen as a valid Start condition when it may not have been intended to be a Start condition.

FIGURE 3: **Tying DI and DO Together**

Note 1: PE pins exist on only the 93XX76X and 93XX86X devices.
Note 2: ORG is in x8 configuration when tied to V_{SS}. For x16 operation, this pin needs to be tied to V_{CC}.
Note 3: Devices with A or B suffix will not have an ORG pin.

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POWER-UP/POWER-DOWN

Microchip serial EEPROMs feature a high amount of protection from unintentional writes and data corruption while power is within normal operating levels. But certain considerations should be made regarding power-up and power-down conditions to ensure the same level of protection during those times when power is not within normal operating levels.

Power Failure During a Write Cycle

During a write cycle, V_{CC} must remain above the minimum operating voltage for the entire duration of the cycle (typically 5 ms max. for most devices). If V_{CC} falls below this minimum at any point for any length of time, data integrity cannot be ensured. It will result in marginally programmed data that may or may not be correct. Furthermore, because the EEPROM cells were not able to be fully programmed, the device will have shorter data retention time than specified in the data sheet.

Power-Up

On power-up, V_{CC} should always begin at 0V and rise straight to its normal operating level to ensure a proper Power-on Reset. V_{CC} should not linger at an ambiguous level (i.e., below the minimum operating voltage).

Brown-Out Conditions

If V_{CC} happens to fall below the minimum operating voltage for the serial EEPROM, it is recommended that V_{CC} be brought down fully to 0V before returning to normal operating level. This will help to ensure that the device is reset properly.

Furthermore, if the microcontroller features a Brown-out Reset with a threshold higher than that of the serial EEPROM, bringing V_{CC} down to 0V will allow both devices to be reset together. Otherwise, the microcontroller may reset during communication while the EEPROM keeps its current state. In this case, a software Reset sequence would be required before beginning further communication.

CONCLUSION

Although not required for operation, utilizing these recommendations on Microwire Serial EEPROM designs will result in a more robust overall design. These recommendations fall directly in line with how Microchip designs, manufactures, qualifies and tests its Serial EEPROMs and will allow the devices to operate fully within the data sheet parameters.

QUESTION AND ANSWER

Q: What would happen if I inadvertently sent either too many or too few clocks during a Write command.

A: If you send too many clocks to the device and then drop the CS line to initiate the write cycle, the extra clocks will be ignored but the command will execute. If you do not send enough clocks and then drop the CS line, then the command will abort and no write will take place.

Q: I am using a 93LC56C device in my application and I am having problems getting it to work correctly. The read sequence seems to work fine, but I am unable to write any data to the part.

A: First, make sure you are issuing an EWEN command prior to attempting a write. But a problem such as this is usually caused by either not giving the part the required number of bits for the command before dropping the CS line or by not dropping the CS line at all. The Write command will not commence until the CS line is brought low.

Q: I am confused, do I have to toggle the CS line low in-between every command?

A: Yes, the CS line must go low for at least 250 ns between each command. If you are doing a Write command and you bring CS low to activate the Data Polling mode, you must toggle CS low again after the Ready signal has been given by the device before the next Start bit can be sent.

Q: If V_{CC} drops during a write cycle will other data in the array be corrupted, or just the data being written?

A: Only the data being written will be corrupted if V_{CC} goes away during a write cycle. Other data bytes will be unaffected.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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02/16/06