AN1023

Using the C18 Compiler and the MSSP to Interface Microwire EEPROMs with PIC18 Devices

Author: *Martin Kvasnicka*
Microchip Technology Inc.

INTRODUCTION

There are many different microcontrollers on the market today that are being used in embedded control applications. Many of these embedded control systems need nonvolatile memory. Because of their small footprint, byte level flexibility, low I/O pin requirement, low power consumption, and low cost, serial EEPROMs are a popular choice for nonvolatile storage.

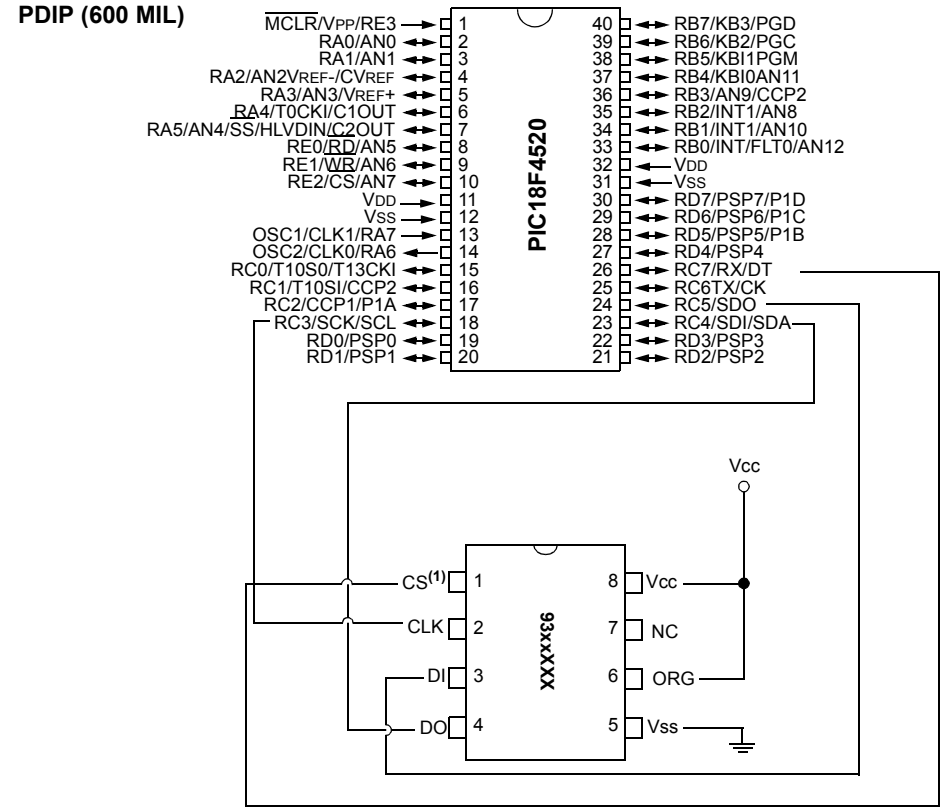
Microchip Technology has addressed these needs by offering a full line of serial EEPROMs covering industry standard serial communication protocol for two-wire (I^2C™), three-wire (Microwire), and SPI communication.

Serial EEPROM devices are available in a variety of densities, operational voltage ranges and packaging options.

This application note provides assistance and source code to ease the design process of interfacing a Microchip mid-range PIC18F4520 microcontroller to a Microchip Microwire serial EEPROM. The Master Synchronous Serial Port (MSSP) provides a simple three-wire connection to the EEPROM and no external "glue" logic is required.

Figure 1 depicts the hardware schematic for the interface between Microchip's Microwire devices and the Microchip PIC18F4520 Microcontroller. The schematic shows the necessary connections to interface the microcontroller and the serial EEPROM (software was written assuming these connections).

FIGURE 1: CIRCUIT FOR PIC18F4520 AND 93XXXXX (MICROWIRE) DEVICE



Note 1: CS should always have a pull-down resistor to protect against data corruption during power-up or power-down of the Microcontroller.

FIRMWARE DESCRIPTION

The purpose of the program is to show individual features of the Microwire protocol and give code samples of the Start bit, opcodes and addressing schemes so that the basic building blocks of a program can be shown. The waveforms provided will be shown from CS active to CS disable so an entire instruction can be seen. To ease the interpretation of the serial data, the data sheet waveform will be provided below the oscilloscope screen shot. A graphic similar to that of Figure 2 will be shown with the values being programmed by the firmware to also assist in ease of reading.

THEORY OF OPERATION

To use an SPI port (MSSP) to communicate with Microchip's Microwire Serial EEPROMs, the bytes to be output to the 93XXXX must be aligned such that the LSB of the address is the 8th bit (LSB) of a byte to be output. From there the bits should fill the byte from right to left consecutively. If more that 8 bits are required, then two bytes will be required to be output. This same method will work for any 93XXXX series device but the data sheet must be referenced for these because density and organization will change the number of bits sent for each command. Since more than 8 bits are required to control a 93LC66C, two consecutive bytes are required.

FIGURE 2: COMMAND ALIGNMENT

High Byte								Low Byte							
0	0	0	0	0	SB	OP1	OP2	A7	A6	A5	A4	A3	A2	A1	A0
Leading 0's here must be 0's, otherwise the device will see a Start bit with an invalid command following.															

High Byte (Where the Start bit, opcode bits, and address MSb reside)

The High Byte is configured in the following format: SB is the Start bit. OP1 is the MSb of the opcode and OP0 is the opcode LSb. The CS line can be set before the byte is output because the leading 0's output to the 93XXXX prevent a Start bit from being recognized by the 93XXXX until the first high bit is sent.

Low Byte (8 Address bits)

The Low Byte contains A7-A0, which are the address bits required to access 256 bytes in x16 mode.

INITIALIZATION

In order to configure the MSSP module to work for the Microwire protocol, several key registers on the PICmicro® Microcontroller need to be properly initialized. Code examples are shown for each. Since the Microwire protocol is not native to the MSSP module, a version of SPI mode 0,0 has been implemented and works within the data sheet specifications for Microwire.

MSSP STATUS Register (SSPSTAT)

SSPSTAT holds all of the Status bits associated with the MSSP module. For Microwire, the SMO bit of the register needs to be set for data to be sampled at the end of the data output time. The CKE bit also needs to be set so that data is transmitted on the rising edge of SCK when CKP (SSPCON1) is cleared.

EXAMPLE 1: SSPSTAT CONFIGURATION

```
SSPSTAT = 0xC0;   //SPI Bus mode 0,0
```

SSP Control Register 1 (SSPCON1)

SSPCON1 is another register for the MSSP module. For Microwire communication, the upper two bits of the SSPCON1 are indicator bits and should be cleared initially. The SSP Enable bit (SSPEN) needs to be set in order to enable the SSP module and the Clock Polarity Select bit needs to be cleared to set the IDLE state of the clock to be a low level. The lower four bits of the SSPCON1 set the mode and speed of communications, in this case we are setting this to Master mode and FOSC/16.

EXAMPLE 2: SSPCON1 CONFIGURATION

```
SSPCON1 = 0x21;  //Enable SSP,Fosc/16
```

TRISC Register

In order to be properly controlled by the MSSP module, the CLK, DI and DO pins must be configured properly. We have also chosen RC7 for Chip Select (CS) control so it must be configured as an output. This is done by setting their respective bits in TRISC to ‘1’ for inputs and ‘0’ for outputs, as shown in Example 3.

EXAMPLE 3: TRISC CONFIGURATION

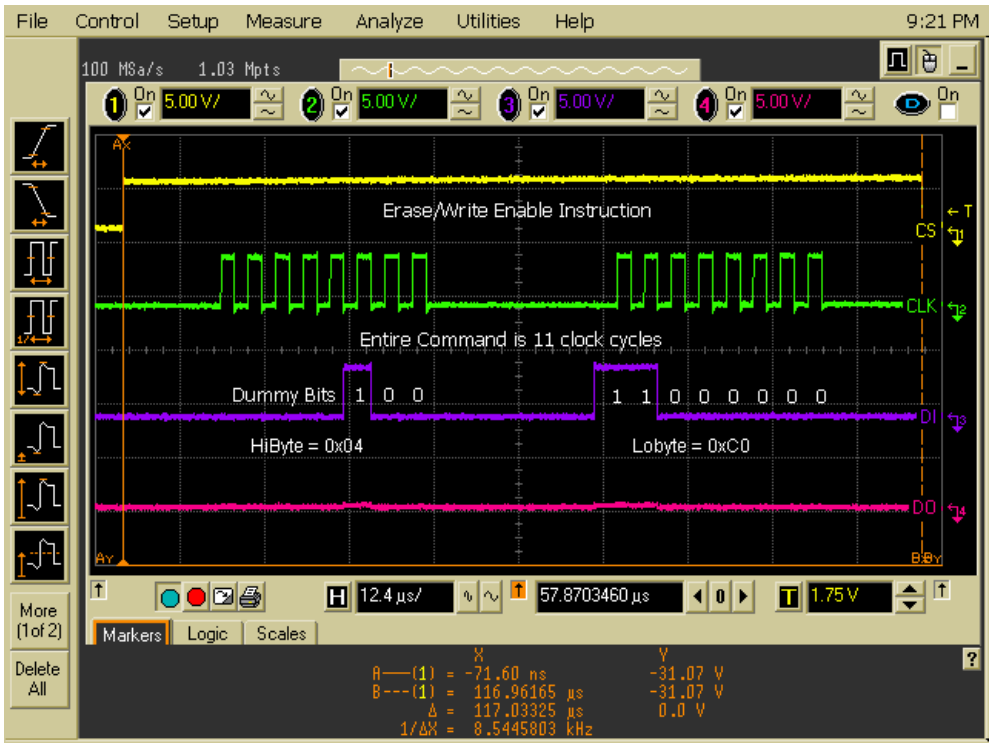
```
DDRCbits.RC7 = 0;  //CS as Output
DDRCbits.RC3 = 0;  //CLK as Output
DDRCbits.RC4 = 1;  //DI as Input
DDRCbits.RC5 = 0;  //DO as Output
```

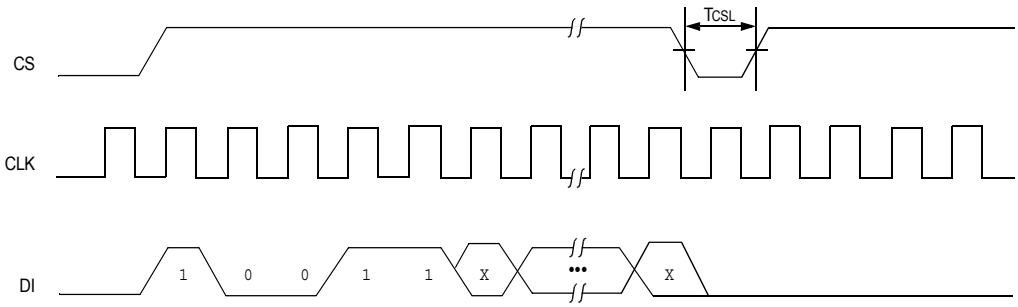
WRITE ENABLE

Figure 3 shows an example of the Erase/Write Enable (EWEN) command. This command consists of a Start bit and the four bit opcode (0000). Because this command doesn't require addressing, the two high order address bits (A7 and A6) are used for opcode. The remaining address bits (set to zeros in this example) are "don't cares".

Chip Select is brought high (active), the Start bit and opcode are sent out through the MSSP port. The EWEN command must be given before a write is attempted. The device will be enabled for writes until a Erase/Write Disable command is given or the device is powered down.

FIGURE 3: ERASE/WRITE ENABLE (EWEN)





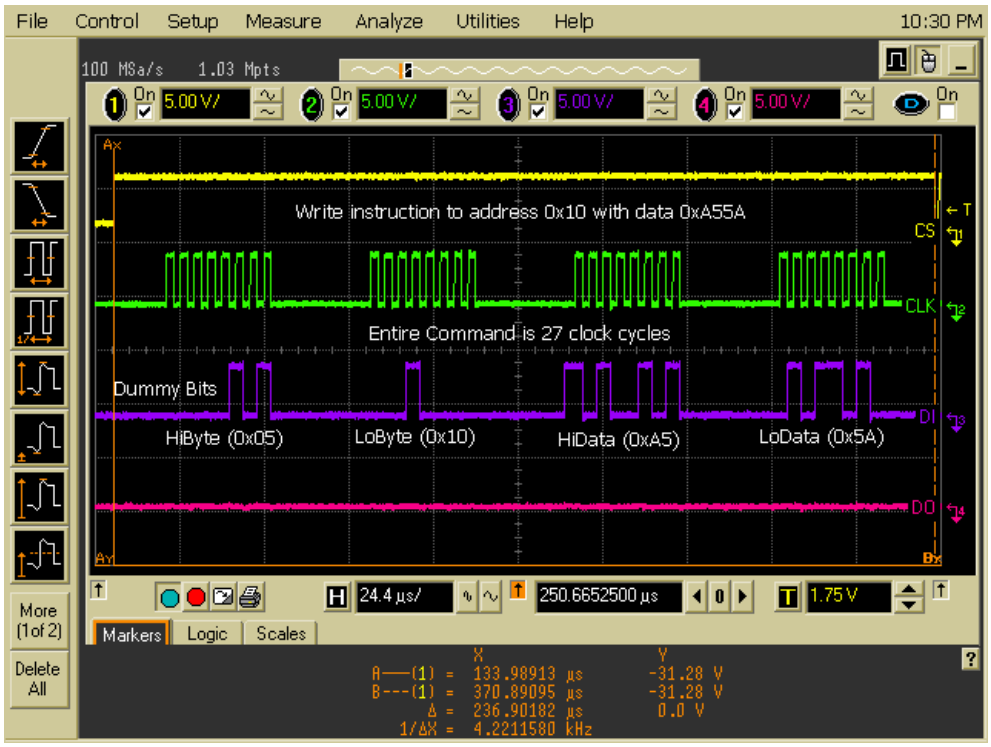
High Byte								Low Byte							
0	0	0	0	0	SB	OP1	OP2	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0
hibyte = 0x04h								lobyte = 0xC0h							

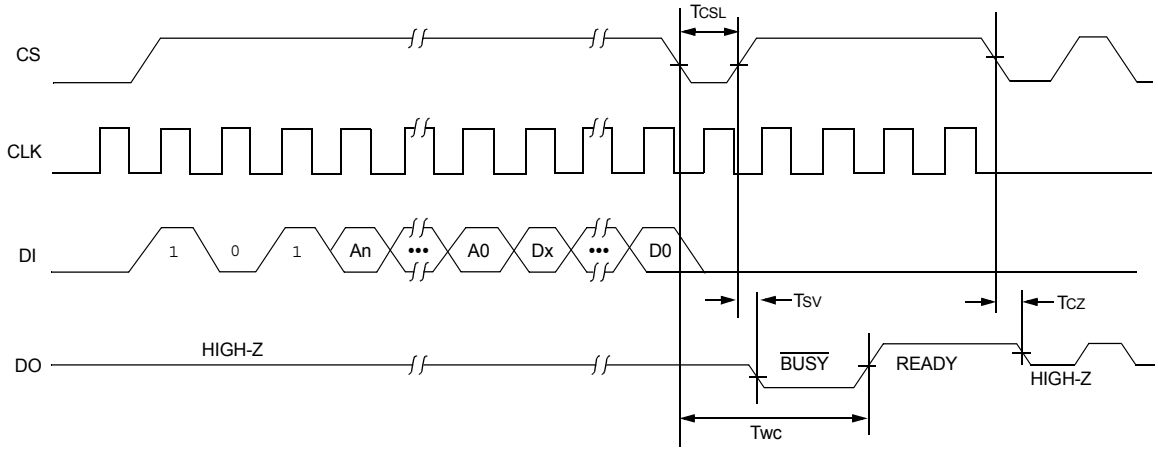
WRITE COMMAND (START BIT, OPCODE, ADDRESS AND DATA)

Figure 4 shows an example of the Write command. The device is selected and the high byte is sent out which contains the Start bit, and opcode. The second low byte is sent which contains the address bits A7-A0.

Finally, the data is clocked in, in this case, 0xA55A. When the Chip Select is toggled at the end of this, the internal write cycle is initiated. Once the internal write cycle has begun the READY/Busy signal can be polled on the DO pin to check when the write finishes. A 6 ms delay needs to be added if the READY/Busy status is not being polled. This code uses READY/Busy polling.

FIGURE 4: WRITE COMMAND, ADDRESS AND DATA





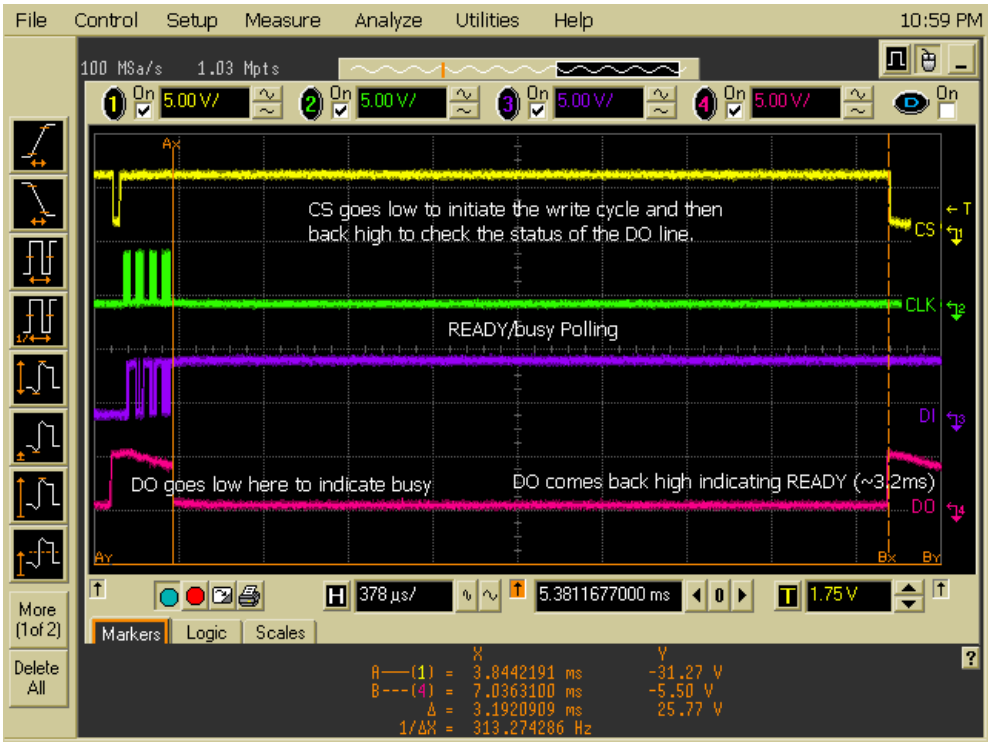
High Byte								Low Byte							
0	0	0	0	0	SB	OP1	OP0	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0
hibyte = 0x05h								lobyte = 0x10h							

READY/$\overline{\text{BUSY}}$ POLLING

After a valid Write command is given, the DO line of the 93XXXX can be monitored to check if the internal write cycle has been initiated and it can continuously be monitored to look for the end of the write cycle.

The oscilloscope plot below shows that the device is selected and the DO line is low for approximately 3.2 ms before the device brings the DO line high indicating that the write cycle is complete.

FIGURE 5: READY/$\overline{\text{BUSY}}$ POLLING

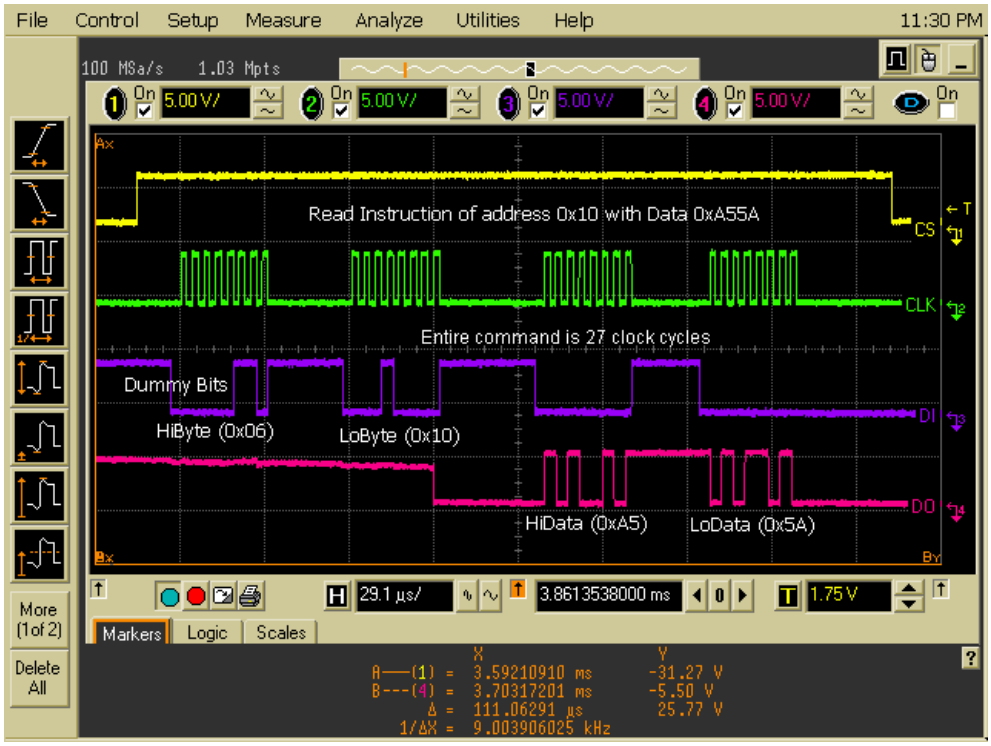


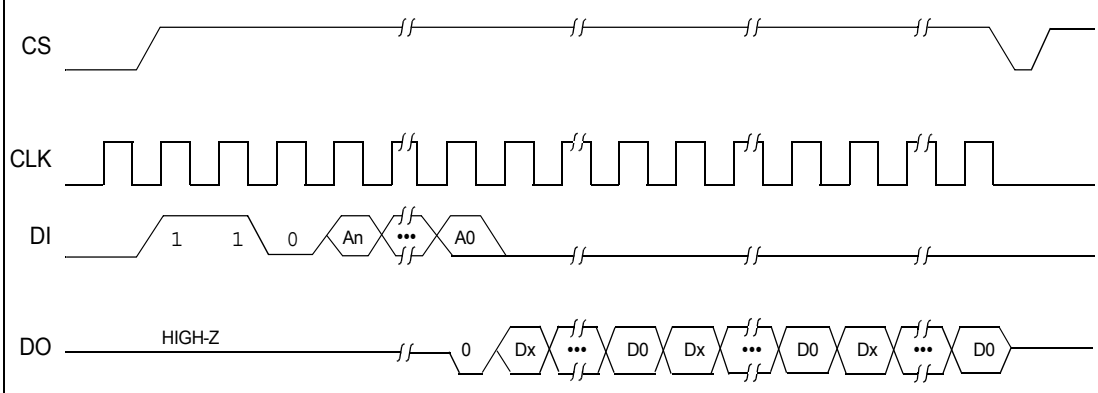
READ COMMAND (START BIT, OPCODE, ADDRESS AND DATA)

Figure 6 shows an example of the Read command. The device is selected and the high byte is sent out which contains the Start bit and opcode.

The second low byte is sent which contains the address bits A7-A0 (0x10). At this point the device gets ready to send data out, the controller needs to send a dummy byte in order for the clock signals to be sent so the data can be read out of the device and into the microcontroller. In this case, data being read is 0xA55A.

FIGURE 6: READ COMMAND





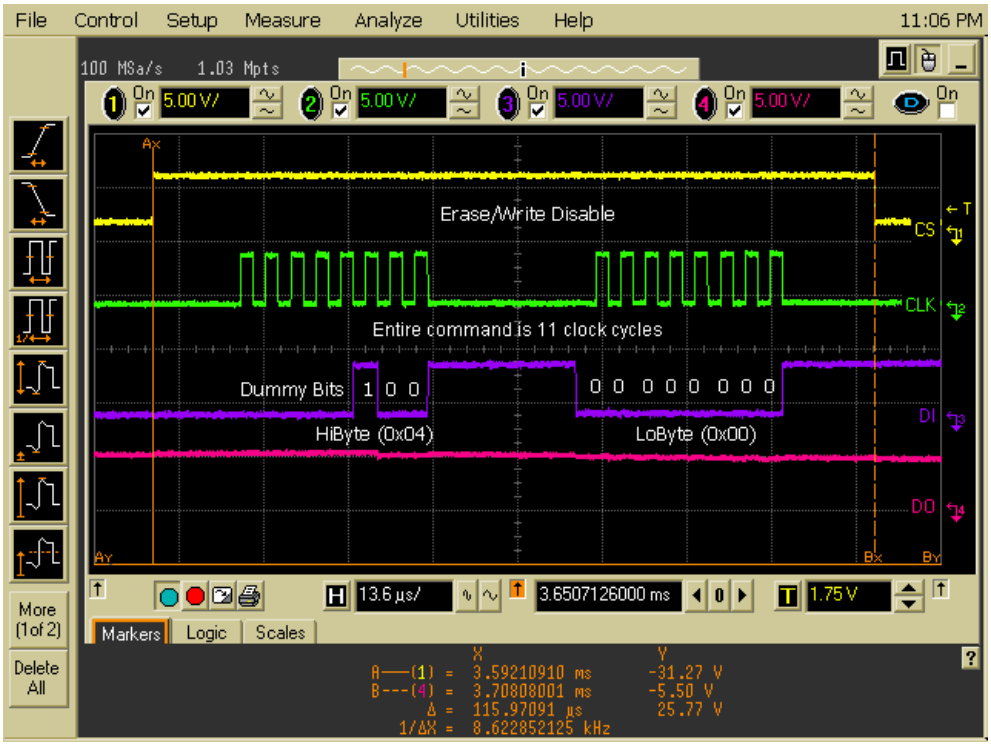
High Byte								Low Byte							
0	0	0	0	0	SB	OP1	OP0	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0
hibyte = 0x06h								lobyte = 0x10h							

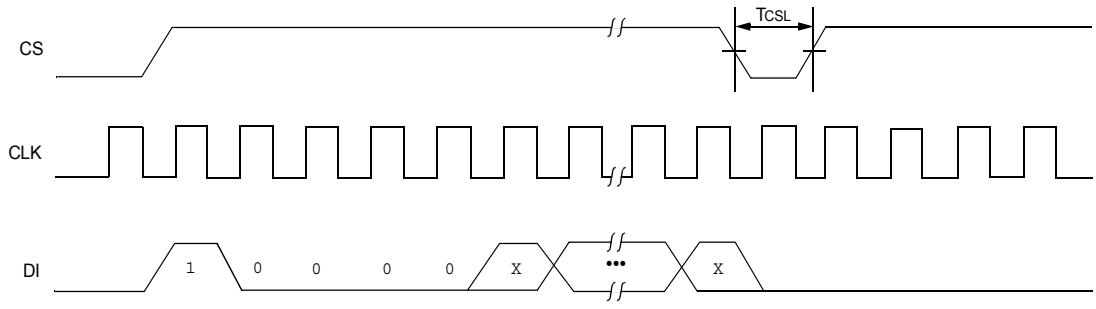
ERASE/WRITE DISABLE COMMAND

Once the device write is finished, the Write Disable (EWDS) command should be given (see Figure 7). This command consists of a Start bit and the four bit opcode (0000). Because this command doesn't require addressing, the two high order address bits (A7 and A6) are used for opcode. The remaining address bits (set to zeros in this example) are "don't cares".

The EWDS command should always be sent to the device after completing a write or prior to powering down the device/system.

FIGURE 7: ERASE/WRITE DISABLE COMMAND





High Byte								Low Byte							
0	0	0	0	0	SB	OP1	OP0	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
hibyte = 0x04h								lobyte = 0x00h							

CONCLUSION

These are some of the basic features of Microwire communications using the MSSP module on the PIC18F4520. The code is highly portable and can be used on many devices that have the MSSP module with very minor modifications. Using the code provided, designers can begin to build their own Microwire libraries to be as simple or as complex as needed.

The code was tested on Microchip's PICDEM™ 2 Plus Demonstration Board with a 4 MHz crystal and the connections shown in Figure 1.

NOTES:

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