EEPROM Endurance Tutorial

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BASIC TERMS

The definition of “endurance” (as applied to EEPROMs) contains various words and phrases that require clear definition and understanding. As shown in the following paragraphs, different manufacturers use different standards. “Endurance cycling” is a test performed by all manufacturers (and some customers) to determine how many “write cycles” the product will achieve before failing.

Microchip defines “endurance” as the minimum number of write cycles the product can be subjected to before it fails.

“Failure” is a somewhat arbitrary definition since a device only truly fails when it no longer meets the customer expectation and does not operate in his system. A failure can be defined in this, the loosest of definitions, or the most stringent of definitions (whereby a device would fail if it did not meet any of the data sheet parameters), as well as a wide range in between. For example, if the device does not correctly store data into a particular address that is not used, then the device would work correctly for the customer but would fail a functional test by the manufacturer. Likewise, if the device draws more current than the data sheet specifies after some time, but the customer application could supply the current needed, the device would work in the customer application but would fail a parametric test set by the manufacturer.

Microchip uses the most stringent definition:

A failure occurs when the device fails to meet any data sheet condition under any *specified* operating condition of a temperature and voltage.

The number of devices that can fail before a particular endurance criteria is not met is also somewhat flexible. Even the most quality-conscious manufacturer will occasionally have a failure, so a failure level is defined. There are several industry standard conditions for many types of reliability tests. For example, IEEE-Std-1005-1998 defines a maximum cumulative failure rate of 1%. JEDEC (The Joint Electronic Device Engineering Council), JESD47, defines that if three lots of 77 units each have no fails (equivalent to an LTPD of 1%) at a given endurance goal, then that goal has been met.

Microchip uses a more stringent criteria for endurance:

No fails out of a sample of 256 units per product, and no fails out of 3 lots of 256 units each per technology for the given endurance goal to have been met. That is equivalent to 0/768 or less than 0.3% LTPD.

A “write cycle” is also a somewhat flexible definition since almost every customer will write the device in a different way. For example, if the customer application uses only the first three bytes of the array to store variable data, and the remainder of the array is used as a look-up table, then a write cycle will be complete when the three data bytes have been re-written to their new data state.

A write cycle is often described as an erase/write cycle since almost all EEPROM technologies employ an “auto-erase” before the data is actually written to the array. This is also used by Microchip but we will use the term “write cycle” since the auto-erase is invisible to, and cannot be suppressed by, the customer.

The term “data changes” is occasionally used in place of “write cycle” or “erase/write cycle.” A data change will occur when an auto-erase cycle is initiated, and a second data change will occur upon the write cycle, therefore, an “erase/write cycle” is equivalent to two “data changes.” The term “data change” may also imply that a different type of cycling is being used than “erase/write cycle”. This will be described later.

The term “write cycle” does not define under what conditions the cycling was done (unless explicitly stated), nor does it define the type of cycling that was done. The endurance cycling can be done at any number of conditions of voltage and temperature (e.g., 85°C and 5.5V, or 25°C and 5.0V) that may or may not meet with a customer’s application. The cycling mode used in endurance cycling can affect the endurance of the product. All these effects will be described later. Microchip uses the most stringent conditions that are reasonable for endurance cycling: Byte or Page mode cycling at a temperature or 85°C at 5.5V. All data not explicitly defined at other conditions is taken at these conditions.

SYSTEM DESIGN CONSIDERATIONS

There are a number of design considerations that the system designer can use to maximize the endurance of an EEPROM-based device, if endurance is the application’s limiting factor.

As will be described in more detail later, if the designer has any control over certain environmental or operating conditions, he should observe the following basic guidelines:

- Keep the application temperature as low as possible.
- Keep the application voltage (or the VCC voltage on the EEPROM) as low as possible.
- Write as few bytes as possible.
- Use page write feature whenever possible
- Write data as infrequently as possible.

With these basic guidelines applied to the fullest extent, the endurance of EEPROM-based devices can be extended well beyond the specified minimum endurance. Under certain very specific conditions, Microchip Serial EEPROMs have been shown to last for over 100 million cycles, and 10-million cycle applications are common.

WRITE MODES IN EEPROMS

There are three ways that EEPROM-based devices can have the entire array data contents changed. These are: Byte mode, Page mode and Block (or Bulk) mode. Some types of devices support all three modes, others may only support one or two modes. The mode that is used to write an EEPROM-based device may affect the long term endurance of the product. Byte mode writing is used when the contents of the array are changed one byte at a time. For some devices this is the only user-accessible write mode available. To change the entire contents of a Serial EEPROM in this way would take up to 6 minutes (using 5 ms per byte on a 512K Serial EEPROM). Page mode writing is a popular feature on many designs of EEPROM memory products. Again using 512K serial EEPROM as an example, this feature allows up to 128 bytes of data to be written to the memory in the same time that one byte would normally take. In this mode, the write time for a 512K Serial EEPROM can be cut from 6 minutes to 3 seconds. Block cycle is generally a test mode used by EEPROM manufacturers to make it easier to test the products. Some types of EEPROM-based products have these modes as user options (such as the ERAL and WRAL mode in 93LXXX products), but generally this mode is not user accessible. A block write can be done in as little as 1 ms, allowing millions of write cycles to be completed in a few hours.

A general rule to follow in choosing write modes is that the larger the number of bytes being written in a single instruction, the longer the device will last. For example, in Byte mode, a device might start to fail after 300,000 cycles under a particular set of conditions. But the device may last 600,000 cycles in Page mode under the same conditions. In Block mode, the device might last 1 million cycles under the same conditions.

The reason for this is related to the internal design of any EEPROM-based product. In these devices, an internal "charge-pump" takes the applied VCC voltage (typically 1.8V to 5.5V) and increases it to 15V to 20V. This voltage is required to induce "Fowler-Nordhiem Tunneling" that is used to program and erase EEPROM-based devices.

The charge pump voltage is used to program however many EEPROM-cells are being programmed. For example, in Byte mode, all the cells in a byte (8 or 16) are biased with the charge pump voltage. In Block mode, all the cells in the array (up to 1M depending on the device) are biased with the charge pump voltage. The charge pump is like a current source during conditions of high load, so the voltage put out by the charge pump will be reduced slightly if more bytes are being written. If the whole array is being programmed then the charge pump voltage will be significantly reduced.

Generally, the lower the charge pump voltage the better the endurance (there is a limit since the charge pump voltage needs to be high enough to program the cell) and so the best endurance is generally achieved by using Block mode cycling. Page mode is worse than Block mode, but better than Byte mode. Block mode is generally not a very useful cycling mode to the end user, since the data contents in the whole array will be changed to the same value (generally 00 or FF). When Microchip tests EEPROM-based products, we use Byte mode cycling on devices which do not have a Page mode, and Page mode cycling for those that do. We encourage our customers to use Page mode writing on all products that have Page mode in order to get the highest endurance.

ENDURANCE TESTING METHODOLOGIES

Different manufacturers use different ways to both cycle and test EEPROM-based products. There is no standard for endurance cycling or for testing devices after cycling.

There are two groups of testing that Microchip performs on all products: qualification and production. Qualification testing is done for all new products and major changes to a product or manufacturing process. Production testing is done on all devices shipped to our customers.

Qualification testing at Microchip is used to ensure that the device is reliable. A great deal of testing is done, including endurance testing on all EEPROM-based products. Endurance cycling is *generally* done at 85°C. After the rated number of cycles, the sample is tested to a full production test program. After endurance, the units are subject to "data retention" to ensure that the required 200 years of data retention will be achieved after the maximum number of cycles has been completed.

Endurance cycling is done under the conditions previously described and the data retention test is performed after this. After the data retention stress is completed (which takes up to six weeks), the devices are tested again to confirm the functionality of the device to all data sheet parameters. No failures are allowed after the endurance or data retention stress (equivalent to more than 200 years at 55°C).

Production testing is done on all devices shipped to a customer. Production testing begins immediately after a wafer lot is finished being processed, continuing in various stages until the devices are shipped to a customer.

The first tests conducted on EEPROM-based products at Microchip are called wafer sort. They are completed before the wafer is cut up into dice for assembly. There is a series of tests which include Block cycle (up to 5000) to ensure reliability by weeding out weak devices so they never get shipped. After assembly, full testing is again done to ensure device functionality at the temperature extremes.

The testing that Microchip does is unique. Microchip firmly believes that our testing ensures the highest quality and reliability.

THE EFFECT OF TEMPERATURE ON EEPROM ENDURANCE

The temperature at which cycling is done will affect the number of write cycles that can be executed before the device fails. The higher the temperature, the worse the endurance will be. Generally, and approximately, a device which fails at 10 million cycles at 25°C will fail at 2 million cycles at 85°C and 1 million cycles at 125°C. The reasons for this are not conclusive (although there is much technical literature supporting one theory or another), but it is apparent that the failure mode of EEPROM cells (electron trapping in the tunnel dielectric causing shielding and dielectric breakdown) is strongly dependent on temperature.

Data taken by Microchip suggests that if the typical failure of an EEPROM-based device is 10 million cycles at 25°C, the mean failure will occur at other temperatures according to the following table:

TABLE 1: TEMPERATURE MEAN FAILURE

Write Cycle Temperature	Mean Failure (Cycles)
-40°C	37.1 Million
0°C	16.7 Million
25°C	10.0 Million
40°C	7.4 Million
55°C	5.4 Million
70°C	4.0 Million
85°C	2.9 Million
100°C	2.2 Million
125°C	1.3 Million

This data was taken on Microchip FLOTOX Fowler-Nordhiem Tunneling EEPROMs and formed a part of the data set used to create the Total Endurance™ model. Other technologies may have different characteristics. As is clearly seen, any cycling done at 25°C can be misleading in the extreme if the application requires a device that can be cycled 10 million times at, say, 55°C.

THE EFFECT OF VOLTAGE ON EEPROM ENDURANCE

The voltage at which a device is written can also affect the endurance. This is simply because the charge pump (used to program and erase EEPROM cells) is more powerful at higher voltages. As has already been described, a higher programming voltage will reduce the endurance of an EEPROM cell and a stronger charge pump will produce a higher voltage.

More recently designed Serial EEPROM products at Microchip have minimized this effect in order to provide a more consistent endurance across V_{DD} voltage.

Data taken by Microchip suggests that if the typical failure of an EEPROM-based device is 1 million cycles when endurance cycling is done at 5.5V, mean failure occurs at other temperatures according to the following table:

TABLE 2: VOLTAGE MEAN FAILURE

Endurance Cycling Voltage	Mean Failure
5.5V	1.0 Million
5.0V	1.2 Million
4.5V	1.4 Million
4.0V	1.7 Million
3.5V	2.0 Million
3.0V	2.4 Million
2.5V	2.8 Million
2.0V	3.3 Million

This data was taken on Microchip FLOTOX Fowler-Nordhiem Tunneling EEPROMs and formed a part of the data set used to create the Total Endurance model. Other technologies may have different characteristics.

THE EFFECT OF WRITE MODE ON EEPROM ENDURANCE

As has been discussed, there are three basic ways of writing data to an EEPROM-based device:

- Byte mode
- Page mode
- Block mode

This is related to the strength of the charge pump in applying the required programming voltages to the EEPROM cells.

Data taken by Microchip suggests that if the typical failure of an EEPROM-based device is 1 million cycles when the endurance cycling is done in Byte mode, the mean failure will occur in other modes according to the following table:

TABLE 3: ENDURANCE MEAN FAILURE

Endurance Cycling Mode	Mean Failure (Cycles)
Byte	2.3 Million
Page	2.8 Million

This data was taken on Microchip FLOTOX Fowler-Nordhiem Tunneling EEPROMs and formed a part of the data set used to create the Total Endurance model. Other technologies may have different characteristics. This data was taken from a Microchip 24LC256. Block cycle data is no longer provided.

THE TOTAL ENDURANCE PREDICTIVE SOFTWARE

Microchip has a Windows®-based model called Total Endurance™ software. This program, based on all the customer endurance parameters, will predict the failure level at the expected end of application life. This tool is invaluable for system designers who would like to fine-tune their application in favor of endurance. It is available to download from Microchip’s web site at www.microchip.com.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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