

Using the MSSP Module to Interface SPI™ Serial EEPROMs with PIC18 Devices

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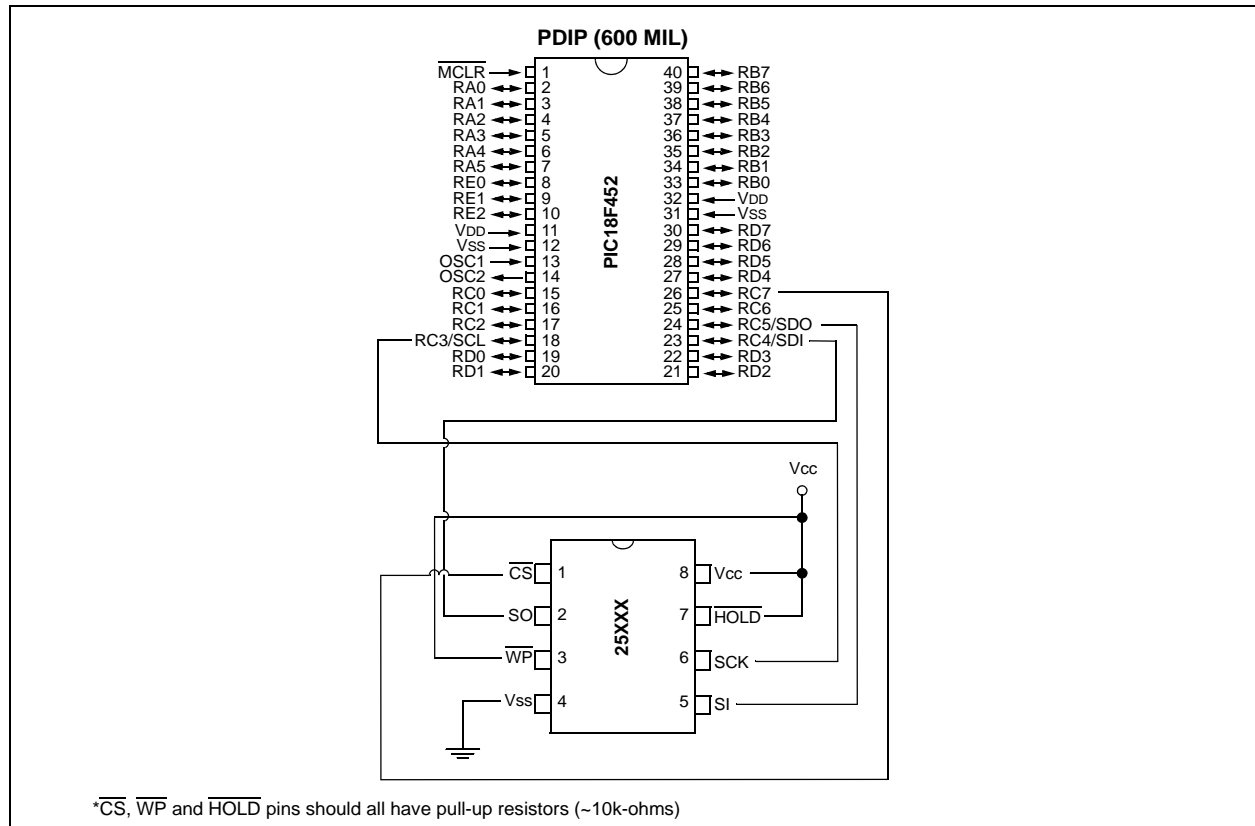
INTRODUCTION

The 25XXX series serial EEPROMs from Microchip Technology are SPI™ compatible and have maximum clock frequencies ranging from 3 MHz to 20 MHz. The MSSP module available on many PICmicro® microcontrollers provides a very easy-to-use interface for communicating with the 25XXX series devices. The largest benefit of using the MSSP module is that the signal timings are handled through hardware rather than software. This allows the firmware to continue executing while communication is handled in the background. This also means that an understanding of the timing specifications associated with the SPI protocol is not required in order to use the 25XXX series devices in designs.

This application note is intended to serve as a reference for communicating with Microchip's 25XXX series serial EEPROM devices with the use of the MSSP module featured on many PIC18 family devices. Source code for common data transfer modes is also provided.

Figure 1 describes the hardware schematic for the interface between Microchip's 25XXX series devices and the PIC18F452 PICmicro microcontroller. The schematic shows the connections necessary between the microcontroller and the serial EEPROM as tested, and the software was written assuming these connections. The \overline{WP} pin is tied to Vcc because the STATUS register write-protect feature is not used in the examples provided.

FIGURE 1: CIRCUIT FOR PIC18F452 AND 25XXX SERIES DEVICE



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FIRMWARE DESCRIPTION

The purpose of the program is to show individual features of the SPI protocol and give code samples of the opcodes so that the basic building blocks of a program can be shown. The opcodes used in the program are Write Enable (WREN), Write, Read, and Read Status Register (RDSR) (used in the program for WIP polling). The oscilloscope pictures have markers that are shown from CS enable to CS disable for ease in reading. The data sheet version of the waveform is below the actual oscilloscope picture. The MSSP module is set up for Mode 1,1 operation at approximately 625 kHz. The code is written in modules and commented so changing modes, speeds, and modifying commands such as sequential reads and page writes is simple. The values represented in this application note are all hex values.

INITIALIZATION

In order to configure the MSSP module for SPI mode 1,1, several key registers on the PICmicro microcontroller need to be properly initialized. Code examples are shown for each.

SSP STATUS Register (SSPSTAT)

SSPSTAT holds all of the Status bits associated with the MSSP module. In SPI mode 1,1 the SMP bit of the register needs to be set for data to be sampled at the end of the output time. The CKE bit also needs to be cleared for mode 1,1 operation, this assures that data is transmitted on the rising edge of SCK when CKP bit (SSPCON1) is set. This is done as shown in Example 1.

EXAMPLE 1: SSPSTAT CONFIGURATION

```
CLRF    SSPSTAT ;clear SSP stat reg
MOVLW  0x80     ;set SPI master mode
MOVWF  SSPSTAT ;cke = 0 (mode 1,1)
```

SSP Control Register 1 (SSPCON1)

SSPCON1 is one of the Configuration registers for the MSSP module. In SPI mode 1,1, the upper two bits of SSPCON1 are indicator bits and should be cleared initially. Also, while in mode 1,1, the Clock Polarity Select bit (CKP) needs to be set for Idle state of the clock to be a high level. The SSP Enable bit (SSPEN) must be set in order to enable the serial port. The mode is set using the SSPM3:SSPM0 bits, '0001' for SPI Master with FOSC/16 for approximately 625 kHz operation. This register is configured using the code shown in Example 2.

EXAMPLE 2: SSPCON1 CONFIGURATION

```
CLRF    SSPCON1 ;clear SSP ctrl reg
MOVLW  0x31     ;set up SPI master
MOVWF  SSPCON1 ;clk/16,ckp=1(mode1,1)
```

TRISC Register

In order to be properly controlled by the MSSP module, the CS, SCK, SDI and SDO pins must be configured properly. This is done by setting their respective bits in TRISC to '1' for inputs and '0' for outputs, as shown in Example 3.

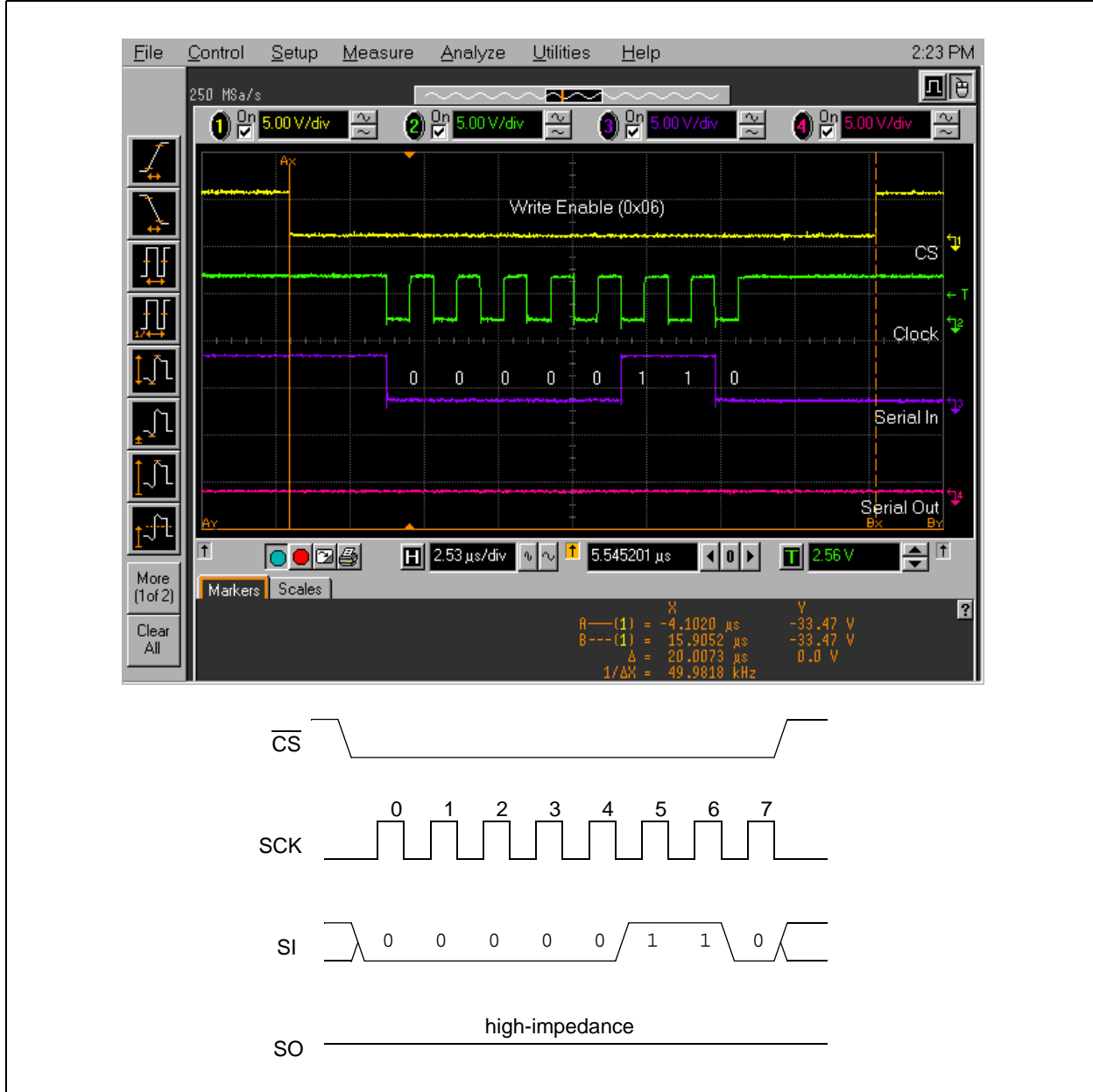
EXAMPLE 3: TRISC CONFIGURATION

```
CLRF    PORTC ;initialize portc to 0
MOVLW  0x10   ;all outputs except SDI
MOVWF  TRISC  ;move to TRIS portc
```

WRITE ENABLE

Figure 2 shows an example of the Write Enable command. Chip Select is brought low (active) and the opcode is sent out through the MSSP port. The Write Enable command must be given before a write is attempted to either the array or the STATUS register. The WEL bit can be cleared by issuing a Write Disable command (WRDI) or it is automatically reset if the device is powered down or a write cycle is completed.

FIGURE 2: WRITE ENABLE (WREN)

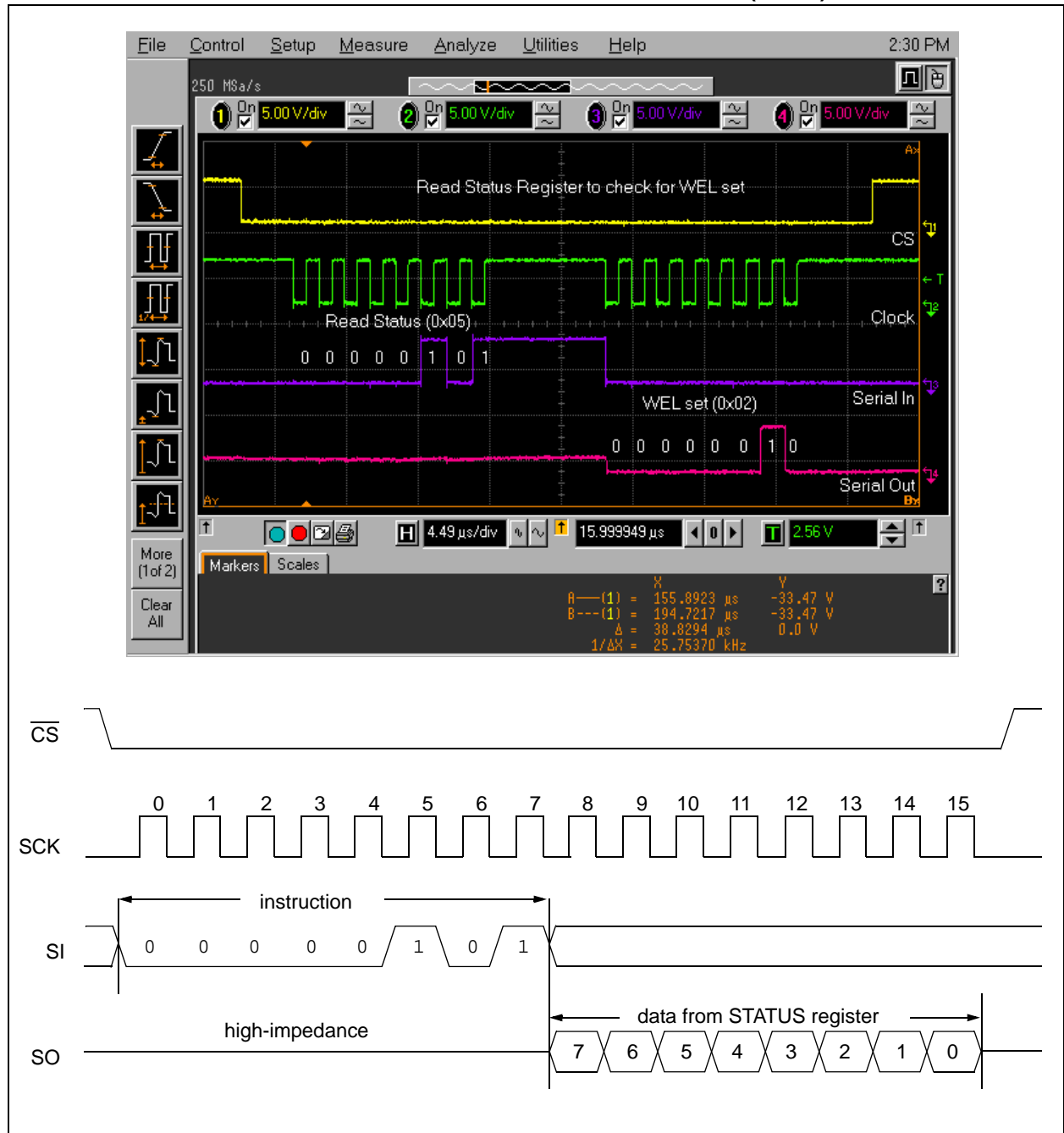


READ STATUS REGISTER TO CHECK FOR WEL BIT

Figure 3 shows an example of the Read Status Register command to check for the WEL bit. The WEL bit must be set before a write is attempted to either the STATUS register or the array. It is good programming practice to check whether this bit is set before attempting the write.

Once again the device is selected and the opcode, 0x05, is sent. The STATUS register is shifted out on the Serial Out pin. A value of 0x02 shows that the WEL bit in the STATUS register has been set. The device is now ready to do a write to either the STATUS register or the array.

FIGURE 3: READ STATUS REGISTER TO CHECK FOR WEL BIT (RDSR)



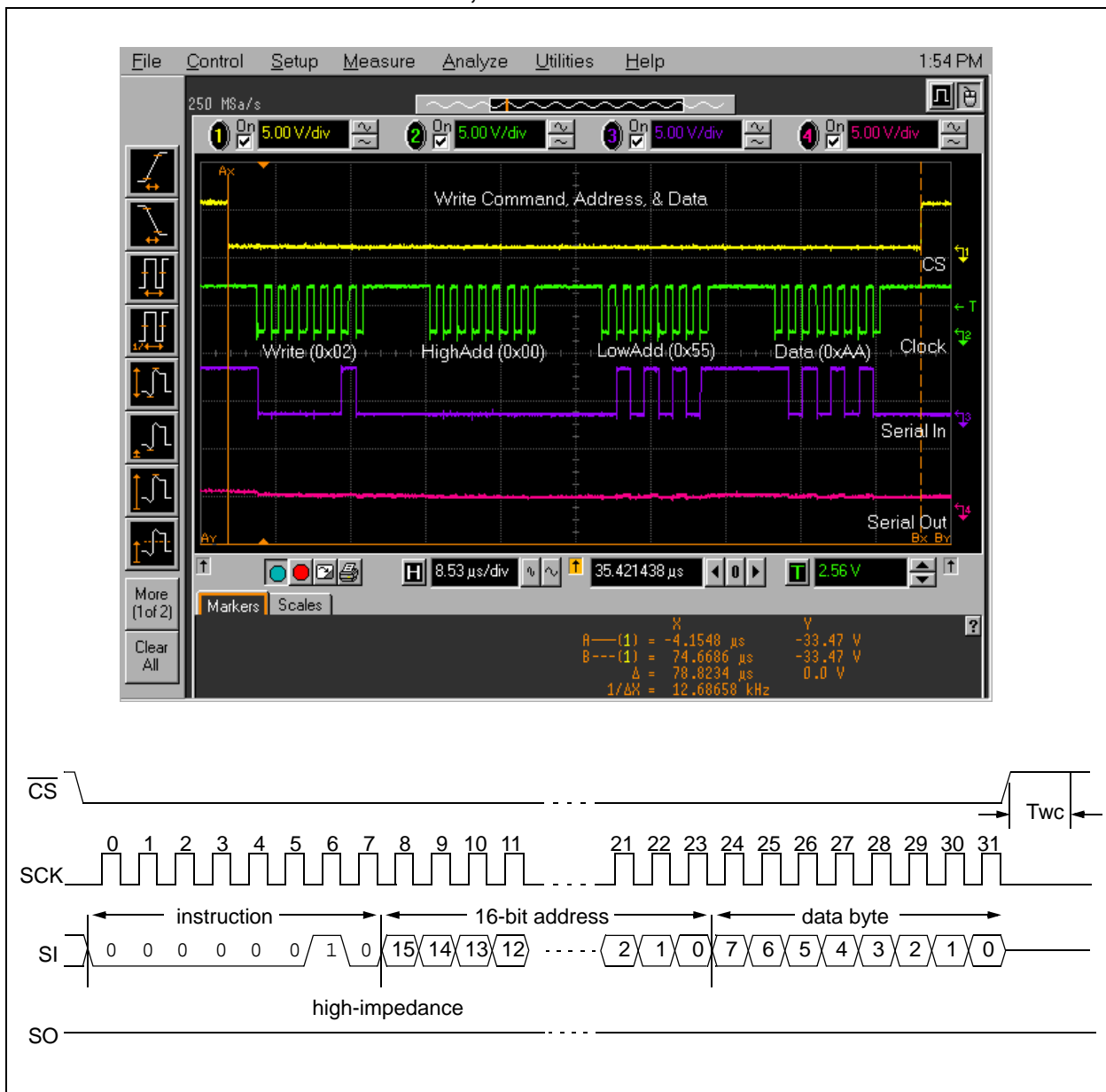
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BYTE WRITE COMMAND (OPCODE, ADDRESS AND DATA)

Figure 4 shows an example of the Write command. For this, the device is selected and the opcode, 0x02, is sent. The High Address byte is given 0x00, followed by the Low Address byte, 0x55. Finally, the data is clocked in last, in this case, 0xAA. Once the Chip Select is toggled at the end of this command, the internal write cycle is initiated. Once the internal write cycle has begun, the WIP bit in the STATUS register can now be polled to check when the write finishes or a delay needs to be added (~5ms), if the WIP bit is not being polled. This code uses WIP polling.

A page write can be accomplished by continuing to give data bytes to the device without toggling \overline{CS} . Up to one full page (64 bytes for the 25XX256) can be written before a write cycle is needed. Once \overline{CS} is brought high after the data bytes have been transmitted, then the write cycle timer will begin and normal polling can be initiated. The Page Write function programs all 64 bytes of data in the first page. Since the starting address is 0x0055, the last 21 bytes of data will wrap from address 0x007F to 0x0040 and complete the page. Caution should be taken when page writes are initiated in this manner so that previously stored data doesn't get overwritten.

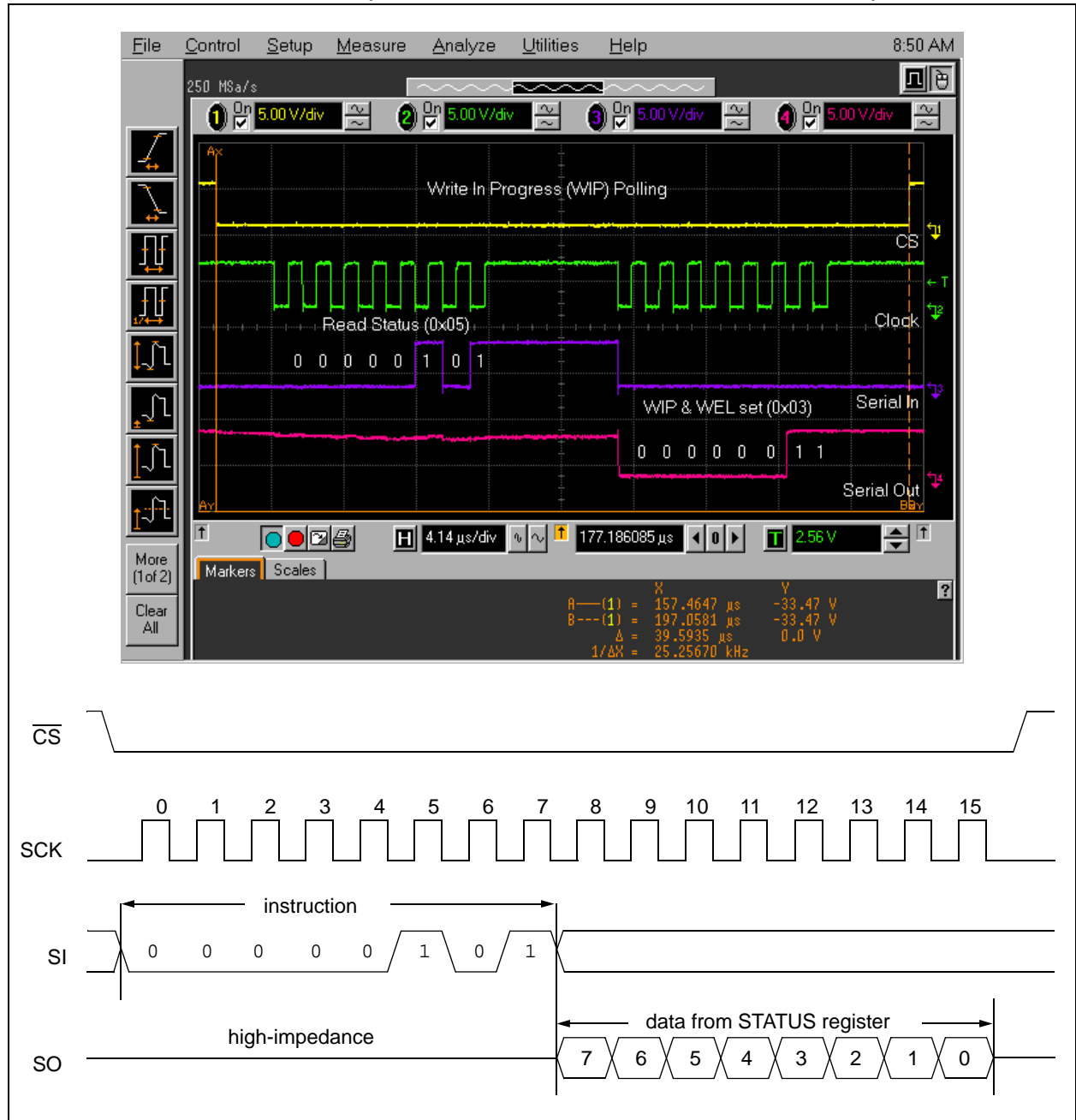
FIGURE 4: BYTE WRITE COMMAND, ADDRESS AND DATA



DATA POLLING (RDSR – CHECK FOR WIP SET)

After a valid Write command is given, the STATUS register can be read to check if the internal write cycle has been initiated, and it can continuously be monitored to look for the end of the write cycle. In this case, the device is selected and the opcode, 0x05, is sent. The STATUS register is then shifted out on the Data Out pin, resulting in a value of 0x03. Figure 5 shows that both the WEL bit (bit 1) and the WIP bit (bit 0) are set, meaning the write cycle is in progress.

FIGURE 5: DATA POLLING (READ STATUS REGISTER TO CHECK WIP BIT)

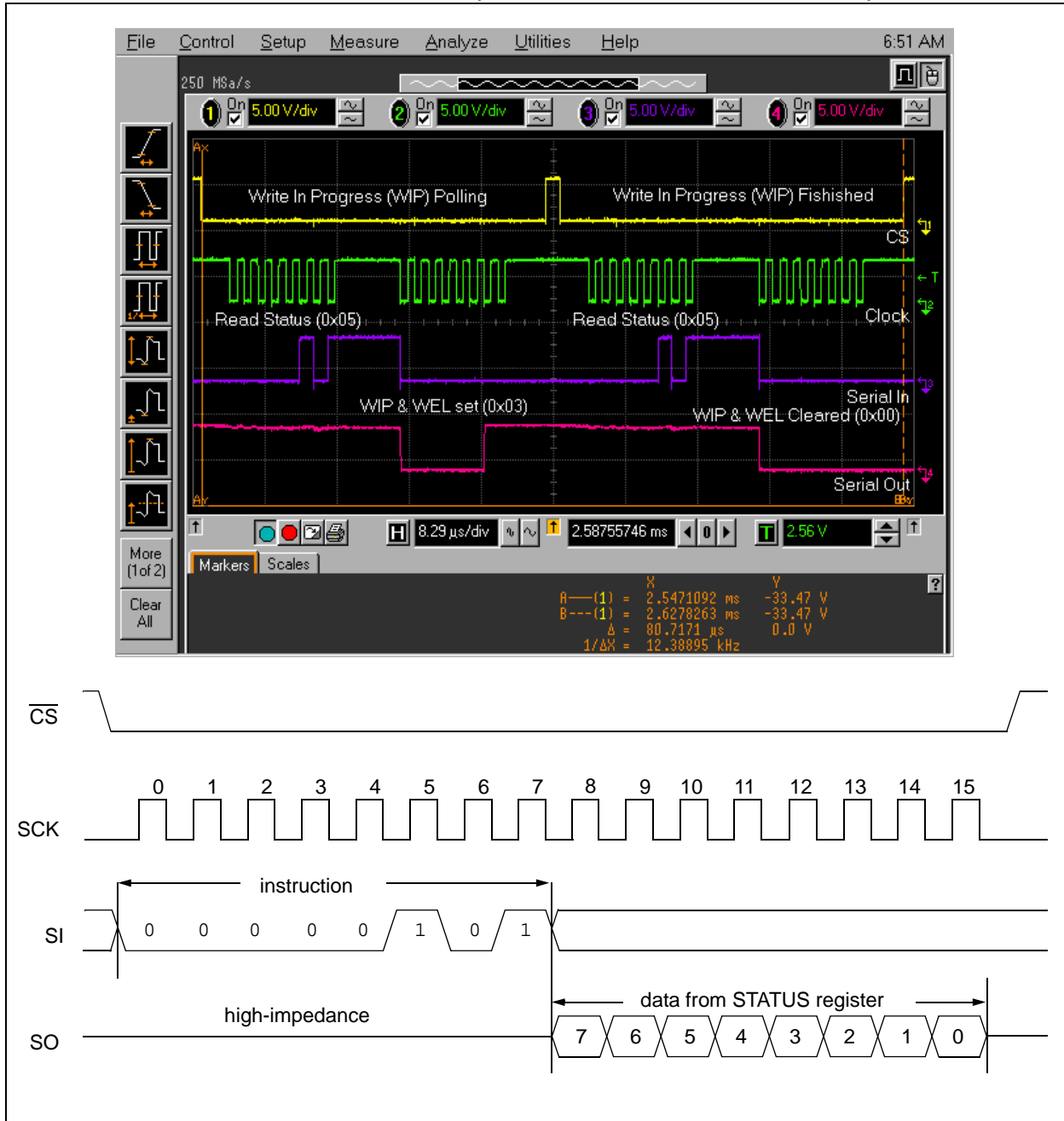


DATA POLLING FINISHED (RDSR – WIP BIT CLEARED)

The part remains in a continuous RDSR loop and the WIP status is evaluated until the bit is cleared. Figure 6 shows the Status Register Read command followed by a value of 0x00 being shifted out on the Data Out pin.

This indicates that the write cycle has finished and the device is now ready for additional commands. The WEL bit is also cleared at the end of a write cycle, which serves as additional protection against unwanted writes.

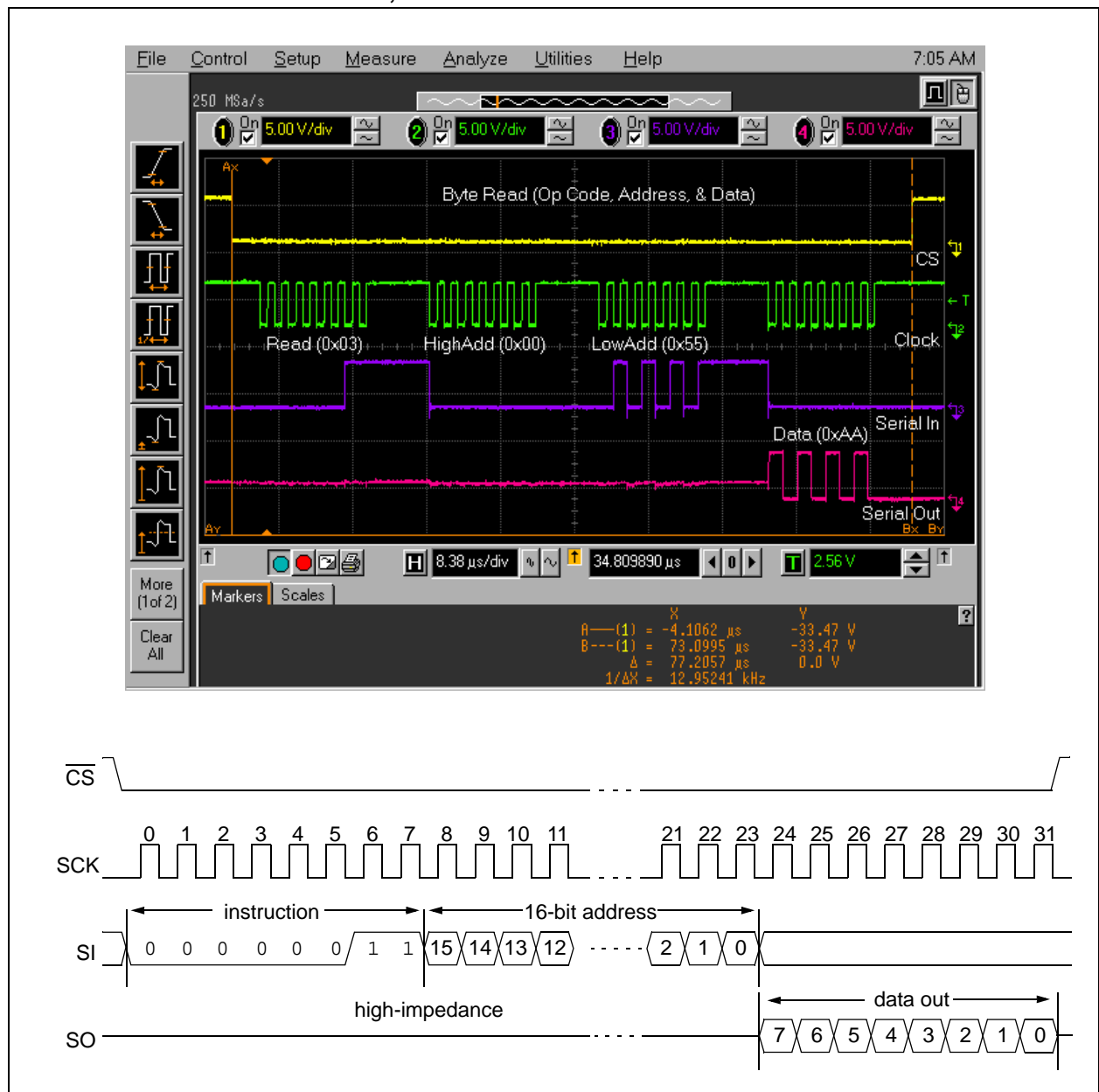
FIGURE 6: DATA POLLING FINISHED (RDSR – WIP & WEL BITS CLEARED)



READ COMMAND (OPCODE, ADDRESS AND DATA)

Figure 7 shows an example of the Read command. For this, the device is selected and the opcode, 0x03, is sent. The High Address byte is given 0x00, followed by the Low Address byte, 0x55. Finally, the data is clocked out on the Serial Out pin, in this case, 0xAA. In order to do a sequential read, more clocks need to be generated. It is possible to read the entire chip by continuing to provide clocks to the device. Once the end of the array is reached, the data will wrap to the beginning of the array (Address 0x0000) and keep reading out until \overline{CS} is deselected or clocks stop being provided.

FIGURE 7: READ COMMAND, ADDRESS AND DATA



CONCLUSION

These are some of the basic features of SPI communications using the MSSP module on one of Microchip's PIC18F devices. The code is highly portable and can be used on many devices that have the MSSP module with very minor modifications. Using the code provided, designers can begin to build their own SPI libraries to be as simple or complex as needed. The code was tested on Microchip's PICDEM™ 2 Plus Demonstration Board with the connections shown in Figure 1.

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