Smaller Packages = Bigger Thermal Challenges

By Bonnie C. Baker, Microchip Technology Inc.

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IC manufacturers are working furiously to reduce the package sizes for their customer base. This effort has been well received by the multitudes, particularly where portable applications are involved. But one of the primary specifications that changes, with smaller packages, is the package thermal resistance. If a smaller outline device is still required to deliver large currents and you want a reliable system, thermal evaluation becomes a requirement.

A first order look at the thermal behavior of your circuit can be done with some simple calculations. From there, lab testing might be necessary in order to prove your calculated conclusions. To illustrate the techniques that are used in a thermal evaluation, we need to choose an appropriate product. One product type that is used extensively in portable applications is a Low-Drop-Out Regulator (LDO). An LDO is used to convert a battery voltage to a lower, regulated output voltage. This regulated output voltage supplies power to the rest of the application circuit. But a closer look at this application family will show that it is not unusual to have more than one LDO in the circuit. This prompts designers to use a dual LDO instead of a single LDO per package. The dual LDO conserves board space and possibly improves the overall price, but dissipates the power of both LDOs in one package. The smaller package, whether it contains a dual or a single LDO, may have a higher thermal resistance. To summarize, this device dissipates more power (or heat) and is housed in a less efficient thermal package. These conditions are aggressive, but the challenge of dissipating the heat can be worked out as follows.

An example of a dual LDO is the **TC1301B** from Microchip. One of the smaller geometry packages that house this dual LDO is the Dual Flat No Lead package (DFN). A diagram of the DFN package is shown in **Figure 1(a).** This device combines two LDO regulators and a microcontroller RESET function into a single, 8-pin, 3X3 DFN package. Regulator number one (LDO_1) inside this package has a dropout voltage of 104 mV @ 300 mA output current (typical). Regulator number two (LDO_2) has a dropout voltage of 150 mV @ 150 mA (typical). The maximum allowable steady state junction temperature for the TC1301B is 125°C. Thermal shutdown occurs at 150°C.

The TC1301B power dissipation is 780 mW, given the following conditions:

Input Voltage = 4.2V
Output voltage of LDO_1 = 2.8V @ 300 mA
Output voltage of LDO_2 = 1.8V @ 150 mA

The thermal resistance junction-to-ambient ($R_{\theta JA}$) of the DFN package is 41°C/Watt. This DFN thermal resistance specification is based on the 4-layer test method described in the JEDEC JESD51-5 and JESD51-7 standards. In the JESD51 specification, some of the conditions of the test are: 4-layer board, copper thickness of 2 oz. on the outer layers and 1 oz. on the inner layers. There are also two vias from the exposed metal pad to the copper plane (ground plane).

The model in **Figure 1b**. can be used to do first order thermal calculations. This model is put in the simple terms of an electrical system where power is illustrated as a current source, temperature is referenced as a voltage and thermal resistance is illustrated as a resistance. The definitions of the variables in this model are:

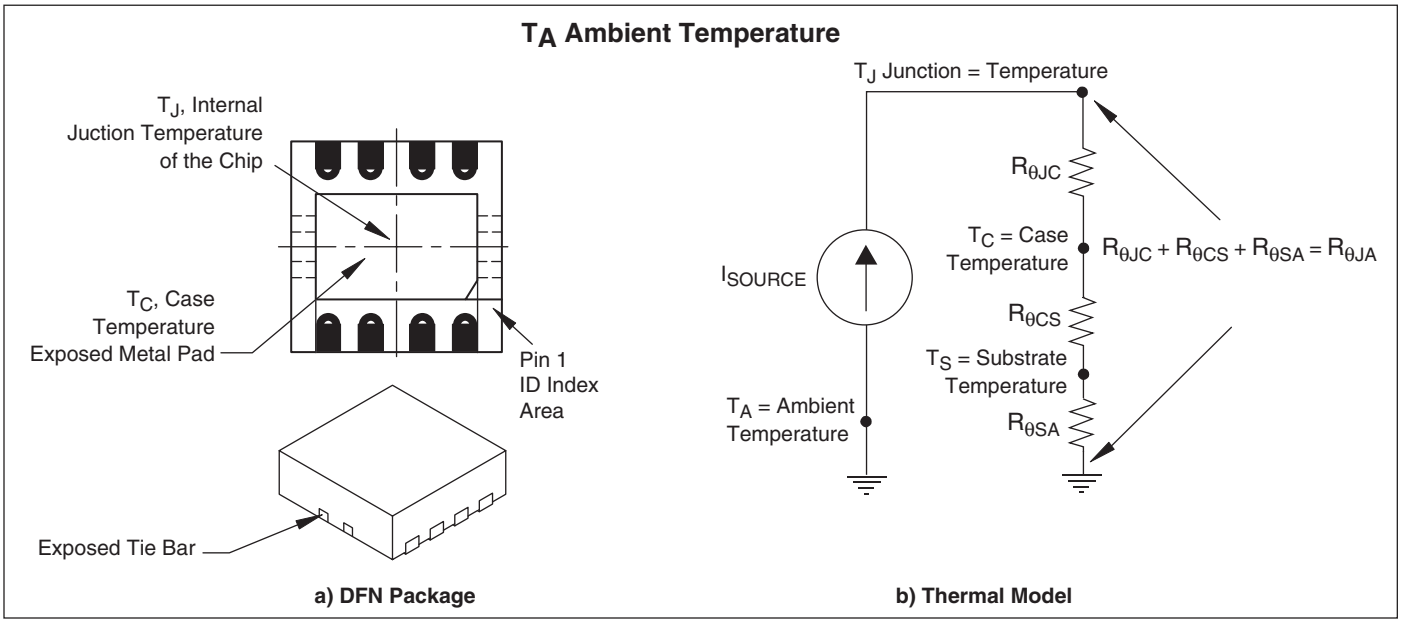

Figure 1. *The dimensions of this DFN package (a) is 3X3 mils. The chip junction temperature (T_J), case temperature (T_C) and ambient temperature (T_A) are used in the package thermal model (b), where $R_{\theta JC}$ is the junction-case thermal resistance and $R_{\theta JA}$ is the junction-ambient thermal resistance.*

I_{SOURCE} = Power in watts

T_J = Chip junction temperature in °C

T_C = Device case temperature in °C

T_A = Ambient temperature in °C

$R_{\theta JC}$ = Thermal resistance from chip junction to device case in °C/Watt

$R_{\theta CS}$ = Thermal resistance from device case to copper ground plane (PC board) in °C/Watt

$R_{\theta SA}$ = Thermal resistance from board copper ground plane to ambient (air) in °C/Watt

Given the above specifications, the rise in temperature at the junction above ambient of the TC1301B is:

$$T_{J(RISE)} = P_{TOTAL} * R_{\theta JA}$$
$$T_{J(RISE)} = 780\ mW * 41°C / Watt$$
$$T_{J(RISE)} = 32°C$$

The thermal resistance from junction to ambient with a 2-layer board with no vias to the copper ground plane can be as high as 150°C/Watt. With this type of layout the capacitors are connected using vias to the copper ground plane without consideration to thermal issues. Under these conditions, the rise in junction temperature is:

$$T_{J(RISE)} = P_{TOTAL} * R_{\theta JA}$$
$$T_{J(RISE)} = 780\ mW * 150°C / Watt$$
$$T_{J(RISE)} = 117°C$$

If this simple 2-layer layout is used in an ambient environment of 25°C, the junction temperature would exceed specification limits.

A feasible 2-layer layout for the TC1301B is shown in **Figure 2**. The board construction is a 0.0625" FR4 substrate with 1 oz. copper traces. The traces reside on the top layer (as shown in Figure 2) and the copper ground plane is on the bottom. The copper plane is accessed through vias. The required 1 µF capacitors (ceramic, tantalum or aluminum electrolytic) are attached as close a possible to the output pins of both LDOs. Using this board design results in a junction-to-ambient thermal resistance ($R_{\theta JA}$) of 78ºC/W.

With the layout in Figure 2, the rise in temperature under full load conditions of the **TC1301B** is increased from 32°C (4-layer with vias) to 59°C. This change in temperature is primarily due to lack of internal layers and an additional via directly into the copper plane, as defined by the JEDEC standard.

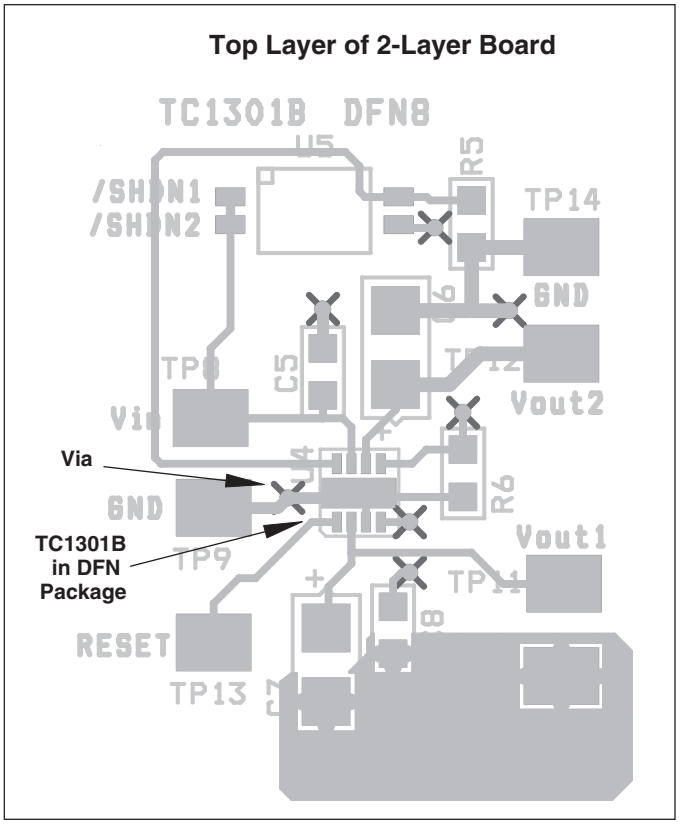

Figure 2. *This is the top layer of a 2-layer board. High junction temperatures under full-load conditions can be lowered by connecting the exposed metal pad on the bottom of the DFN package to the copper ground plane.*

The TC1301B is one of a family of four dual LDOs; **TC1301A, TC1302A** and **TC1302B**. The key difference between these options are summarized in the following table.

Device	LDO_1 Shutdown Pin	LDO_2 Shutdown Pin	Voltage Detect	Microcontroller RESET (300 ms)
TC1301A	—	X	X (pin 8)	X
TC1301B	X	X	Tied to V_{OUT1}	X
TC1302A	—	X	—	—
TC1302B	X	X	—	—

Recommended References:

AN792: *"A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application",* Cleveland, Terry, Microchip Technology

Dual LDO with Microcontroller RESET Function, TC1301A/B, Microchip Technology, Inc., DS21798

Low Quiescent Current Dual Output LDO, TC1302A/B, Microchip Technology, Inc., DS21333

"Testing the Junction Temperature of Small Outline Packaged Devices", Cleveland, Terry, December 17, 2003, WebSeminar, www.microchip.com

"*MLP Application Note: Comprehensive User's Guide* (MLP, Micro Leadframe Package)", Carsem, April 2002

JEDEC Standards JESD 51-5, 51-7