AVR 32 | 32-BIT MCU/DSP

AP7000

HIGH PERFORMANCE

LOW-POWER

APPLICATION PROCESSORS

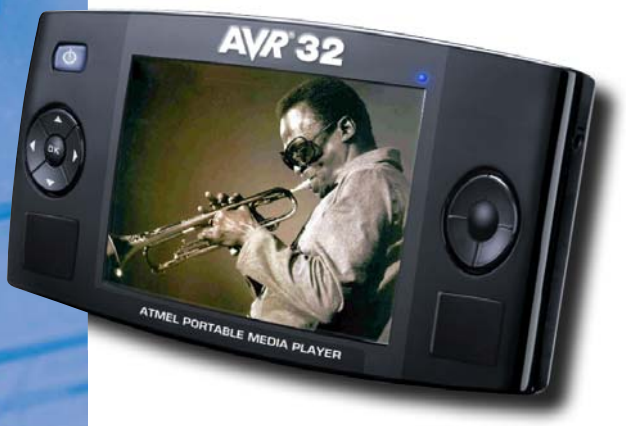
Redefining Performance

ATMEL

Embedded Market Demand

Whether hand-held or automotive, today's consumer infotainment applications have two things in common: they are required to execute computationally intensive DSP algorithms and they must consume a minimal amount of power.

Most traditional processors were developed in the 1970's and 1980's, before the advent of MP3 players, digital video, GPS, voice recognition or, most importantly, small footprint, battery-powered, hand-held products. The only way for 20th century processors to meet 21st century performance requirements is to turn up the clock rate. Unfortunately, turning up the processor clock also increases power consumption and heat dissipation.

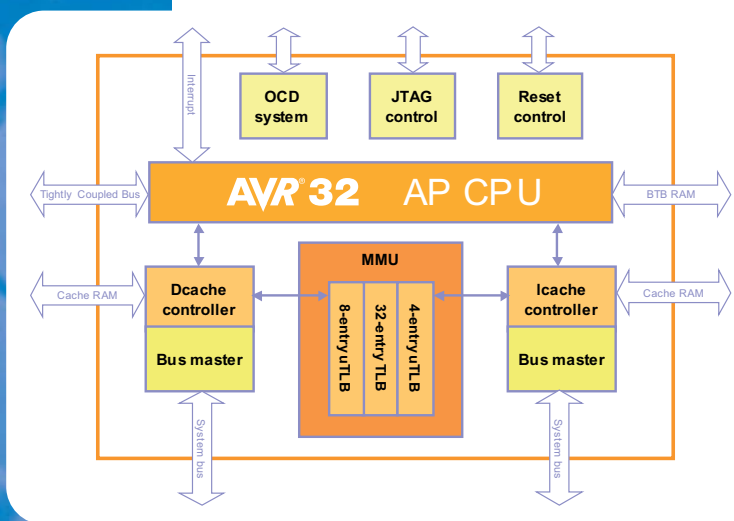


As DSP-based features proliferate, turning up the processor clock will result in power consumption that is incompatible with today's demand for products that fit in the palm of your hand and that can operate without recharging for a day or longer.

21st Century Architecture:
High Throughput with a Slow Clock

Introducing AVR32

Atmel has created the first processor architected specifically for 21st century applications. The AVR®32 32-bit RISC processor core is designed to do more processing per clock cycle so the same throughput can be achieved at a lower clock frequency.



In fact, the AVR32 CPU executes about three times as much processing per clock cycle as its nearest competitor. This means the compute intensive algorithms required for today's applications can be executed at a lower clock rate, with substantially less power consumption.

During the development of the AVR32, Atmel has filed over 18 patents on the innovative techniques used to optimize the architecture. The AVR32 core minimizes penalties from load/store and branch operations and maximizes pipeline throughput, allowing complex algorithms to be executed with a much lower clock frequency and power consumption than comparable processors.

For example, the AVR32 can execute quarter-VGA MPEG4 decoding at 30 frames per second (fps) running at less than 100 MHz including audio layer (Mplayer on Linux® platform) while comparable architectures require 260 MHz and more to decode the same movie stream.

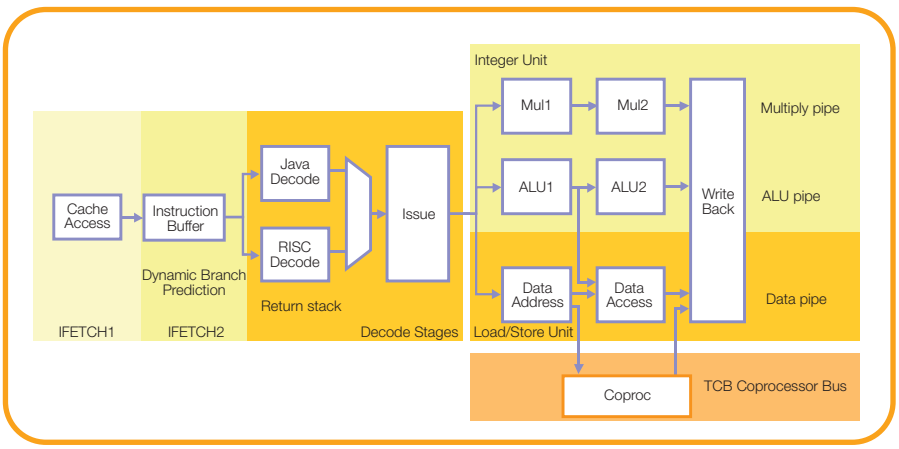
In addition to the technical advantages of the AVR32, one of the major benefits of this new core is to rely on a license-free model. AVR32 is an Atmel Intellectual Property (IP) that will be used to develop general purpose microcontrollers as well as specific or custom ICs.

> "Traditionally chip vendors have increased processing power by making processors run faster. This is a real issue for portable devices because turning up the clock directly increases power consumption and reduces battery life; the approach we have taken with the AVR32 is to increase the amount of processing the processor can do internally and actually turn the clock frequency down. Although it's difficult to digest the notion that a processor could be more powerful using fewer clock cycles, that is exactly what we are doing."
>
> Øyvind Strøm, PhD
>
> *AVR32 Lead Designer*

Multiple Pipelines Support Out-of-Order Execution

The AVR32 AP CPU has a 7-stage pipeline with 3 sub pipelines (multiplication/MAC, load/store, and ALU) that allow arithmetic operations on non-dependent data to be executed, out-of-order and in parallel.

A conventional architecture has a single pipeline that stalls the code until each instruction is completed. This can waste valuable computational resources during multi-cycle instructions. Logic in the AVR32 AP pipeline allows non-dependent instructions to be executed simultaneously, using available pipeline resources. Out-of-order execution can increase the throughput per cycle. Hazard detection logic detects and holds dependent instructions at the beginning of the pipeline until the operation on which they depend is complete.



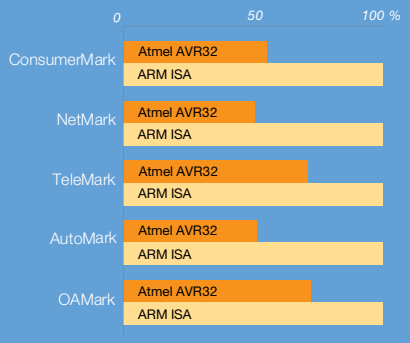
AVR32 AP Outperforms Major 32-bit Architectures

The AVR32 AP core consistently outperforms major high-end 32-bit standard MCU cores in every EEMBC® benchmark for performance and code density.

In EEMBC benchmarks, AVR32 code consistently requires 5% to 20% less code than the ARM® Thumb® instruction set to execute the same functionality. More significantly, for high-performance applications, when optimized for speed of execution, AVR32 code is 30% to 50% more compact.

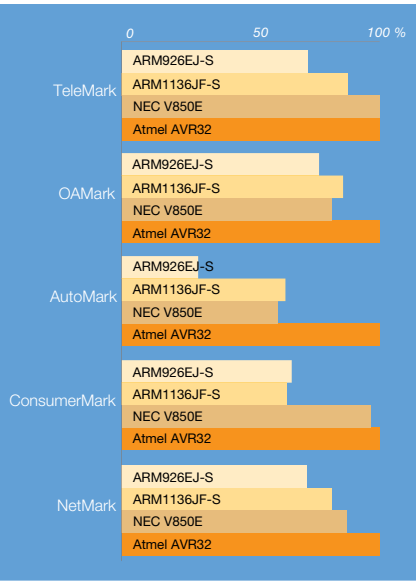
AVR32 performance-optimized code density is also consistently better than that of the ARM Instruction Set Architecture (ISA) in every EEMBC benchmark.

EEMBC code size benchmarks are based on publicly available numbers from EEMBC (www.eembc.org), based on ARM's simulated numbers for the ARMv5 Thumb ISA. AVR32 code was compiled with the IAR AVR32 2.09 compiler while ARM-code was compiled with ARM's ADS 1.2 compiler.



EEMBC code size benchmarks

The advantage of the AVR32 in regards to code size with a lower value indicating better performance.



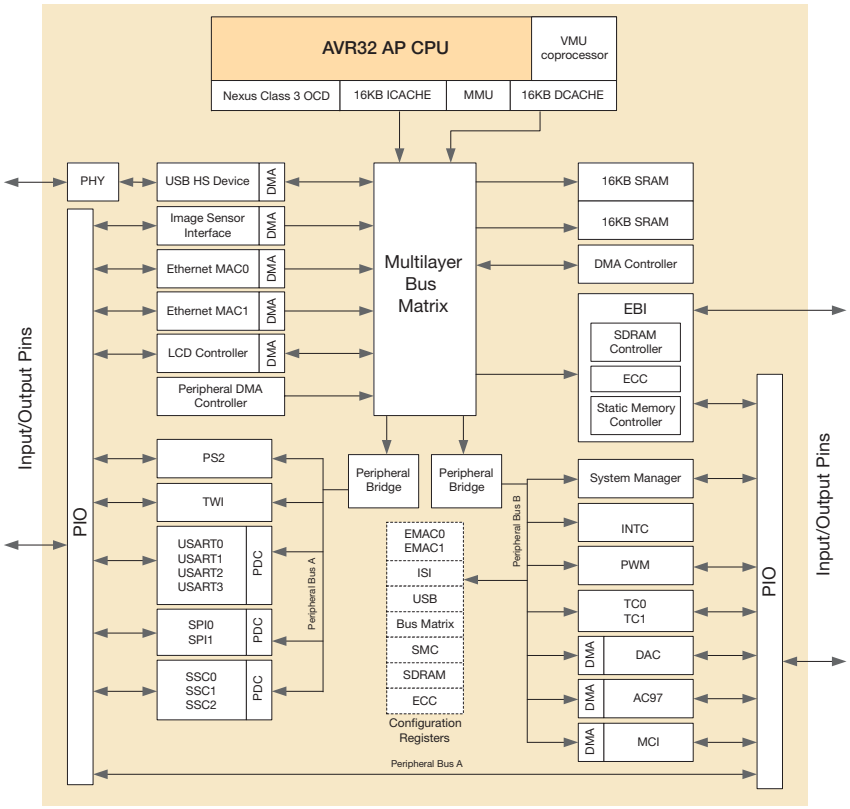
EEMBC performance benchmarks

The architectural performance when comparing CPU cores with a higher value indicating a better performance

The AVR32 AP consistently outperforms both ARM9™, ARM11™ and NEC V850E cores in EEMBC's TeleMark™, OAMark™, AutoMark™, ConsumerMark™ and NetMark™ benchmarks. Its performance exceeds that of the ARM11 by over 35% on the ConsumerMark benchmark.

The EEMBC benchmark numbers are normalized to the same clock frequency. The ARM926EJ (based on the Freescale i.MX21 values using GCC 3.3.2), ARM1136JF (based on the Freescale i.MX31 values using GCC 3.4.3) and NEC V850E (using Green Hills multi 2000 4.0.1 compiler) ***benchmark data can be found at the EEMBC website (www.eembc.org).***

The AP7000 is the first AVR32-based processor family and the first to integrate on a single chip, virtually all the functionalities required for multimedia systems deployed in cell phones, digital cameras, PDAs, automotive infotainment, set top boxes, and home entertainment systems, as well as network switches/routers and printers.



Vector Multiplication Coprocessor

- 10x Image scaling optimization
- YUV<->RGB hardware convert

LCD-controller

- 640x320 and 320x240 TFT/STN
- Maximum 2048x2048 TFT

Image Sensor Interface

- VGA and CMOS-cameras

Audio Interfaces

- 16-bit stereo audio-DAC
- I2S/AC'97 digital i/f

Connectivity

- USB 2.0 480 Mbps PHY
- Ethernet MACB (optional)
- True-IDE Hard-drives
- CF/SD/MMC
- IrDA, 3xSPI, I2C, 3xSSC, 4xUSART

AVR32 AP7000 BENEFITS

- Reduced power consumption and heat dissipation
  - Reduced CPU clock frequency
  - Higher throughput / MHz
- Ease of development
  - Well-featured, industry standard development tools and OCD system
- Higher Performance
  - Zero-cycle branches
  - SIMD DSP instructions
  - 186 innovative RISC instructions
  - 7-stage pipeline with parallel out-of-order execution
  - Exceptional code-density reduce cache-misses and increase throughput

The AT32AP7000 device is available now and the AP70xx family will progressively expand in 2006.

	AT32AP7000	AT32AP7001	AT32AP7002
USART, I2C, SPI and SSC ports	Yes	Yes	Yes
SD/MMC	Yes	Yes	Yes
EBI (SRAM, SDRAM, NF...)	Yes	Yes	Yes
Ethernet MAC	2	0	0
USB High Speed	Yes	Yes	Yes
Camera Interface	Yes	Yes	Yes
LCD Controller	Yes	No	Yes
Audio (DAC, I2S, AC97)	Yes	Yes	Yes
Package	256-pin BGA	208-pin QFP	196-pin BGA

AP7000 Features

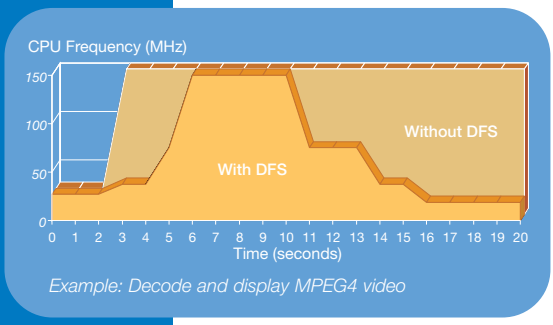
Vector Multiplication Coprocessor

Multimedia applications commonly require arithmetic operations on 3x8-bit matrices for image filtering (FIR filtering), image color-space conversion (RBG<->YUV), image scaling, and MPEG-4/H.264 Quarter Pixel Motion Estimation. In order to keep CPU throughput as high as possible, the AP7000 has integrated the vector multiplication unit (VMU) to the AVR32 AP co-processor interface, tightly coupled to the CPU.

For example, MPEG4 video is compressed using the YUV color space, while most video DACs and LCD controllers require RGB input. The vector multiplier co-processor executes this conversion in real-time without CPU intervention. When used for image scaling operations, the AP7000's vector multiplication co-processor increases the performance by as much as ten times.

Direct Memory Access (DMA)

Managing data-intensive applications with streams of data passing between the peripherals and the memories can seriously compromise the CPU. Without DMA, the 100 Mbps Ethernet MACBs and the 480 Mbps USB slave controller would take up all the CPUs cycles. The AP7000 provides several flexible Direct Memory Access (DMA) mechanisms that offload, from the CPU, data transfers between peripherals and memory and between two memory locations in the chip. Two simultaneous memory-to-memory data transfers can be performed between on-chip SRAM, or off-chip memories connected to the chip's external bus interface (EBI), as they are all addressable to the DMA controller.



Example: Decode and display MPEG4 video

Dynamic Frequency Scaling of Four Clock Domains

The AP7000 architecture has a multi-layer, high-speed bus architecture that increases performance by allowing multiple operations to take place in parallel. In addition, there are two peripheral bus bridges that allow different clock frequencies to be set for high- and low-speed peripherals. In a conventional bus structure, the bus clock is determined by the fastest peripheral, such that slower peripherals that could operate on a slower bus, draw unnecessary power. The AP7000 allows the dynamic configuration of the individual clock frequencies of these two bridges, as well as the frequency of the CPU's internal clock and that of the bus matrix.

Dynamic frequency scaling algorithms are used to set the clocks in each of the four domains at the lowest possible frequency for the function it is performing.

System-on-Chip for Portable Multimedia Players.

The AP7000 is a real System-on-Chip (SoC) solution for Portable Multimedia Application, achieving an exceptional performance with low power consumption. For example, streaming a 320x240 MPEG movie over the AP7000's on-chip Ethernet MAC at 100 Mbit/s and decoding it at 30 frames per second requires a CPU clock of only 120 MHz and system bus clocks of only 60 MHz. The processor also simultaneously runs a full Linux operating system and drives a QVGA TFT LCD with these clock frequencies. Total AP7000 power consumption for this application is only 250 mW.

SINGLE PROCESSOR TOOL FLOW - COMPLETE AND POWERFUL TOOL SET

Unlike multi-core processor solutions, the AP7000 has a single development environment for straightforward debugging. The AVR32 Instruction Set Architecture (ISA) is specifically designed for high-level programming languages like C, C++ and Java®. Compilers with C, and C++ support include GNU GCC and IAR Embedded Workbench®. The compilers are able to utilize the AVR32 architecture's SIMD and DSP instructions from within the C/C++ programming environment.

The IAR compiler is optimized to recognize patterns in the C-code that can use SIMD and DSP instructions, thus further increasing the ease of use and performance when running compiled C-code applications. Both compilers support access to inline assembly for tight-loop / inner-loop algorithmic optimizations.

GCC and GNU Debugger (GDB) are available directly from Atmel and plug directly into many Integrated Development Environments, including the Eclipse™ debug environment.

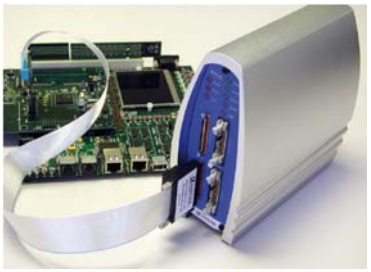
The AP7000 has a fully supported Linux 2.6 kernel supported by Atmel to further ease the transition of existing code or the adoption of the many hundreds of thousands of free open source applications available for embedded systems.

The STK®1000 provides a complete development environment. Priced at $499 this kit comes with dual ethernet ports, a high quality QVGA LCD display, VGA connector and USB connectors. The PCI style expansion header can be used for prototyping purposes. The kit comes with a 256 MB SDcard with a pre-installed Linux image enabling the user to boot Linux on the target and start program development within few minutes after powering up the card.

The AVR JTAGICE mkII emulator supports AVR32 and can be used together with the STK1000 either with GCC or the IAR compiler. The JTAGICE mkII supports basic runtime control and a limited trace capability through the JTAG interface.

The AP7000 is also supported by the Vitra and the Opella products from Ashling. This provides high-end debugging capabilities as sustained trace and SQA (software quality assurance).

An extensive white paper is available from Ashling at www.ashling.com



MPEG4 software decode - 75 MHz

- 30 fps QVGA (320x240) MPEG-4
- 3x performance vs ARM926

Audio software decode

- MP3 audio at 15 MHz CPU
- AAC ~25 MHz CPU

Vector Multiply Unit (VMU)

- Hardware color-space conversion (YUV<->RGB24)
- Image scaling 10X acceleration

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