ANALOG DEVICES

AN-928
APPLICATION NOTE

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# Understanding High Speed DAC Testing and Evaluation

by Justin Munson

## SCOPE

This application note describes the test methods used by the Analog Devices, Inc., High Speed Converter group to characterize the performance of high speed digital-to-analog converters (DAC). This application note should be used as a reference when evaluating a high speed DAC in conjunction with the appropriate device data sheet.

## DYNAMIC TEST HARDWARE SETUP

The typical hardware setup for testing alternating current (AC) conditions such as spurious-free dynamic range (SFDR), intermodulation distortion (IMD), and noise spectral density (NSD) is shown in Figure 1. The basic setup for the dynamic testing includes a sine source for the DAC clock, low noise power supplies, a spectrum analyzer, and a data pattern generator. Various types of pattern generators can be used to drive either CMOS or LVDS data into the DACs, ranging from arbitrary waveform generators (AWG) to field programmable gate arrays (FPGA). Analog Devices also provides a data pattern generator to aid in the bench evaluation.

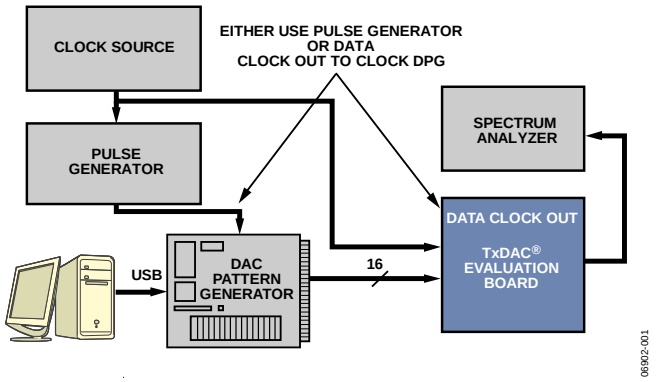


*Figure 1. Typical AC Characterization Test Setup*

## DATA PATTERN GENERATOR 2 (DPG2)

The data pattern generator 2 (DPG2) is designed to simplify the evaluation of Analog Devices high speed DAC products. A block diagram of the DPG2 is shown in Figure 2. The DPG2 provides two channels of 16-bits each and supports both LVDS and CMOS standards. The maximum sample rate on each channel in LVDS mode is 1.25 GSPS and 250 MSPS in CMOS mode.

The DPG2 provides up to 512 MB of RAM to allow for complex waveform generation. There is also the capability to synchronize up to four DPG2s together using a HSC-DAC-DPG-CLKDIS board, along with one Samtec HQCD-030-15.00-TED-TEU-1 cable for each DPG2.

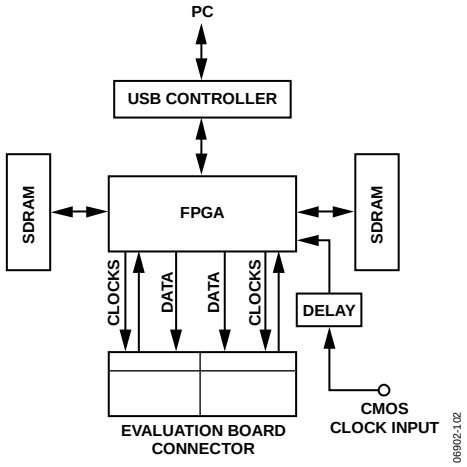


*Figure 2. DPG2 Block Diagram*

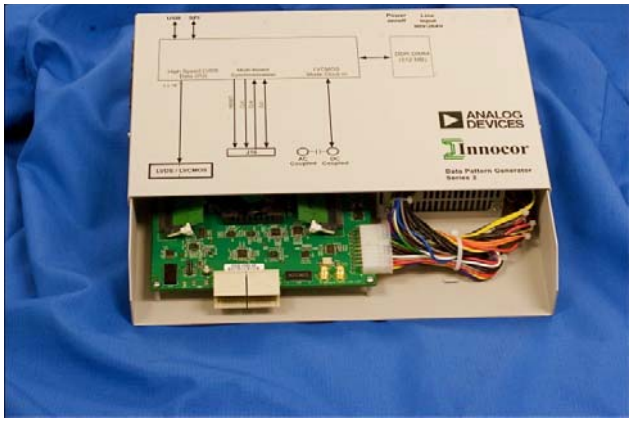


*Figure 3. DPG Board*

Software is provided with the DPG2 to allow the user to generate single- and multitone sine waves, various CMTS waveforms, various WIFR standards, and static DC patterns as well as to load a user-generated pattern,

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## REVISION HISTORY

**11/10—Rev. 0 to Rev. A**

Replaced DPG with DPG2 Throughout ..... Universal
Replaced Figures Throughout ..... 1
Replaced LabVIEW Executables for Vector Generation Section with DPG Downloader Software Suite Section ..... 3
Changes to Power Supplies Section ..... 7

**3/08—Revision 0: Initial Version**

# EQUIPMENT FOR DAC BENCH SETUP

This section discusses the hardware and software required to properly characterize high speed DACs.

Analog Devices provides a DPG2 to aid in the bench evaluation. Patterns to exercise the DAC can be generated by using the DPG Downloader software suite provided with the DPG2.

## DPG DOWNLOADER SOFTWARE SUITE

To evaluate a DAC properly, a user must be able to generate single- and multitone continuous wave (CW) patterns, as well as patterns for various communication standards. All of the patterns can be generated using the DPG Downloader software. The user interface for the DPG Downloader is shown below in Figure 4.

The DPG Downloader can automatically determine which evaluation board is connected and configure the correct data port configuration via the USB cable connected to each evaluation board. The software also detects the data clock frequency, which is either transmitted across the data bus connector for LVDS interfaces, or through the SMA connectors for CMOS interfaces (J12 or J13 on the DPG2 main board).

All of the available waveforms that can be generated via this software can be found under the **Add Generated Waveform** pull-down menu as shown in Figure 4. A user can also load their own generated vector via the **Add Data File** option found in the top left corner. The following sections describe the steps to generate each of the vectors in the **Add Generated Waveform** menu.

### *Single Tone*

Upon selecting the **Single Tone** option from the menu, a single tone vector block appears as shown in Figure 5. The variables that are adjustable for this vector are as follows:

- **Sample Rate**
- **Desired Frequency**
- **DAC Resolution**
- **Record Length**—must be divisible by 256
- **Offset**—constant offset added to every code generated
- **Amplitude**
- **Relative Phase—** can be used if generating I and Q vectors

### *Multi-Tone*

Upon selecting the **Multi-Tone** option from the menu, a multi tone vector block appear as shown in Figure 6. The multi-tone generation has many of the same variables as the single tone block. The main difference between the two functions is that the Add Tone button is selected (circled in Figure 6) to specify the number of tones, tone spacing, and start frequency.

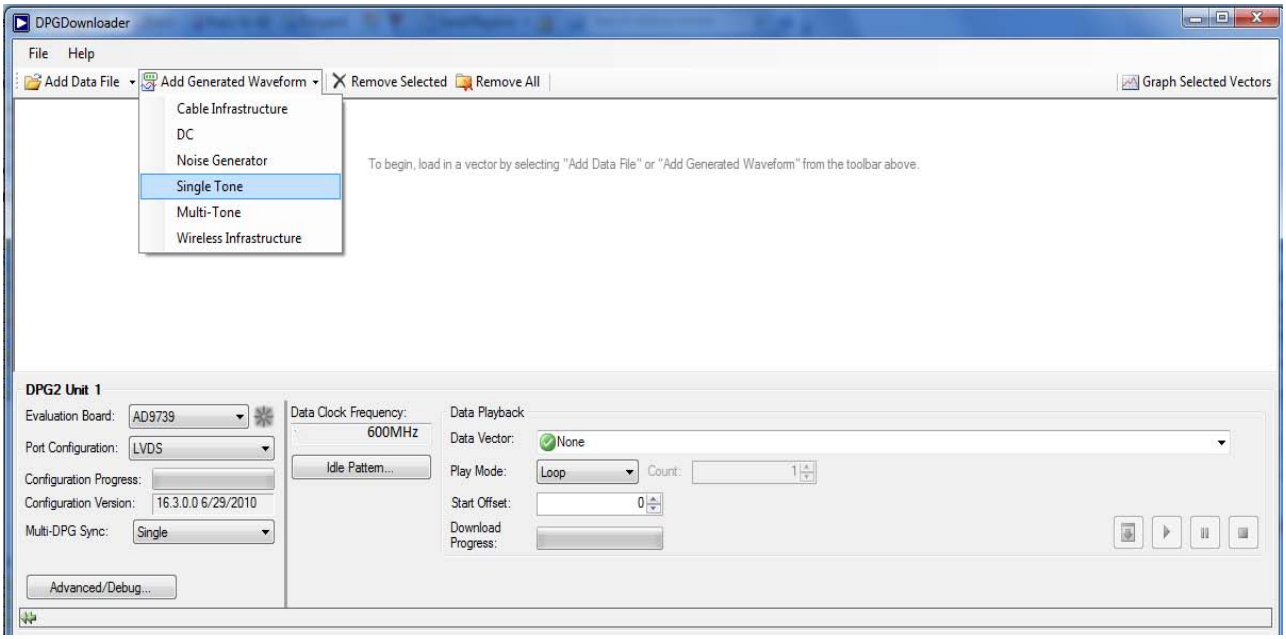



Figure 4. DPG Downloader Front Panel Interface

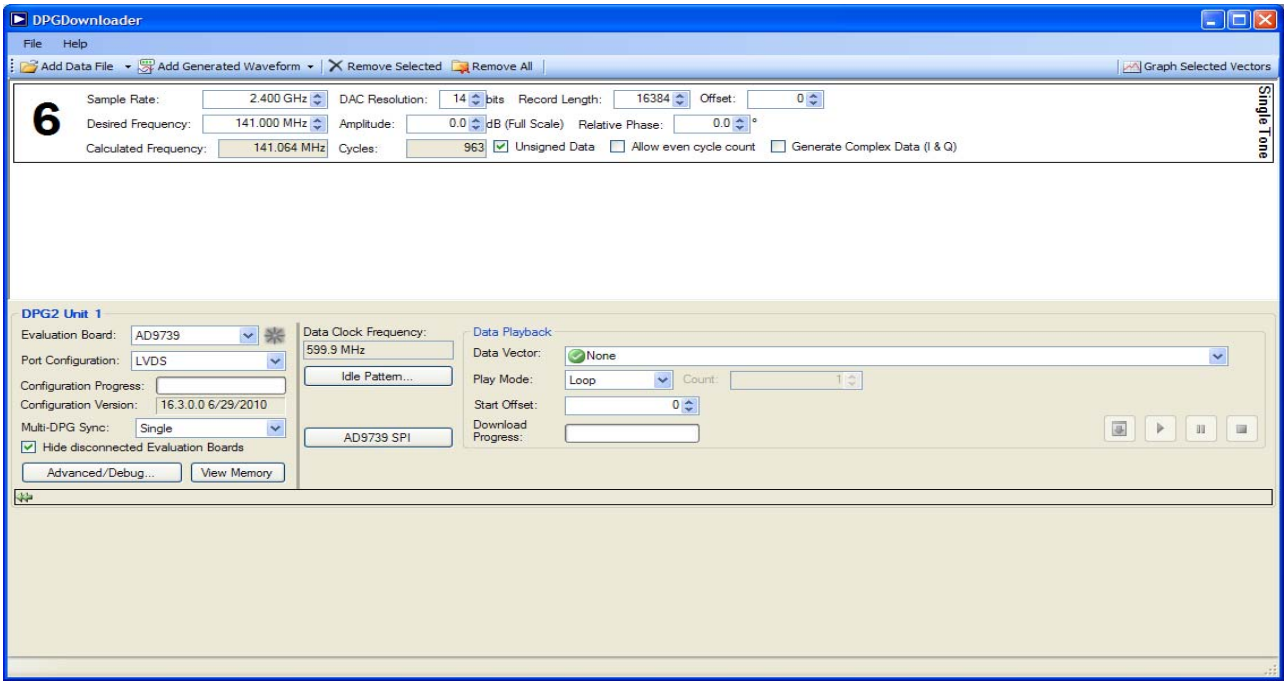



*Figure 5. Single Tone Vector Generation*

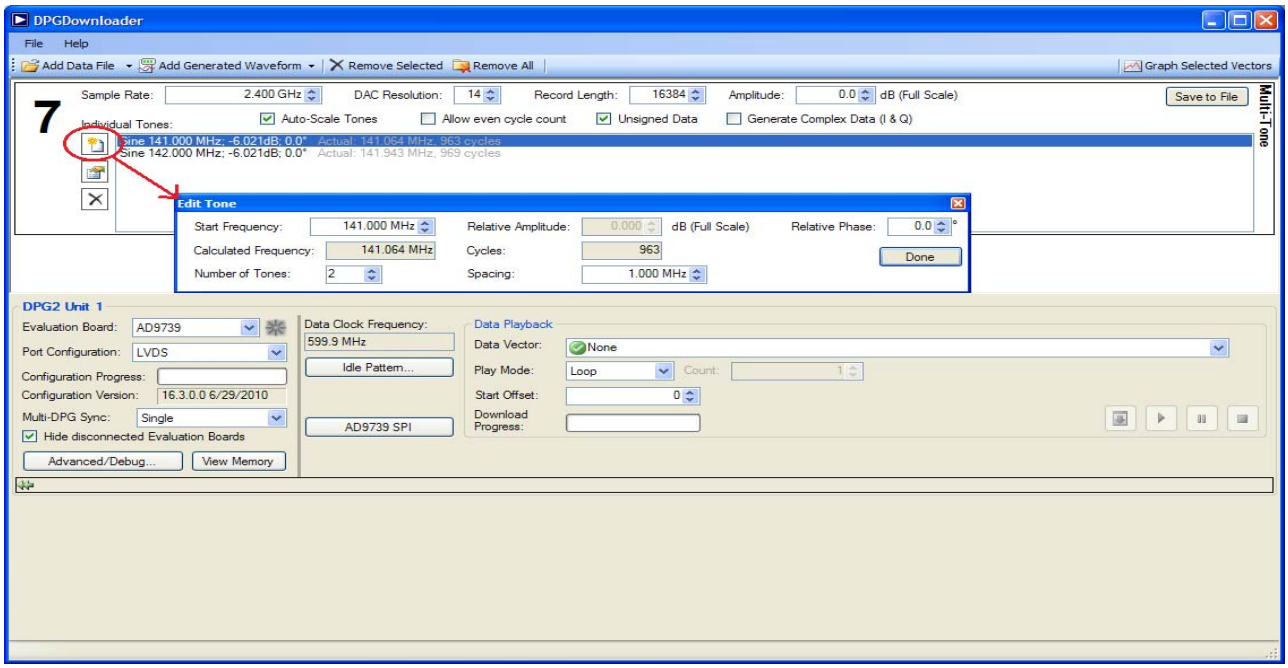



*Figure 6. Multi-Tone Vector Generation*

### *DC Pattern*

The dc pattern option allows the user to load in a constant static value or a pattern of alternating values and zeros. The dc pattern generator block is shown in Figure 7.

### *Noise Generator*

The noise generator function allows the user to generate a pattern for various types of random noise patterns such as Gaussian, uniform, or white noise. The noise generator block is shown in Figure 8.

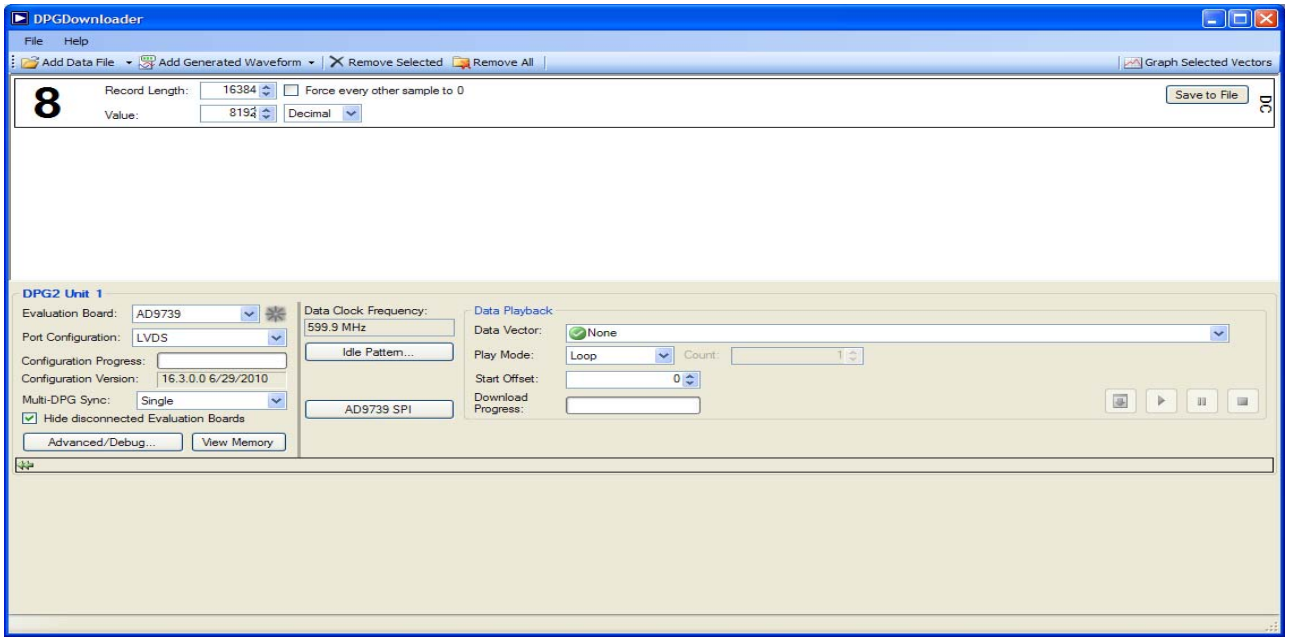



*Figure 7. DC Vector Generation*

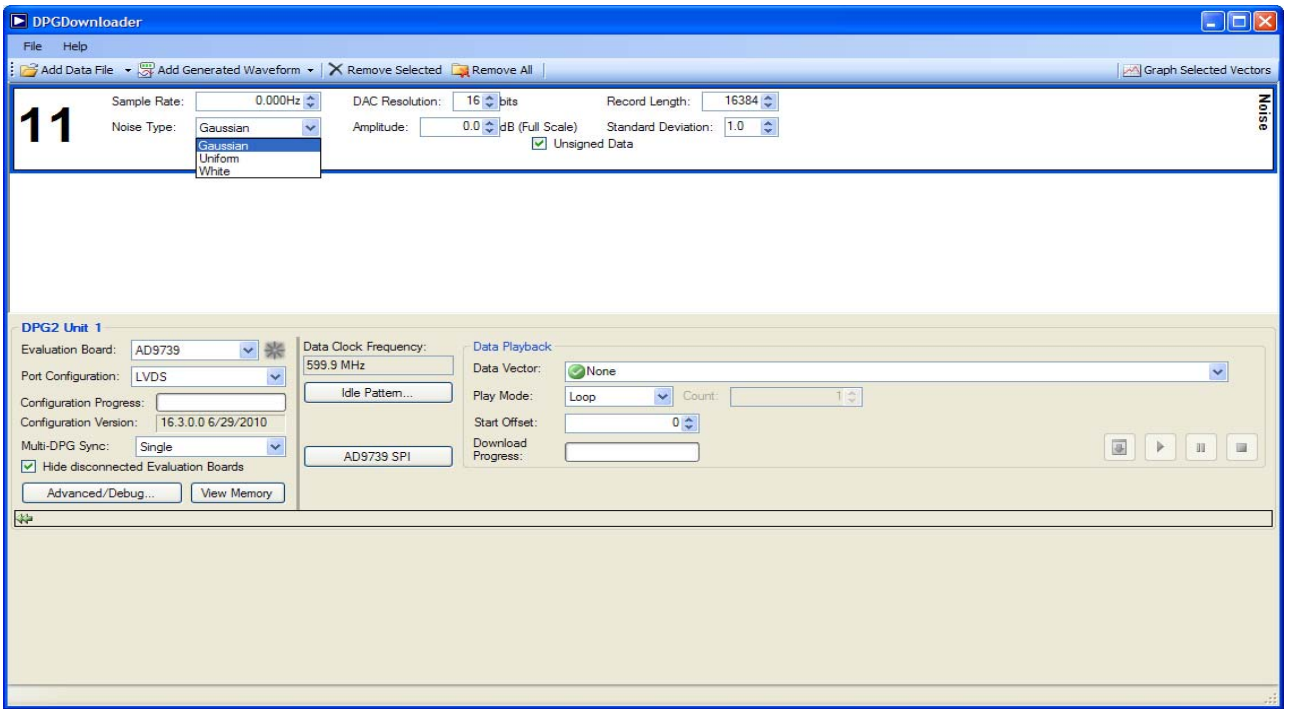



*Figure 8. Noise Vector Generation*

### *Cable Infrastructure*

The cable infrastructure block is shown in figure 9. This block allows the user to create various CMTS vectors using the standard pull-down menu, such as US64QAM, US256QAM, US64QAM, and EU256QAM. The symbol rate is automatically selected depending on which standard is chosen. The user can also select the number of channels to be generated in the vector.

### *Wireless Infrastructure*

The wireless infrastructure block is shown in figure 10. This block allows the user to create various WIFR vectors using the standard pull-down menu, such as WCDMA, GSM, and CDMA2K. The carrier spacing is automatically selected depending on which standard is chosen. As was the case with the CIFR block, the user can select the number of carriers to be generated.

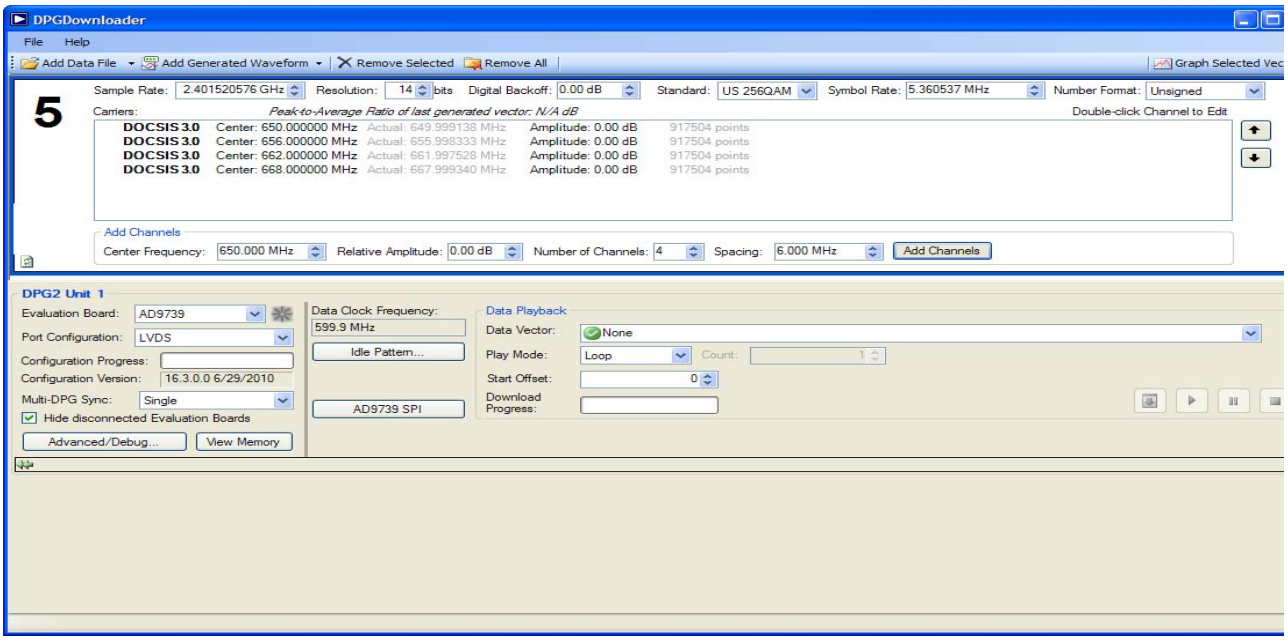



*Figure 9. Cable Infrastructure Vector Generation*

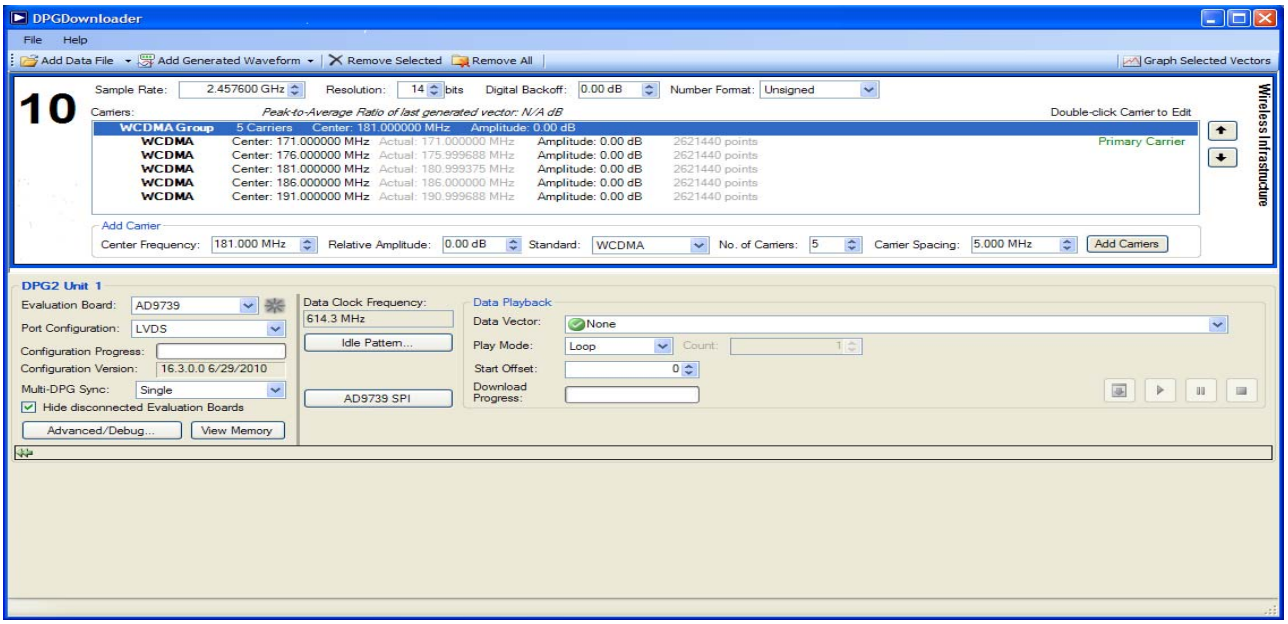



*Figure 10. Wireless Infrastructure Vector Generation*

## DAC CLOCK SIGNAL SOURCE

Depending on the clock speed and desired performance, the dynamic test setup uses either an Agilent E4426B ESG-AP/8644 or a Rohde & Schwarz SML01/SML02/SMA100A generator to provide the clock for the DAC. These generators can provide clock frequencies from several kHz to several GHz depending on the DAC under test.

All of these sources provide very low phase noise and good jitter performance. The phase noise, especially at offsets further away from the carrier frequency (5 MHz to 10 MHz), has a large impact on the overall achievable noise performance of the DAC. Some sine sources can provide exceptional noise performance at lower frequencies and worse performance at higher frequencies or vice versa. For more information on the impact of the phase noise of the sine source on the noise performance of the DAC, see the Noise Spectral Density section.

## SPECTRUM ANALYZER

To analyze the dynamic performance of the DAC, a spectrum analyzer is employed. The two analyzers used by Analog Devices to characterize the DACs are the Agilent E4443A PSA spectrum analyzer and the Rohde & Schwarz FSEA30 spectrum analyzer.

The Agilent PSA has many features that make it ideal for DAC dynamic testing, including adjacent channel power ratio (ACPR) measurement capability, channel power measurement used to measure noise spectral density (NSD), phase noise measurement capability, demodulation functions, and optional personalities for various wireless communication standards. The PSA also has an optional internal preamplifier to aid in measuring NSD. For more information on this function, see the Noise Spectral Density section.

The harmonic distortion of the analyzer is also important when measuring the spurious performance of the DAC. The harmonic performance of the analyzer depends on several settings: the settings of the RF attenuation, resolution BW, and reference level, as well as the setting of the input level of the CW signal being measured. If the spurious performance of the DAC is lower than the HD2 and HD3 of the analyzer for a specified setting, external methods must be employed to properly measure the performance of the part. For more information about optimizing the spectrum analyzer for harmonic measurements, see the Single-Tone, In-Band, Spurious-Free Dynamic Range section.

## DIGITAL MULTIMETER

A digital multimeter (DMM) measures the majority of the direct current (DC) parameters for the DAC. The Agilent 3458A is a good choice when trying to measure direct current parameters with precise accuracy.

The 3458A offers up to 8.5 digits of resolution and various range settings (5 ranges for DC volts: 0.1 V to 1000 V and 8 ranges for DC current: 100 nA to 1 A), making it ideal for measuring the offset of the DAC or DAC segments in the nA to µA region. The Agilent 3458A can be used to measure the direct current out of the DAC, or an external current to voltage converter (I-V) circuit can be used to measure voltage rather than current. The I-V circuit used for DC testing is shown in Figure 11. The overall gain of this circuit is 100; a 20 mA full-scale (FS) current converts to a 2 V signal.

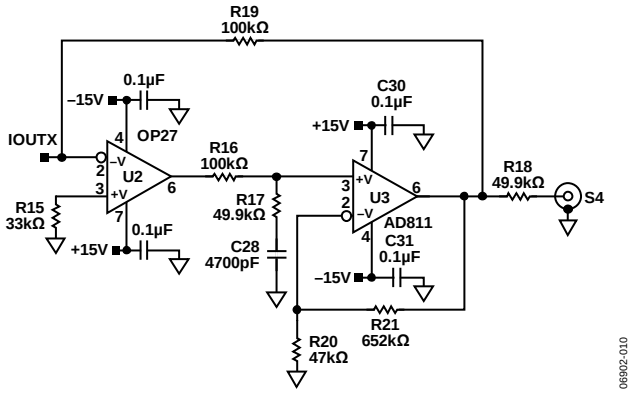



*Figure 11. I-V Converter Circuit*

## POWER SUPPLIES

It is important to provide clean, quiet power supplies to optimize the alternating current (ac) performance and lower the power supply rejection ratio (PSRR) for DACs.

Two solutions can be employed on a DAC evaluation board: direct power using an Agilent E3631A programmable triple output power supply or regulated power supplies using the ADP3333, ADP3338, and ADP3339 LDO regulators. The ADP series regulators provide very low noise and well regulated sources for a variety of supply voltages.

The typical application circuit for the ADP3339 is shown in Figure 12.

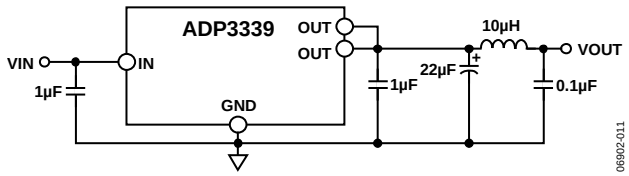



*Figure 12. ADP3339 Typical Application Circuit*

Another option to supply power to a high speed converter is to use dc-to-dc converters in place of the linear regulators. If proper care is taken with power supply decoupling, dc-to-dc converters can provide the same level of spectral purity with greater efficiency than linear regulators. For more information on this topic, see CN-0141.

# AC TEST DEFINITIONS

AC testing is usually made with the analog signal at about 0 dBm, which for most of the DACs in the portfolio is done using an analog full-scale value of approximately 20 mA. For DACs with adjustable full-scale currents via either an external resistor or internal gain adjust DAC, testing is performed at various gain values to determine how the performance of the parts scales with the analog output power. Testing is also performed with respect to temperature and analog supply voltage. Consult the specific device data sheet to determine the test conditions under which the AC testing is performed.

## SINGLE-TONE, IN-BAND, SPURIOUS-FREE DYNAMIC RANGE

The spurious-free dynamic range (SFDR) is the difference, in dBc, between the peak amplitude of the output signal and the peak spurious signal over the specified Nyquist bandwidth. Typically, the dominating spur is a harmonic, usually the second or third harmonic of the input signal. The major problem that arises when measuring the SFDR for a DAC is optimizing the spectrum analyzer to measure the true harmonic performance of the DAC and not of the spectrum analyzer itself.

Several controls on the spectrum analyzer can be used to try to optimize the measurement: RF attenuation, reference level, and sweep time. RF attenuation, the most critical parameter, optimizes the input level into the first mixer stage of the spectrum analyzer to avoid overloading the mixer stage and causing unwanted distortion. The reference level controls the IF gain stage after the mixer. This is coupled to the RF attenuation, but changing the reference level does not affect the signal level at the input of the mixer, only on the display. The final parameter is the sweep generator, which is controlled by the resolution bandwidth and sweep time. These parameters optimize the time it takes to take the measurement and have an effect on how accurately one can measure the true noise floor of the DAC.

RF attenuation is the key parameter when measuring the harmonics of a DAC, especially in the presence of a full-scale single-tone sine wave. Figure 13 and Figure 14 show the DAC synthesizing a 10 MHz sine wave, with two different settings for RF attenuation.

In Figure 13, RF attenuation is set to 30 dB. Note that it is obvious that RF attenuation is too high, which causes the mixer level internal to the analyzer to be too low. This setting causes the signal-to-noise ratio of the input signal to be unnecessarily reduced.

Setting RF attenuation to 20 dB (see Figure 14) causes the analyzer to add unwanted distortion to the measurement and causes over-loading of the input mixer stage. This means that the true harmonic performance of the DAC is not being measured.

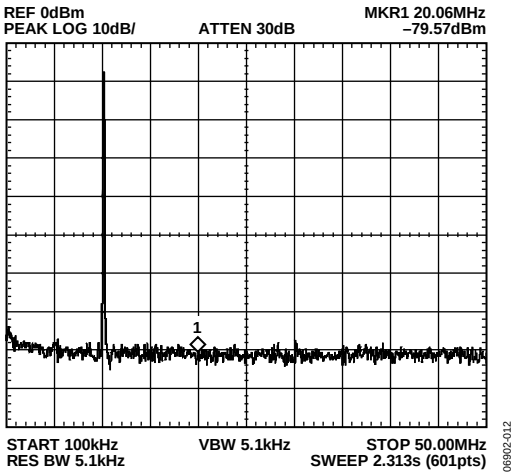



*Figure 13. DAC Output with 30 dB RF Attenuation*

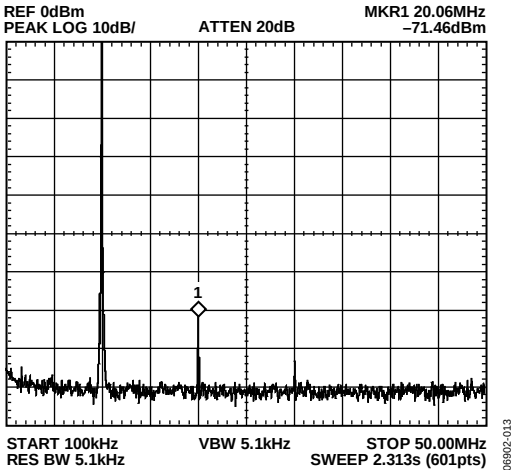



*Figure 14. DAC Output with 20 dB RF Attenuation*

Optimization of RF attenuation is especially key when measuring spurious performance in the 80 dBc to 100 dBc range. At these levels, the spurious performance of the DAC is usually better than the spurious performance of the analyzer itself at the specified RF attenuation setting. One way to ensure that the analyzer is measuring the true performance of the DAC converter is to use a notch filter between the converter output and the spectrum analyzer as shown in Figure 15. Using a notch filter allows the user to bring the RF attenuation level down to zero (because the signal level out of the notch is attenuated by almost 60 dB) and to bring the reference level down to zoom in closer to the actual harmonics.

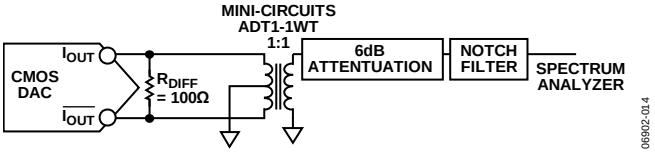



*Figure 15. SFDR Measurement Configuration Using a Notch Filter*

Before using the notch filter to measure the harmonics, it is necessary to calibrate out the loss in the filter at the frequency of the harmonics. This can be done by applying a 0 dBm sine wave at the frequency of each harmonic into the 6 dB pad and the notch filter and then recording the loss at the output of the notch filter. This value can then be factored out of the measured harmonic value to determine the actual amplitude for each harmonic. Figure 16 shows the output of the 6 dB pad and 10 MHz notch filter with a 0 dBm 20 MHz signal applied to the input. The overall loss through the pad and the notch filter is 6.01 dBm, so there is little or no loss in the notch filter itself at the frequency of the harmonic.

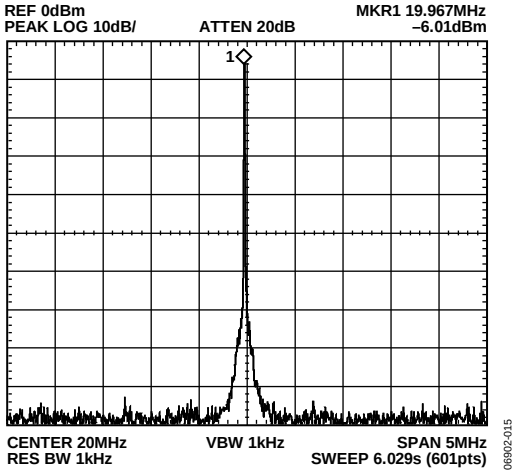



*Figure 16. Calibration of Loss in the 6 dB Pad and Notch Filter*

Figure 17 shows the converter output with the notch filter in place. The actual harmonic value measured is −87.5 dB. Once the 6 dB attenuation is added back in, the actual level of the highest spur is −81.5 dB. Without the notch filter and 20 dB RF attenuation, this spur measures at −71.5 dB, which is a difference of 10 dB, caused by distortion in the analyzer not by the DAC itself.

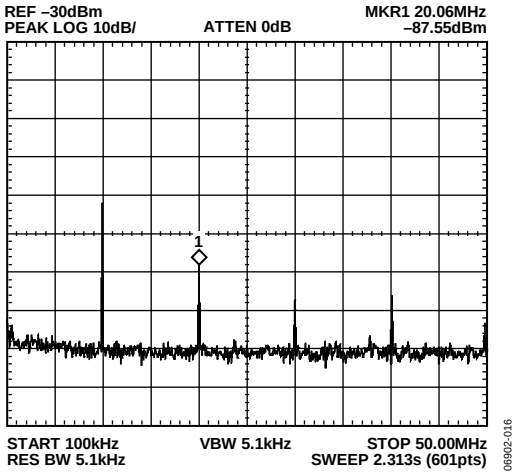



*Figure 17. SFDR Measurement with a Notch Filter*

## OUT-OF-BAND, SPURIOUS-FREE DYNAMIC RANGE

Out-of-band SFDR is the difference, in dBc, between the peak amplitude of the output signal and the peak spurious signal within the band that starts at the Nyquist frequency of the input data rate and ends at the frequency of the DAC output sample rate.

For converters with interpolation filters, this range is between the Nyquist frequency of the input data rate and the Nyquist frequency of the DAC update rate. Typically, energy in this band is rejected by the interpolation filters. This specification, therefore, defines how well the interpolation filters work and the effect of other parasitic coupling paths on the DAC output.

## TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental.

## TWO-TONE INTERMODULATION DISTORTION

### *2F1±F2 and 2F2±F1*

The terms 2F1±F2 and 2F2±F1 represent the third-order intermodulation distortion (IMD) products of the DAC when synthesizing two coherent tones. The third-order IMD performance is the worst-case ratio of the peak value of each term to the peak value of one of the two input tones. The minus terms in the third-order IMD products are very important; depending on the spacing of the two tones, the intermodulation products fall very close to the desired signals. This necessitates a very steep and often expensive band-pass filter if the intermodulation products are too high. The typical spacing for two tones for IMD testing is 1 MHz.

### *3F1±2F2 and 3F2 ±2F1*

The terms 3F1±2F2 and 3F2±2F1 represent the fifth-order IMD products of the DAC. Because these terms are usually smaller in amplitude than the third-order IMD products, and are further away from the desired signals, they do not usually represent such a significant impact on performance. Figure 18 through Figure 21 show a typical DAC two-tone output spectrum and its IMD products. To adequately measure the IMD products, it is necessary to reduce the frequency span and change both the reference level and RF attenuation because they are not visible with the spectrum analyzer settings in the presence of the two tones, as can be seen in Figure 18.

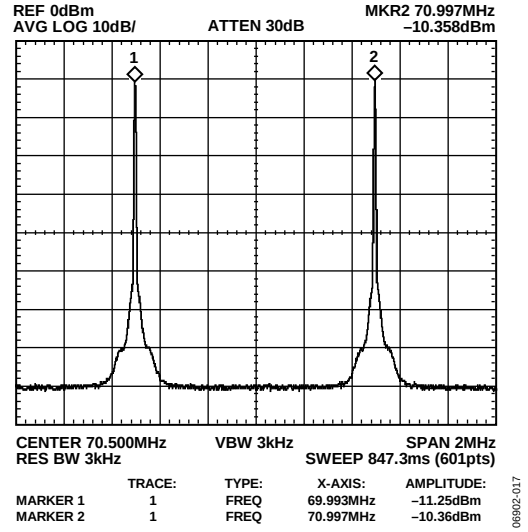



*Figure 18. Typical Two-Tone Output Spectrum ($F_{OUT}$ = 70, 71 MHz)*

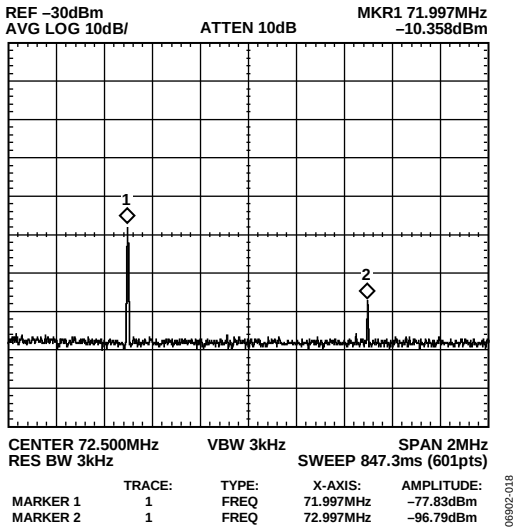



Figure 19. 2F2-F1 and 3F2-2F1

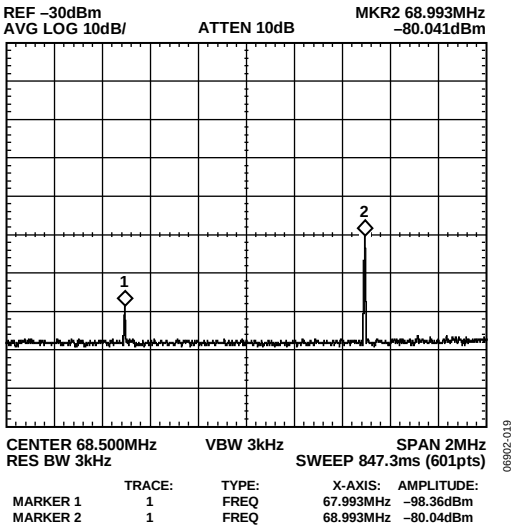



Figure 20. .2F1-F2 and 3F1-2F2

**Table 1. Typical IMD Calculation**

| Fundamental Amplitude | Third Order IMD Amplitudes | Fifth Order IMD Amplitudes | IMD (dBc) |
|---|---|---|---|
| –11.25 | –77.8 | –96.8 | 66.55 (3rd) |
| –10.36 | –80 | –98.4 | 85.55 (5TH) |

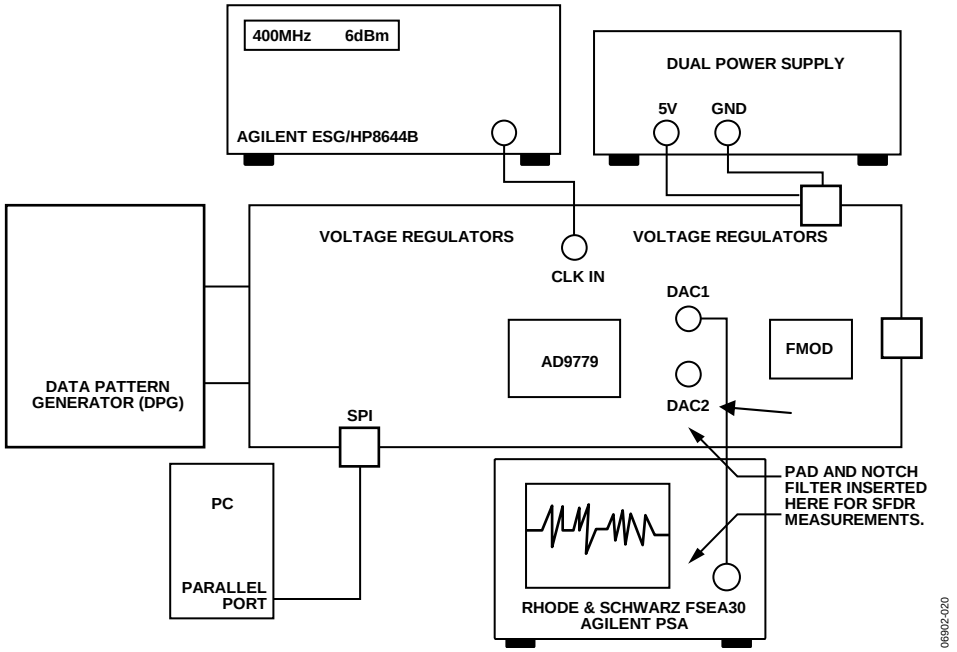



Figure 21. Single-Tone and Two-Tone AC Test Setup

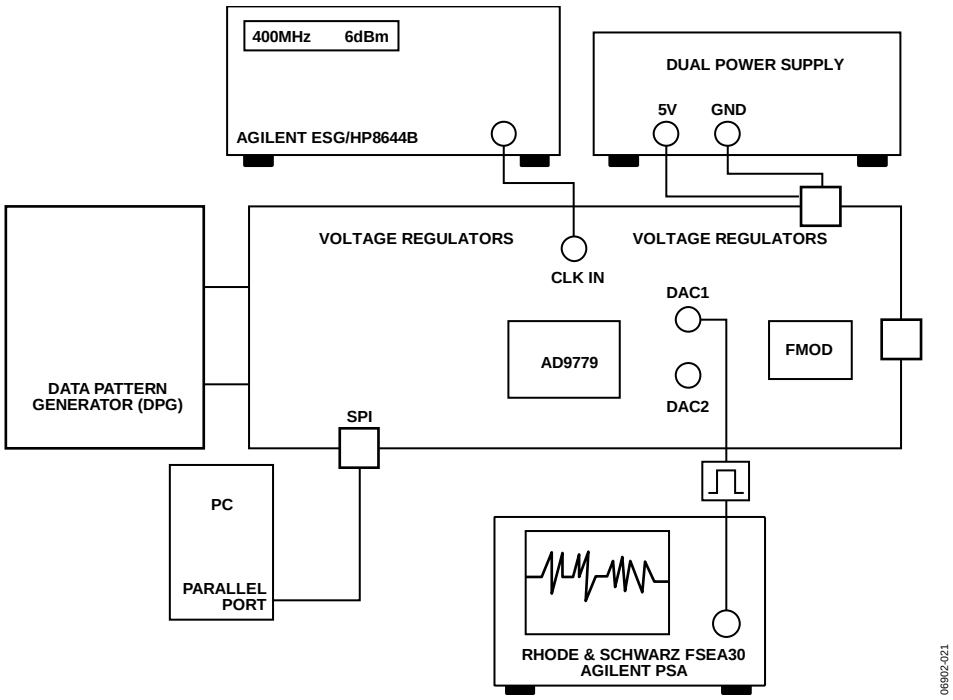



*Figure 22. NSD AC Test Set*

## NOISE SPECTRAL DENSITY

Noise spectral density (NSD) is the converter noise power per unit of bandwidth. This is usually specified in dBm/Hz in the presence of a 0 dBm full-scale signal. If the signal power is less than or greater than 0 dBm, it is necessary to specify the NSD in dBc/Hz and specify the output signal power. To characterize the NSD for a converter, with respect to clock frequency and $F_{OUT}$, the setup shown in Figure 22 is used.

A band-pass filter at a specified frequency is used to isolate a section of the DAC noise floor and knock down the signal level going into the spectrum analyzer. The internal preamp of the spectrum analyzer is used to ensure that the noise floor of the DAC is above the noise floor of the analyzer. If the spectrum analyzer does not have an internal preamp, an external low noise amplifier (LNA) can be used to achieve the same results. An appropriate LNA for these measurements is the Mini-Circuits ZFL-500LN.

As with the SFDR measurements, it is first necessary to calibrate the filter path to be able to factor the loss in the filter out of the measured NSD results. Typically, the NSD performance is measured using a 70 MHz band-pass filter, but it is important to check a few sections of the noise floor with various band-pass filters to ensure that the noise floor is flat over the entire Nyquist band.

Figure  shows the output of a 70 MHz band-pass filter with a 0 dBm, 70 MHz sine wave input. Because the loss through the filter is approximately 1.25 dB, this value needs to be factored out of the measured NSD numbers.

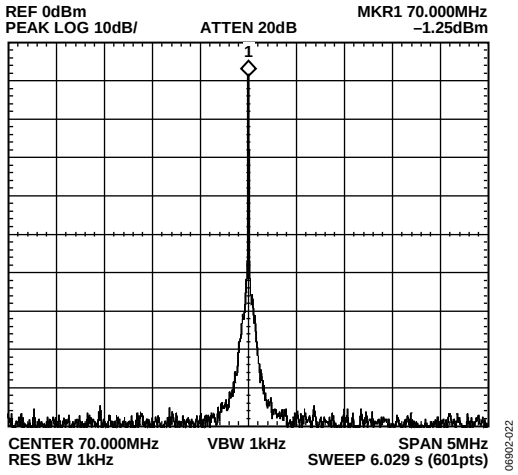



*Figure 23. 70 MHz Band-Pass Filter Output ($F_{OUT}$ = 70 MHz, 0 dBm)*

For a spectrum analyzer, which contains an internal preamp, the band-passed signal can be applied directly to the input of the spectrum analyzer, and the NSD can be directly measured as shown in Figure 23. The NSD number shown has the gain of the internal preamp factored out. To calculate the correct NSD number from this value, the loss in the filter must be factored in as

NSD = −160 + 1.25 = −158.75 dBm/Hz

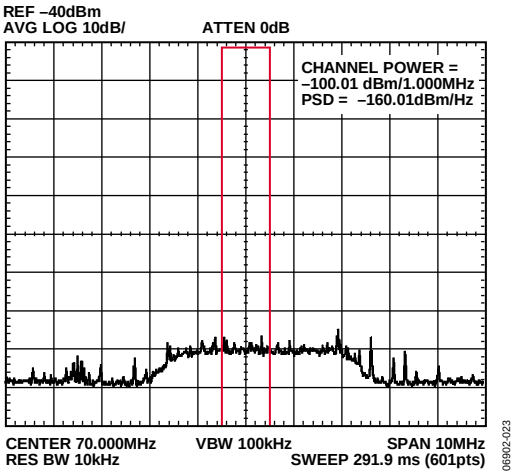



*Figure 23. Measured NSD Using Internal Preamp*

For a spectrum analyzer that does not contain an internal preamp, an external LNA can accomplish the same result as the internal preamp. Before using the LNA in the measurement path, the actual gain of the LNA must be calibrated. To determine the gain of the LNA, a −30 dBm 70 MHz sine wave is applied to the input of the LNA and the output of the LNA is measured with a spectrum analyzer. In this case, the gain of the LNA is approximately 29 dB, as shown in Figure 24.

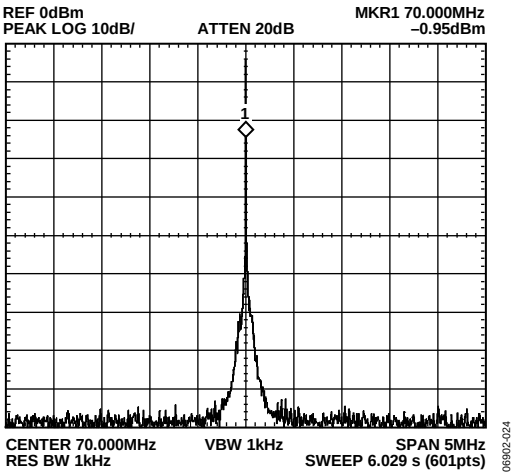



*Figure 24. Output of LNA with −30 dBm 70 MHz Sine Wave Input Signal*

The measured NSD using the band-pass filter followed by the LNA is shown in Figure 25. The actual NSD is calculated as follows:

NSD = (−130.5) − (29) + (1.25) = −158.25 dBm/Hz

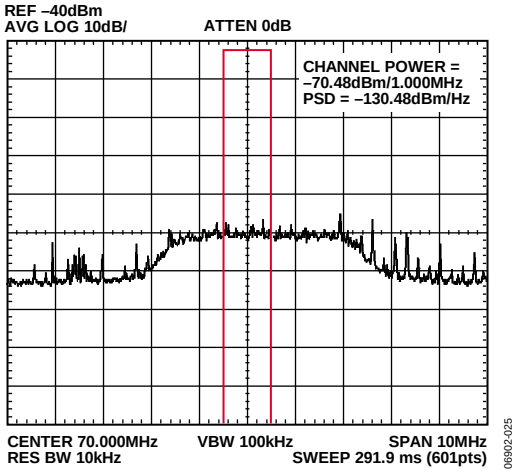



*Figure 25. Measured NSD Using External LNA*

A major factor in the degradation in NSD performance for a DAC is the sine source used to clock the part. Figure 26 shows the NSD for the AD9783 running at 400 MSPS with respect to $F_{OUT}$ using three different sine sources (Rohde & Schwarz SMA100A, Agilent ESG, and Rohde & Schwarz SML02).

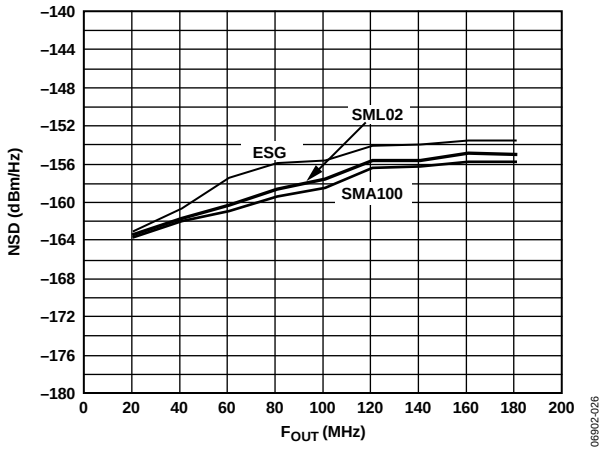
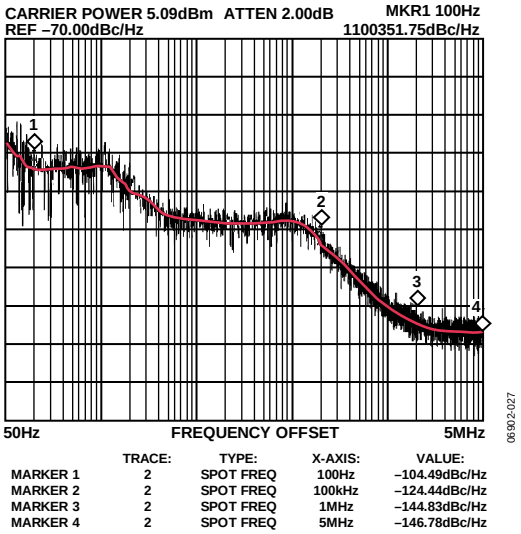


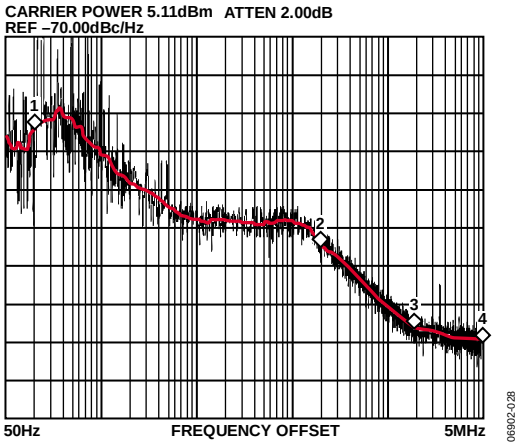

*Figure 26. AD9783 NSD vs $F_{OUT}$ for Various Sine Sources at 400 MSPS*

Referring to the phase noise plots for each sine source (see Figure , Figure 27, and Figure ), note that the main differ-ence is at the 1 MHz and 5 MHz offsets. The close-in phase noise does not appear to vary much and does not have a significant impact on the performance. This means that the noise performance of the sine source itself is the largest limiting factor on the overall achievable noise performance in the DAC.




| | TRACE: | TYPE: | X-AXIS: | VALUE: |
|---|---|---|---|---|
| MARKER 1 | 2 | SPOT FREQ | 100Hz | –104.49dBc/Hz |
| MARKER 2 | 2 | SPOT FREQ | 100kHz | –124.44dBc/Hz |
| MARKER 3 | 2 | SPOT FREQ | 1MHz | –144.83dBc/Hz |
| MARKER 4 | 2 | SPOT FREQ | 5MHz | –146.78dBc/Hz |

*Figure 28 Phase Noise Performance at 400 MSPS for the Agilent E4426B ESG Sine Source*




| | TRACE: | TYPE: | X-AXIS: | VALUE: |
|---|---|---|---|---|
| MARKER 1 | 2 | SPOT FREQ | 100Hz | –98.67dBc/Hz |
| MARKER 2 | 2 | SPOT FREQ | 100kHz | –124.77dBc/Hz |
| MARKER 3 | 2 | SPOT FREQ | 1MHz | –146.25dBc/Hz |
| MARKER 4 | 2 | SPOT FREQ | 5MHz | –149.16dBc/Hz |

*Figure 27. Phase Noise Performance at 400MSPS for the Rohde & Schwarz SML02 Sine Source*

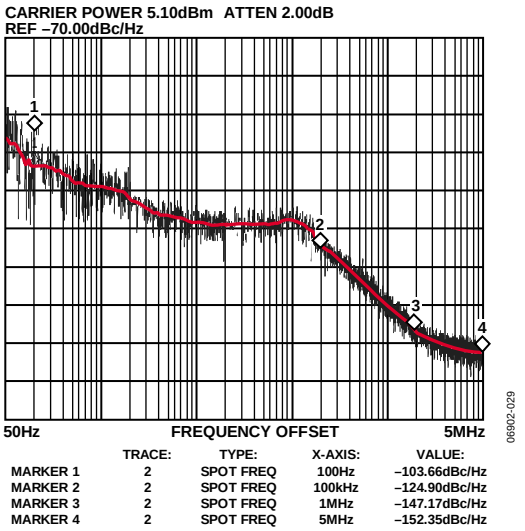



*Figure 30 Phase Noise Performance at 400 MSPS for the Rohde & Schwarz SMA100A Sine Source*

**Table 2. Sine Source Phase Noise Summary at 400 MSPS**

| | Offset | | | |
|---|---|---|---|---|
| **Sine Source** | **100 Hz** | **100 kHz** | **1 MHz** | **5 MHz** |
| Agilent E4426B ESG | −104.5 | −124.4 | −144.8 | −146.8 |
| Rohde & Schwarz SML02 | −98.7 | −124.8 | −146.3 | −149.2 |
| Rohde & Schwarz SMA100A | −103.7 | −124.9 | −147.2 | −152.4 |

Figure 28 shows the NSD measured using the AD9739 and the same three sine sources. Here, the NSD is measured at 2.1 GSPS; the phase noise of each sine source is measured at 2.1 GSPS to determine if there is any degradation or improvement at the higher operating frequency.

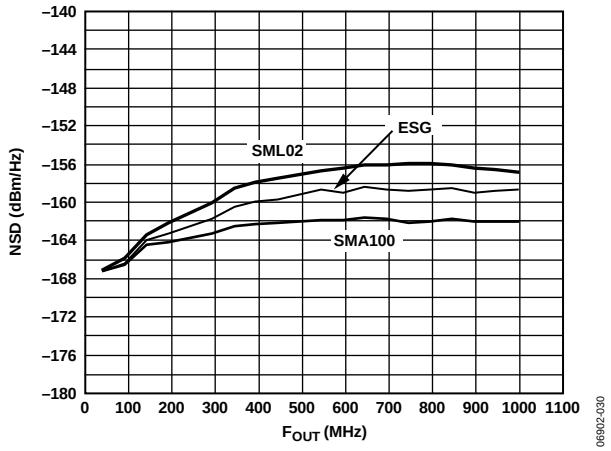



*Figure 28. NSD vs. $F_{OUT}$ for Various Sine Sources at 2.1 GSPS*

The Rohde & Schwarz SML02 at 2.1 GSPS provides the worst noise performance for the AD9739, whereas at 400 MSPS, the Agilent E4426B ESG provides the worst noise performance for the AD9783. As with the AD9783, the phase noise plots support the lower performing NSD performance.

The Rohde & Schwarz SML02 proves inferior to both the Agilent ESG and the Rohde & Schwarz SMA100A at all of the offset frequencies. This is most likely because the maximum frequency for the SML02 is 2.2 GSPS, thus the performance drops off significantly when running close to the maximum specified frequency. The major difference between the ESG and SMA100A occurs at the 5 MHz offset. This is similar to the results at 400 MSPS.

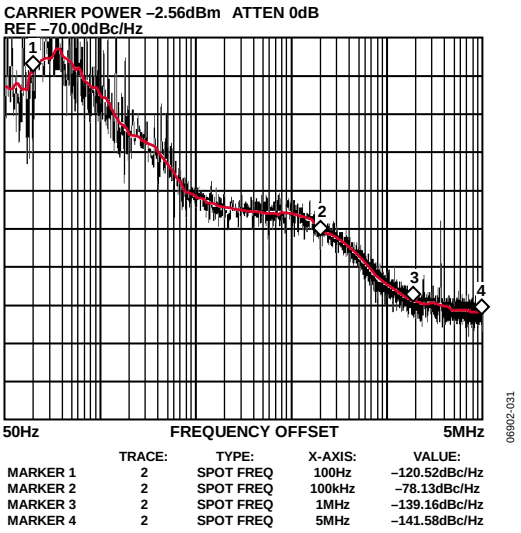



*Figure 29. Phase Noise Performance at 2.1 GSPS for the Rohde & Schwarz SML02 Sine Source*

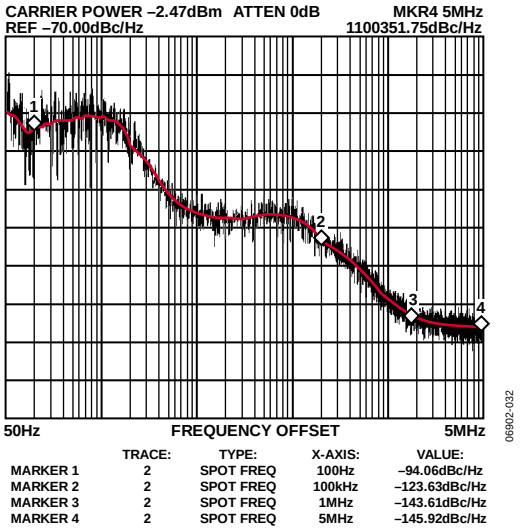



*Figure 33. Phase Noise Performance at 2.1 GSPS for the Agilent E4426B ESG Sine Source*

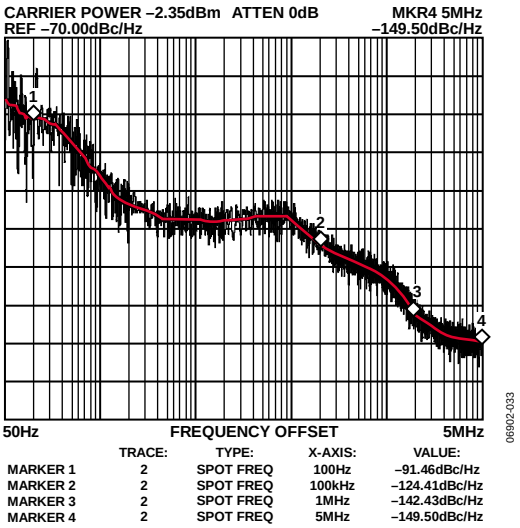



*Figure 30. Phase Noise Performance at 2.1 GSPS for the Rohde & Schwarz SMA100A Sine Source*

**Table 3. Sine Source Phase Noise Summary at 2.1 GSPS**

| | Offset | | | |
|---|---|---|---|---|
| **Sine Source** | **100 Hz** | **100 kHz** | **1 MHz** | **5 MHz** |
| Agilent E4426B | −94.1 | −123.6 | −143.6 | −145.9 |
| Rohde & Schwarz SML 02 | −78.1 | −120.5 | −139.2 | −141.5 |
| Rohde & Schwarz SMA100A | −91.2 | −124.4 | −142.4 | −149.5 |

Because the noise performance of the sine source can vary significantly over the entire operating frequency range, care must be taken when choosing the correct sine source for a given application when NSD is a critical parameter.

## ADJACENT CHANNEL LEAKAGE RATIO OR ADJACENT CHANNEL POWER RATIO

The adjacent channel leakage (power) ratio is a ratio, in dBc, between the measured power within a channel relative to its adjacent channels. Various standards require different channel bandwidths and adjacent channel spacing as defined in Table 4 through Table 7.

**Table 4. ACLR Setting for WCDMA**

| | Offset (MHz) | Channel Bandwidth |
|---|---|---|
| Carrier | 0 | 3.84 MHz |
| 1st Adjacent Channel | 5 | 3.84 MHz |
| 2nd Adjacent Channel | 10 | 3.84 MHz |
| 3rd Adjacent Channel | 15 | 3.84 MHz |
| 4th Adjacent Channel | 20 | 3.84 MHz |

**Table 5. ACLR Settings for CDMA2000 IF > 1 GHz**

| | Offset (MHz) | Channel Bandwidth |
|---|---|---|
| Carrier | 0 | 1.228 MHz |
| 1st Adjacent Channel | 1.6 | 1.228 MHz |
| 2nd Adjacent Channel | 3.2 | 1.228 MHz |

**Table 6. ACLR Settings for CDMA2000 IF < 1GHz**

| | Offset (MHz) | Channel Bandwidth |
|---|---|---|
| Carrier | 0 | 1.228 MHz |
| 1st Adjacent Channel | 0.885 | 30 kHz |
| 2nd Adjacent Channel | 1.25 | 30 kHz |

**Table 7. ACLR Settings for TDSCDMA**

| | Offset (MHz) | Channel Bandwidth |
|---|---|---|
| Carrier | 0 | 1.228 MHz |
| 1st Adjacent Channel | 0.750 | 30 kHz |
| 2nd Adjacent Channel | 1.98 | 30 kHz |

Figure 31 and Figure 32 show typical ACLR performance for WCDMA and CDMA2000. The WCDMA data shows the AD9736 running at 491.52 MSPS. The CDMA2000 data shows the AD9779 running at 122.88 MSPS, 4× interpolation, FDAC/4 modulation.

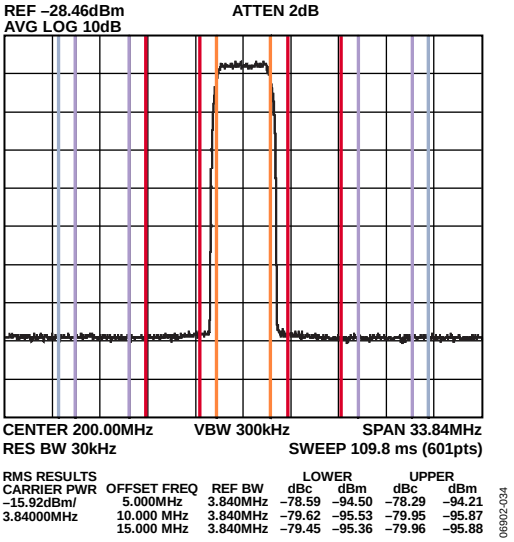



*Figure 31. AD9736 Typical WCDMA Performance*

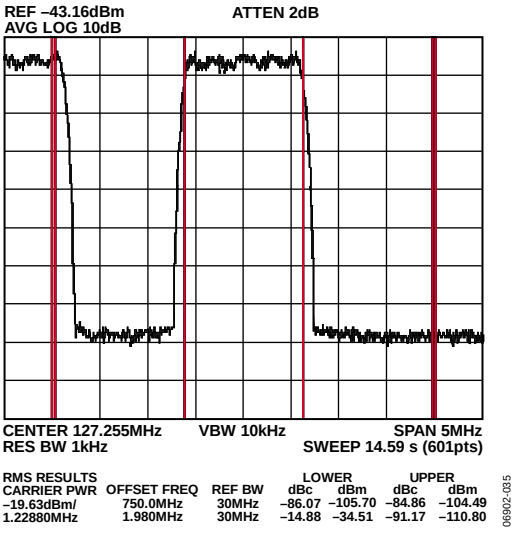



*Figure 32. AD9779 Typical CDMA2000 Performance*

## CROSSTALK

Crosstalk is the measure of any feedthrough from one converter to another on a multichannel DAC. Crosstalk can be measured using one of the following two methods:

- Drive each DAC with a distinct frequency tone and check each channel for the appearance of the other tone.
- Drive one DAC with a distinct tone and the other DACs with 0 and look for the appearance of the tone on the spectrum of idle DACs.

Figure 33 and Figure 34 show the crosstalk measurement using the second method. Not only does the fundamental signal feed through but the harmonics and images do also. Because crosstalk results can also be affected by coupling mechanisms on the evaluation board, care must be taken to ensure that what is measured is due to the converter itself and not to the evaluation board.

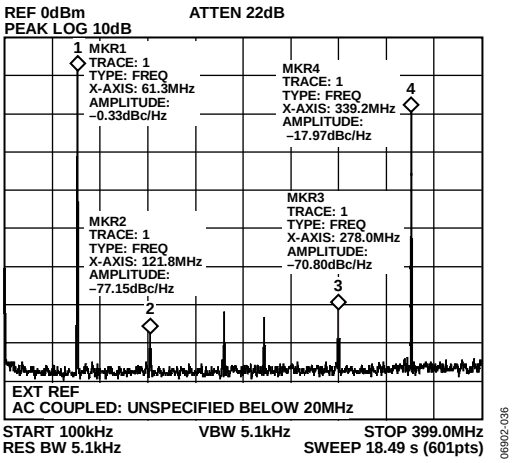



*Figure 33. Output of DAC1 for a 60MHz Sine Wave Input*

Note that, in Figure 33 and Figure 34, the markers are on the following spurs:

1. Fundamental tone: 60 MHz
2. Second harmonic: 120 MHz
3. FDAC minus the second harmonic: 280 MHz
4. First image of DAC (FDAC – $F_{OUT}$): 340 MHz

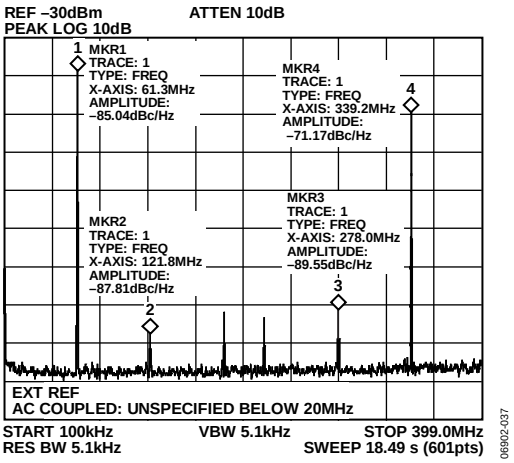



*Figure 34. Feedthrough of DAC1 onto DAC2 with 0 Applied to DAC2*

## SINX/X ROLL-OFF

All DAC converters have an inherent sinx/x roll-off that affects the amplitude of the signal being synthesized as it gets closer to the Nyquist frequency. It is important to characterize this roll-off to determine how the decrease in signal amplitude affects the AC performance. To measure this effect, simply generate various full-scale sine waves out of the DAC and measure the fundamental amplitude as the output frequency increases. Figure 35 shows this measurement for the AD9783 running at 600 MSPS. This part also has an analog mix mode that can generate tones in the second and third Nyquist zones; thus, the amplitude response in mix mode is also shown.

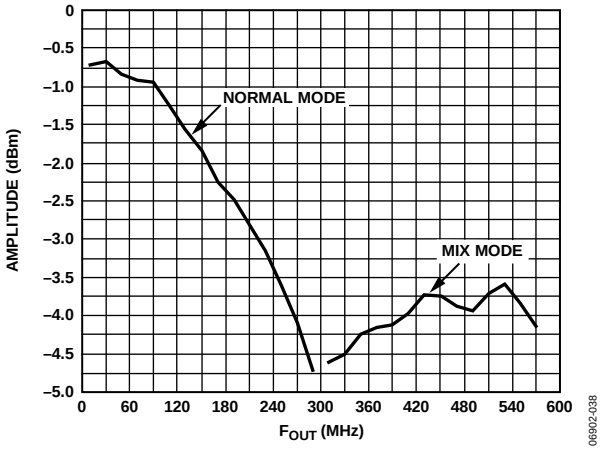



*Figure 35. AD9783 Amplitude Response in Normal and Mix Modes*

# DC TEST DEFINITIONS

The DC test definitions in this section assume binary data inputs.

## FULL-SCALE GAIN

The full scale of a converter is the measured output current with all the input bits set to 1. For $I_{OUTA}$ (or, for some converter pinouts, $I_{OUTP}$), full scale is expected when all inputs are set to 1. For $I_{OUTB}$ (or, for some converter pinouts, $I_{OUTN}$), full scale is expected when all the inputs are set to 0.

## GAIN ERROR

Gain error is the difference between the actual and ideal output span. The actual output span is determined by the output when all inputs are set to 1, minus the output when all inputs are set to 0. Figure 37 shows the effect on the DAC transfer function when a gain error is present.

## OFFSET

The offset of a converter is the measured output current with all the input bits set to 0. For $I_{OUTA}$ (or, for some converter pinouts, $I_{OUTP}$), 0 mA is expected when all inputs are set to 0. For $I_{OUTB}$ (or, for some converter pinouts, $I_{OUTN}$), 0 mA is expected when all the inputs are set to 1.

## OFFSET ERROR

Offset error is the deviation of the output current from the ideal zero. Figure 37 shows the effect on the DAC transfer function when an offset error is present.

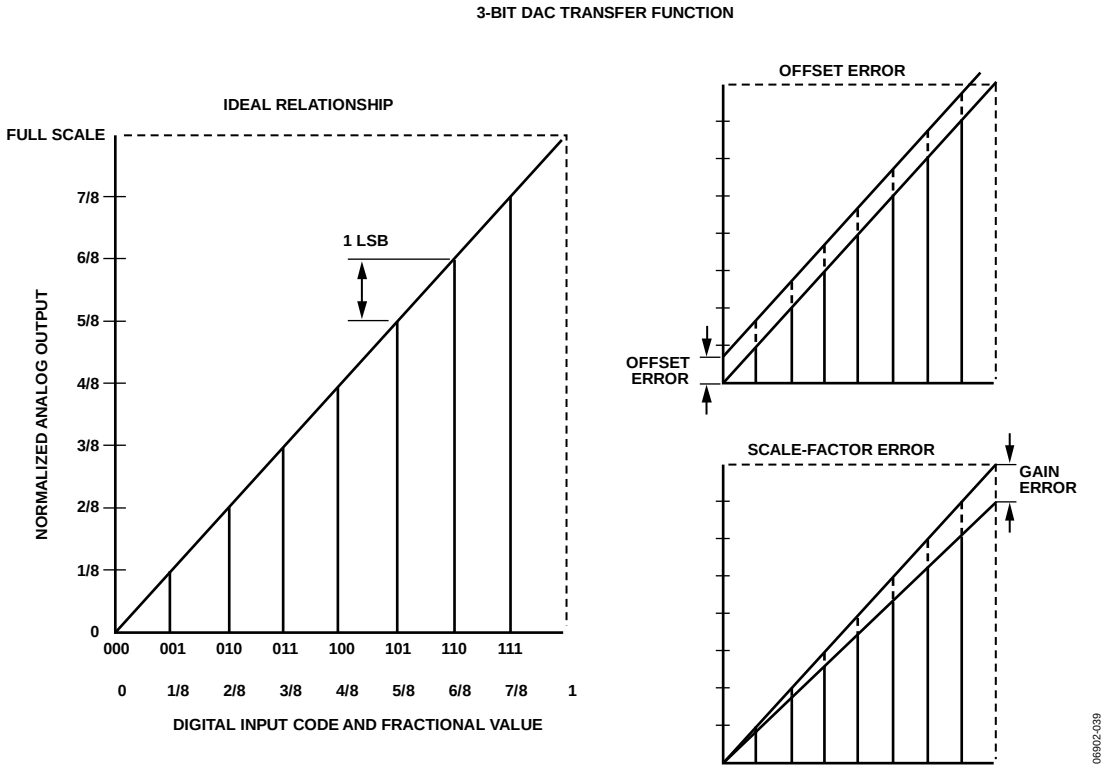



*Figure 36. Effect of Offset and Gain Errors on the Ideal Transfer Function*

## TEMPERATURE DRIFT

Temperature drift is the maximum change over the entire operating temperature range $T_{MIN}$ to $T_{MAX}$. For offset and gain drift, the drift is reported in ppm of full-scale range per °C. For reference drift, the drift is reported in ppm per °C. The drift in ppm per °C is usually calculated from the maximum measured value. A typical reference drift plot is shown in Figure 37.

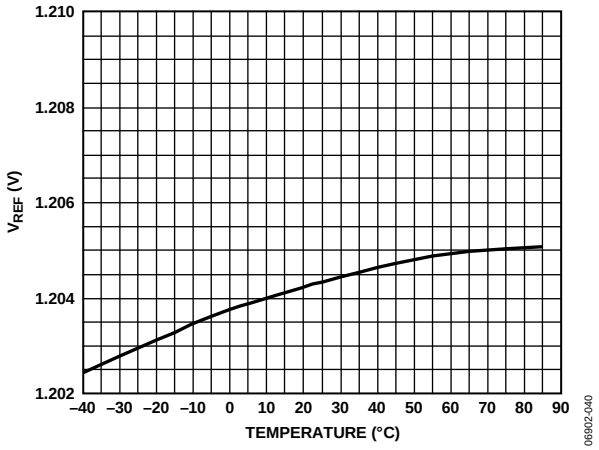



*Figure 37. Typical Reference Drift Plot*

In this case, the maximum measured value occurs at 85°C, so the drift is calculated from this value. The data for this curve is shown in Table 8.

**Table 8. Reference Drift Data**

| Temperature | VREF | PPM from Maximum |
|---|---|---|
| 85 | 1.20508 | 0 |
| 65 | 1.204974 | −88.035 |
| 45 | 1.204714 | −303.092 |
| 25 | 1.204352 | −604.217 |
| 0 | 1.203768 | −1088.733 |
| −20 | 1.203126 | −1621.428 |
| −40 | 1.202425 | −2203.190 |
| Maximum | 1.20508 | |
| PPM/°C | 17.62552 | |

PPM from max is calculated by

$$ppm\_from\_max = \frac{(VREF - VREFMAX)}{VREFMAX} \times 1e^{6}$$

Finally, PPM/°C is calculated by

$$PPM/°C = \frac{(PPMMAX - PPMMIN)}{125°C}$$

## POWER SUPPLY REJECTION RATIO

Power supply rejection ratio (PSRR) is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

## GAIN MATCHING

Gain matching is the ratio of the gain of one DAC to the gain of the other DAC. This measurement is only valid for parts with multiple DACs and is calculated by

$$GainMatch = \left| \frac{GAIN\_DAC1 - GAIN\_DAC2}{GAIN\_DAC1} \right| \times 100$$

## LINEARITY

There are two types of linearity: differential nonlinearity (DNL) and integral nonlinearity (INL). In order to calculate either the INL or DNL of a converter, it is necessary to first reconstruct the entire transfer function of the converter by measuring the output current for each digital input code. Measuring all of the codes for a converter, especially 14-bit or 16-bit converters, can be a long, painstaking process that is not entirely necessary if the converter has segmentation.

Take, for example, the AD9779, which is a 16-bit 1GSPS DAC. The AD9779 consists of a PMOS current source array divided into 63 equal current sources that make up the six most significant bits (MSBs). The remaining 10 bits are a binary weighted fraction of the MSB current sources (LSBs).

The entire transfer function can be reconstructed by taking only 73 measurements, rather than 65,535 measurements, which is a significant savings in test time. Some other converters, such as the AD9786, a 16-bit 500 MSPS DAC, are segmented into MSBs, ISBs, and LSBs. The AD9786 has 127 equal current sources that make up the seven most significant bits. The next four bits (ISBs) consist of 15 equal current sources whose value is 1/16 of an MSB current source. The remaining five bits (LSBs) are a binary weighted fraction of the ISBs. In this case, the ramp can be reconstructed by taking only 147 measurements, rather than 65,535 measurements.

## INTEGRAL NONLINEARITY ERROR

INL error is the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale. An illustration of how an INL error manifests itself using the ideal transfer curve and measured data is shown in Figure 38 for a 3-bit DAC.

## DIFFERENTIAL NONLINEARITY ERROR

DNL error is the measure of the variation in analog value, normalized to full scale, associated with one LSB change. An illustration of how a DNL error manifests using the ideal transfer curve and measured data is shown in Figure 39 for a 3-bit DAC.

## MONOTONICITY

A DAC is considered monotonic if the output either increases or remains constant as the digital input increases. If the analog output decreases at any point during the digital input sequence, the converter is nonmonotonic.

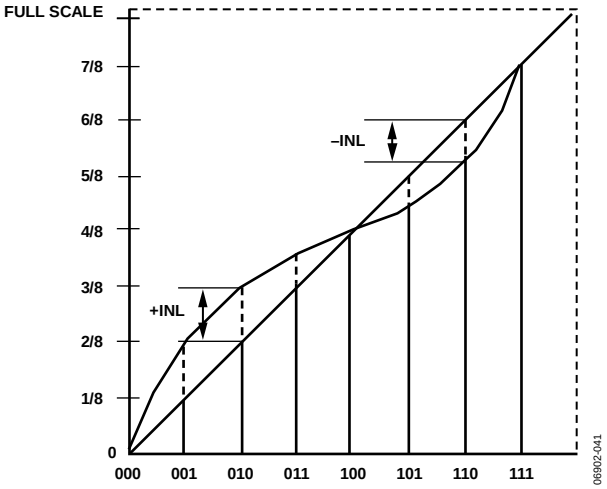



Figure 38. INL Measurements

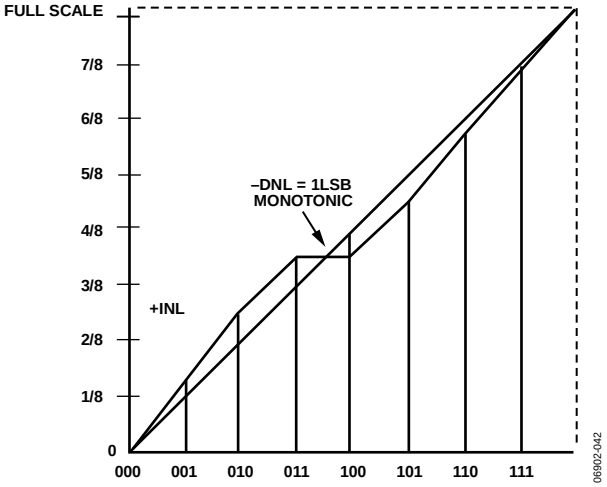



Figure 39. DNL Measurements

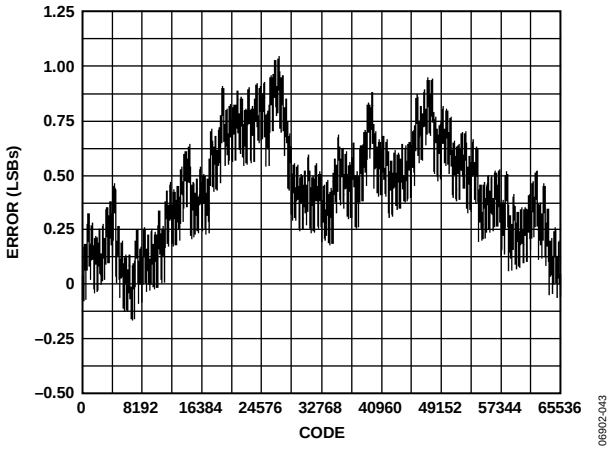



Figure 40. Typical INL Plots for the AD9786

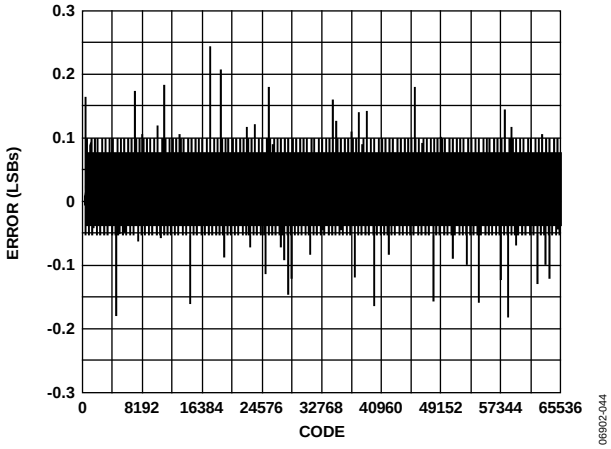



Figure 41. Typical DNL Plots for the AD9786

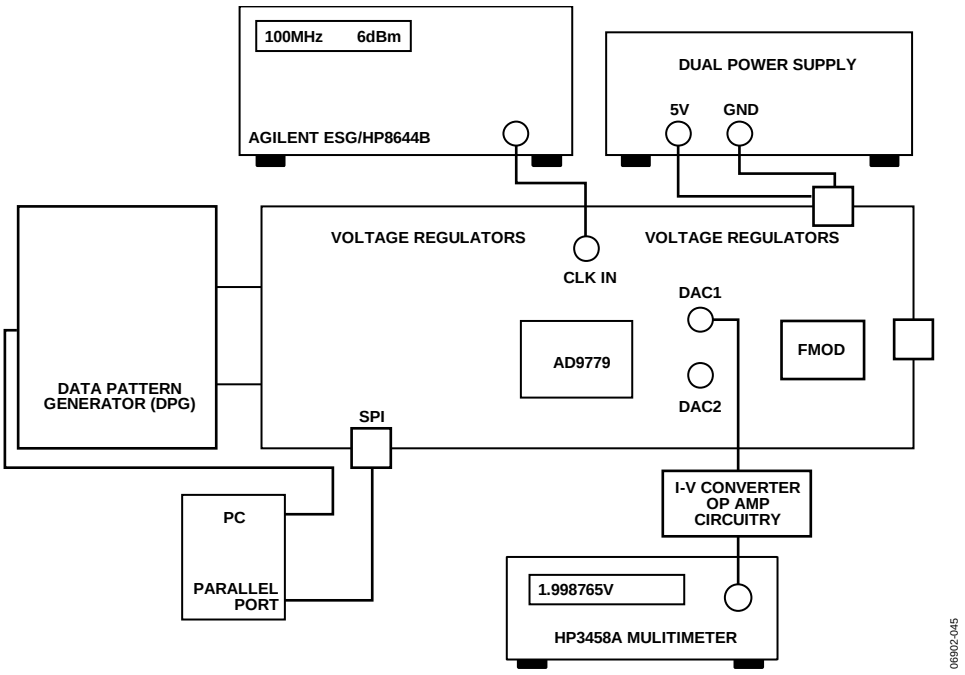



*Figure 42. DC Measurement Test Setup*

# DIGITAL INPUT TIMING

## SETUP TIME

The setup time for a DAC is the amount of time before the clock latching edge at which the data needs to be stable. This time is usually defined as a minimum specification. The setup time can be either positive or negative depending on where the keep-out window occurs with respect to the latching edge of the clock, as shown in Figure 43 through Figure 45.

## HOLD TIME

The hold time for a DAC is the amount of time the data must be stable after the latching edge for the data to be acquired accurately. This time is also usually defined as a minimum time. As is the case with the setup time, the hold time can be positive or negative, as shown in Figure 43 through Figure 45.

## KEEP-OUT WINDOW

The keep-out window for a DAC is the total window around the latching clock edge, which includes both setup and hold times.

For a more detailed description of the setup and hold measurements for high speed CMOS input DACs, refer to Application Note AN-748.

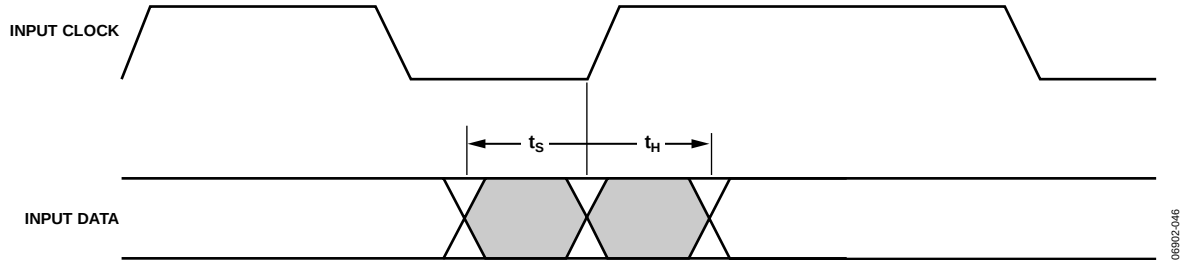



*Figure 43. Setup and Hold Times Symmetric to the Latching Clock Edge ($t_S$ and $t_H$ Are Both Positive)*

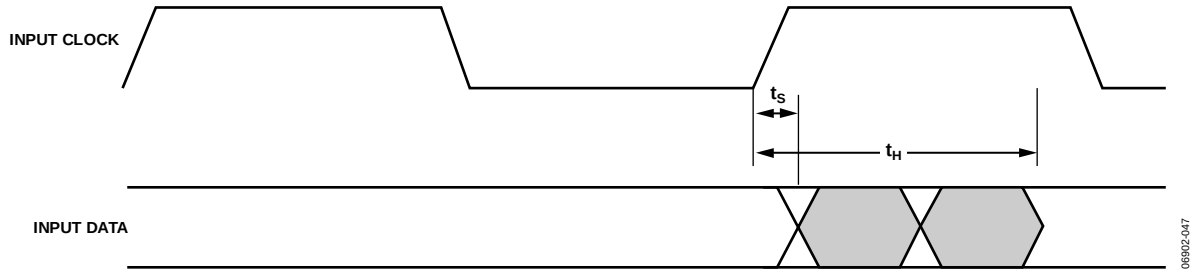



*Figure 44. Setup and Hold Times Are Delayed from the Latching Clock Edge ($t_S$ Is Negative and $t_H$ Is Positive)*

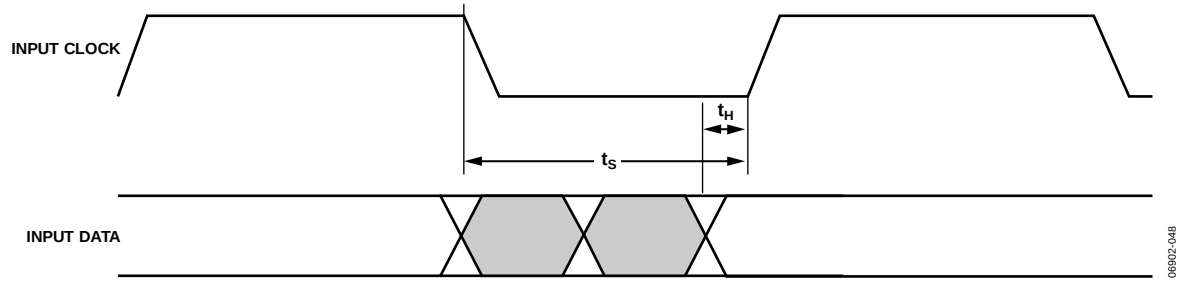



*Figure 45. Setup and Hold Times Are Advanced in Time from the Latching Clock Edge ($t_S$ Is Positive and $t_H$ Is Negative)*

## NOTES

## NOTES

## NOTES


AN06902-0-11/10(A)