

AN-808 APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106 • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Multicarrier CDMA2000 Feasibility

by Brad Brannon and Bill Schofield

ABSTRACT

The goal of this application note is to determine the feasibility of implementing a multicarrier CDMA2000 transceiver and what the major subsystem performances must be.

GENERALIZED BLOCK DIAGRAM

The block diagram in Figure 1 is the general block diagram used in this discussion. While there are many variations of this design, the key focus is on this architecture, which represents a flexible radio platform that can easily implement a wide variety of air standards including WCDMA, CDMA2000, and TD-SCDMA.

Some variations of this architecture include high or low IF sampling as well as direct conversion for receive. Although the latter is not feasible for multicarriers today, it is acknowledged as the low cost, high performance solution of the near future. In the transmit path, direct RF modulation is feasible for most applications if some amount of in-phase and quadrature (IQ) balance is provided. Direct RF modulation represents the lowest cost transmit path. For applications requiring high performance without an IQ balance network, superheterodyne IF upconversion is another excellent option.



Figure 1. ADI Wideband Multicarrier TRX Common Platform CDMA2000/WCDMA/TD-SCDMA

In addition to variations in the electrical schematic discussed, there are many assembly options that have a wide range of implications. These options include system-level partitioning in the form of split Rx and Tx boards as well as split radio and baseband processing and chip partitioning. For example, MxFE functions that incorporate both Rx and Tx functions in a single package are available. This option can facilitate higher integration and lower cost and offers an excellent alternative for low capacity system options. Other possibilities include combining the ADC and RSP to provide higher integration, and lower cost while avoiding import/export restrictions. These and other options are good sources of discussion.

CDMA2000

Specifications for this report are taken from the requirements from 3GPP2, EIA, and TIA specifications. Key specifications from this standard are the reference sensitivities, band of deployment, and blocking requirements. It is assumed that Band Class 0 is the reference point and that performance in other band classes is achieved by adjusting the level plan of the BTS.

RECEIVE DISCUSSION

Receiver operating conditions: From the standard, the required minimum sensitivity in bands 0, 2, 3, 5, 7, 10, 11, and 12 is –117 dBm/1.23 MHz. Bands 1, 4, and 6 require a sensitivity of –119 dBm/1.23 MHz. On a per Hertz basis, this is a signal density of –178 dBm/Hz for the first set of bands and –180 dBm/Hz for the second set of bands.

A second set of conditions relates to single-tone desensitization. This condition limits the amount of conversion gain possible for multicarrier applications and is therefore important in determining this. Although Band Class 0 lists a blocker at +50 dBc (±750 kHz offset), the +87 dBc (±900 kHz offset) is the limiting factor. Band Classes 1, 4, 6, 7, 8, and 10 have a maximum desensitization level of +80 dBc allowing for a higher gain.

The final consideration is that of intermodulation performance. For intermodulation performance, two or more narrow-band tones are placed adjacent to the desired channel. The intermodulation product of an offending signal is designed to fall within about 100 kHz of the center of the channel, potentially disrupting the receiver. The worst condition is Band Class 0 where the intermodulating signals must be +72 dBc (spacing and number of tones depends on the band of deployment and the number of CDMA carriers). If the reference sensitivity is –117 dBm, a power of –45 dBm per intermodulating term results.

Other blocking conditions exist, but it is assumed that the combination of band selection filters and antialias filtering adequately remove those signals from the signal path and not be allowed to enter into the dynamic range considerations for the ADC. This is true for either IF sampling or direction conversion.

Assumptions: Given this information, the front-end design information can now be determined. If the receiver is targeted as being a multicarrier receiver, the largest signal at the antenna is about -30 dBm with a converter full scale at 4 dBm rms (2 V p-p into 200 Ω); a fixed conversion gain of up to 34 dB can be used with no headroom support. A gain of around 30 dB causes the ADC to be driven with a maximum rms signal of about 0 dBm, leaving 4 dB at the top that can serve as margin for power from other nearby strong signals as well as component margin. Given current receiver trends in LNAs, passive mixers, and filter elements, typical downconverter blocks are possible with noise figures below 3 dB (not including the ADC). These numbers will be used in the following calculations. Many applications can require additional dynamic range. Additionally, if losses from cabling and other hardware are considered along with variations in component tolerance, a variable gain configuration should be considered.

Assuming a serial line clock rate that is a multiple of 614.4 MHz, selecting a clock with an integer ratio of this value simplifies clock tree design. For the ADC, the logical clock rates are 61.44 MSPS and 122.88 MSPS. Other possibilities exist each with its own benefits. The next generation converters are capable of higher sample rates and therefore, can be taken advantage of when possible. However, there are trade-offs to be made. A higher sample rate helps to spread the converter noise of a wider band and results in a relatively relaxed converter specification. This tends to be a good thing because converters designed to run at the higher rate have wider bandwidths allowing more noise to be digitized resulting in a lower signal-to-noise ratio (SNR) anyway. In the end, the theoretical difference between 61.44 MSPS and 122.88 MSPS is 3 dB. In comparing two converters at these sample rates, the converter running at the lower speed must be 3 dB greater than the higher speed device to give the same level of performance (all else being equal). If the performance is better than 3 dB, then the lower sample rate device is better. If not, there are advantages of using the higher sample rates. Of course other rates such as 92.16 MSPS can also be used, but require a slightly different clocking circuit. Table 1 outlines the performance relaxation that can be achieved with higher rate converters. If the selected converter performs better than the allowed degradation then performance using that converter is at an advantage. Using any of the clock values shown in Table 1 allows common operation between WCDMA and CDMA2000.

Table. 1

Sample Rate	61.44 MSPS	92.16 MSPS	122.88 MSPS		
Maximum Relaxation	0 dB	1.77 dB	3 dB		

ADC SNR requirements: Given the conversion gain and noise figure (NF) mentioned previously, the ADC SNR can now be calculated. At the antenna, the noise spectral density (NSD) is assumed to be –174 dBm/Hz and the noise spectral density (NSD) at the ADC input is –141 dBm/Hz (–174 + 30 + 3). This assumes that noise outside the Nyquist band of the ADC is filtered with antialiasing filters to prevent front-end thermal noise from aliasing when sampled by the ADC. Ideally, the ADC noise floor should be at least 10 dB below this or –151 dBm/Hz. At a sample rate of 92.16 MHz, this is an SNR of 79.4 dB. Currently only one ADC is capable of this level of performance—the AD9446. If using any other converter, some compromises are necessary. Some of the more reasonable options include:

- 1. Increasing the fixed conversion gain that is limited by the clipping point of the ADC (see Table 2).
- 2. Adding an automatic gain control function that responds after the -45 dBm two-tone levels have been surpassed. This ensures maximum gain below this point and maintains reference sensitivity up to the specified blocking level of either +80 dBc or +87 dBc.
- 3. Reducing the margin between ADC noise floor and thermal noise floor allowing the ADC to contribute to the overall NF of the receiver. See "DNL and Some of its Effects on Converter Performance" found in *Wireless Design & Development* Online June 2001 online issue to determine how this can adversely impact receiver performance.
- 4. Increasing the NF of the analog front end to force the noise of the front end to approach 10 dB above the noise from the ADC.

Options 3 and 4 have similar effects on overall receiver characteristics and sensitivity is the same. However, because the ADC noise is not white, various anomalies result if the ADC is allowed to contribute to the noise floor. Therefore, Option 4 provides overall better performance vs. Option 3. Option 1 does not allow for component variations that normally occur in production runs, and therefore, overall receiver margin can be lost and insufficient performance can result. Therefore, Option 2 is a better overall choice.

Including margin for component tolerance, Option 2 allows the greatest flexibility and overall performance. Gain control includes restrictions and limitations that can be difficult to manage. For example, the gain must be slow enough so as not to unnecessarily track envelopes of commonly occurring signals such as the beat between tones. However, it must be fast enough to track into and out of deep fades. To limit additional intermodulation problems, gain should be maximized until after the two-tone levels have been reached. Beyond this point, gain can be gradually reduced to prevent clipping of the ADC. For the Band Class 0, the two-tone requirements are -45 dBm. Signal powers above -42 dBm (accounting for signal peaking of two -45 dBm tones) can be reduced by limiting conversion gain. If full scale is 4 dBm, the conversion gain can be as high as 46 dB. However, a nominal gain of 42 leaves a few decibels at the top for improved intermodulation performance and accounts for variation in component tolerance. Minimum gain is set by maximum in-band blockers, assuming that outof-band signals are adequately removed. Therefore, as discussed in the previous section, the presence of the 87 dBc blocker, the gain should be reduced to 30, again leaving a few decibel margin at the top for device tolerances.

Using a 12 dB range facilitates gain control in the digital domain where a bit shift left or right shifts gain by 6 dB, making digital compensation for the gain a simple task.

With this configuration, absolute gain can be adjusted in a control or calibration loop to account for part-topart variation so while the absolute gain can change from system to system, the range still stays at 12 dB. If gain trim is desired to compensate for system variations, an overall range greater than 42 dB to 30 dB is





required, but the gain shift should remain 12 dB. In the high gain configuration of 42 dB, the NF must be about 3 dB and the NF can increase to 6 dB as the gain is reduced.

For a nominal gain of 42 dB and a peak power into the ADC from two signals at -45 dBm (each) would be 0 dBm, leaving about 5 dB of margin before the full scale of the ADC. At a gain of 42 dB and an analog front-end NF of 3 dB, the noise level presented to the ADC input is -129 dBm/Hz. At 92.16 MSPS, a typical 14-bit ADC can deliver between 72 dBFS and 75 dBFS of SNR depending on the part and input frequency. Under these conditions, the noise density of the ADC is between -144 dBm/Hz and -147 dBm/Hz. Worst case, the front-end thermal noise is 15 dB above the ADC noise and therefore, the total contribution by the ADC to the NF is 0.1 dB, increasing it to 3.1 dB. When the gain is minimum (30 dB) and the NF maximum, the total NF is 7 dB, including the AFE and the ADC. In this condition, the margin between the front-end noise and the ADC noise is reduced but is tempered because the NF increases as the gain reduces, which therefore somewhat lessens the effects of reduced gain on noise.

With the high conversion gain and a low overall NF (about 3.1 dB), sensitivity is greater than the required specification and is limited primarily by the NF. Static sensitivity for a voice channel is on the order of 8 dB greater than the required –117 dBm for the 800 MHz band (see Table 2).

For the case of a single-tone blocker at 87 dBc (-30 dBm in the 800 MHz band), the gain needs to be reduced as previously indicated. Nominally, the gain setting should change at -42 dBm. This is after the intermodulation test levels to prevent additional intermodulation issues and it must be completed before the single tone desensitization test is performed. Analog techniques or the digital AGC features of an RSP such as the AD6636 can be utilized for this. Assuming an initial gain of 42 dB, the gain can be reduced by 12 dB (two 6 dB steps) resulting in an overall gain of 30 dB in the low setting. The key factor of the conversion gain is to boost the thermal noise above the noise of the ADC in the high-gain case. Once this is done, any excess gain can be useful for implementing any required margins.

At the reduced gain of 30 dB, the NF increases. Assuming that the gain control is in the IF and not RF attenuation, a modest increase in NF is anticipated. If it is assumed that NF increases to 7 dB (including the ADC), then the following is offered for IF sampling: The noise from the ADC is about -146 dBm/Hz (4 dBm ADC full scale, 73 dB SNR and a sample rate of 92.16 MHz) and the noise of the front-end referenced to the ADC is -138 dBm/Hz (-174 dBm/Hz + 30 dB (gain) + 6 dB (NF)) at the ADC input. This results in an overall noise density of -137.4 dBm/Hz through the ADC. The total noise in a CDMA2000 channel is found by simple integration. Over 1.25 MHz, the total noise is -76.4 dBm through the ADC. The blocker is a few decibels below the full scale of the converter for margin sake. Finally, the desired CDMA2000 signal that began at -117 on the antenna terminal is at -87 dBm through the ADC. This is an SNR of -10.6 dB. After despreading, an effective SNR of about 10.4 dB results. Because only 5 dB is required, there is sufficient SNR to provide a reasonable BER.

Working the other way, a reference sensitivity of -117 dBm is required with an Eb/N0 of 5 dB. With an ideal despreading gain of 21 dB, the in-band noise can be 16 dB greater than the desired in-band signal. Thus, referenced to the antenna, total thermal noise can be -101 dBm or -162 dB/Hz. To determine how much of the noise comes from the electronics, available noise from the antenna must be subtracted. The results are that the worst NF can be as high as 12 dB, which easily meets with contemporary designs and devices.

For single tone desensitization, a user power of -117 dBm is assumed. Without a blocker present, the received SNR is 13.5 dB. In the presence of blocker, the gain is reduced to 30 dB and the SNR falls to 10 dB. From these numbers, it does not appear that a 3 dB increase in user power is required for this configuration. Therefore, the excess SNR indicates that additional margin can be allocated to other places in the circuit.

Although direct downconversion is not quite ready for multicarrier market space, it is the preferred architecture for cost and simplicity reasons. It is likely that this approach will be available within the scope of a new multicarrier development and is therefore, already considered here. The current limitations are the quadrature demodulator and data converters. For multicarrier applications, the critical aspects are IQ balancing and second-order intermodulation through the demodulators and data converters. Beyond this, the data converters must still meet the same general performance levels as the IF sampling variations with the advantage of a low frequency input range.

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Gain	AFE NF	Total NF	0 dB SNR	Effective SNR @ -117 dBm	Nominal Gain Trip Point	ADC Clip Point					
40 dB	3 dB	3.1 dB	130.5 dB	13.9 dB	-42	–38 dBm					
36 dB	4.5 dB	4.9 dB	129.1 dB	12.1 dB	-36	–32 dBm					
30 dB	6 dB	7 dB	127.0 dB	10 dB	-30	–26 dBm					



Figure 3.

There are several issues for multi-carrier applications. The primary issue is quadrature balance and even order intermodulation. Images caused by quadrature imbalance cause blocking on the opposite side of the dc. Therefore, strong signals in the positive frequency domain cause blocking in the negative frequency domain by image mismatches. Significant improvements in the IQ balance in analog components is not likely to happen; however, users can compensate for this elsewhere in the signal path in either the analog or digital domain. With a symmetrical frequency plan, demodulator performance must be the same as with an IF sampling architecture. For example, if a narrow-band blocker is present, the image caused by the imbalance should not block a signal on the other side of the dc as much as a harmonic would in an IF sampling system. This requirement is discussed in the following section.

In addition to imbalance, even-order intermodulation (especially second-order) can cause blocking problems. For even-order distortion, the amplitude modulation (AM) content of all signals in-band appears at dc. Although LO leakage is more related to IQ imbalance, it too shows up at dc. Here too, spurious requirements are discussed in the next section.

Many of the quadrature balance issues in the digital domain are more fully discussed in a later section. To facilitate this, means of addressing IQ gain mismatch, dc offset, IQ phase correction, and complex baseband tuning are required. In order to combat some of these issues, the AD6636 includes various features used to compensate for them. The AD6636 is equally suitable for IQ signal processing of multicarrier signals as it is for multicarrier IF sampling. It includes IQ gain adjustment, automatic dc offset correction, IQ phase correction, and the ability to perform complex baseband tuning.

For direct conversion, several other considerations must be made. First, a lower sample rate is likely, but not required. Because two converters are required, a lower sample rate is likely to be used to keep digital processing and power as low as possible. A sample rate of 61.44 MSPS likely provides a full 61.44 MHz of complex bandwidth. If the ADCs keep the same input range, a 3 dB increase in gain is allowable because the demodulator also divides the power between the two ADCs and the losses associated with a typical frequency translation stage. Without this additional gain, 3 dB (approximately) of ADC range is lost. In the digital processing, these signals are again summed and produce an overall 3 dB higher signal along with a 3 dB higher ADC noise floor from the noncorrelated ADC noise floor of both ADCs. At the same time, the effective ADC input range is also 3 dB higher, as is the noise floor of the effective ADC contributions. A first-order wash in sensitivity results as signal levels and noise increase by the same amount. If the signal path includes the extra 3 dB gain, then the IP3 requirements increase a proportionate amount relative to the full scale of the system. First, each single ADC must also meet the same requirements as IF sampling. Although the sample rate is lower than may have otherwise been used for IF sampling, the noise bandwidth is equal to the full sample rate. The resulting noise performance is similar to that of an IF sampling solution operating at 122.88 MSPS with two added advantages. First, because the analog signals are at baseband, clock jitter is no longer a problem. Second, because the analog signals are at baseband, they are not subjected to input slew rate limitations of the converter, which is one of the biggest causes of poor harmonic distortion in IF sampling systems. Finally, typical SNR for a baseband converter of the same number of bits can be much higher than an IF sampling converter because the bandwidth can be reduced, further improving the SNR performance.

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SFDR requirements: Spurious performance is slightly less obvious in the specifications. However, there are several guidelines in the standard that provide SFDR requirements. These are primarily found in the single- and two-tone blocking specifications. As indicated earlier, the single-tone test is in the form of a narrow-band blocker at 50 dBc and 87 dBc or 80 dBc, depending on the band of operation. In this example, the receiver can not be desensitized either by gain reduction or by direct jamming. For two-tone testing, two carriers at -45 dBm are set at 900 kHz and 1.7 MHz offset where the intermodulation product is allowed to fall 100 kHz off the channel center. Therefore, these two factors determine the conditions whereby spurious levels can be measured. In each test, the signal level increases by 3 dB to maintain the same level of performance; however, it has already been established that this increase is not required for the normal gain control loop. This indicates that the noise floor is allowed to increase by 3 dB due strictly to spurious performance. Therefore, the power of the spurious generated by these two test conditions equals the noise within one CDMA2000 channel. At the antenna, this is the available noise power plus the NF of the receiver. At maximum gain, this is about 3.1 dB including the ADC. Therefore, total effective noise at the antenna port is about -171 dBm/Hz. Integrating the noise over 1.25 MHz gives -110 dBm/1.25 MHz. For minimum gain, the total NF is about 7 dB, giving a noise density of -167 dBm/Hz or -106 dBm/1.25 MHz. If the energy due to the blocker is allowed to equal this power (-106 dBm) for their respective case, then the spurious can also be at this same level. Because this narrow-band signal has no correlation to the spreading sequence after the rake receiver, it appears simply as added Gaussian white noise.

Worst case desensitization is at 87 dBc (or -30 dBm). Under this situation, the conversion gain has been nominally reduced to 30 dB and the NF is about 7 dB. As indicated in the previous paragraph, the tolerable noise from the spurious of this single tone equals -167 dBm/Hz (or -106 dBm/1.25 MHz) at the antenna. If the ADC contributes 6 dB below this level, this provides for distortion from other components in the signal chain. Therefore, the ADC must contribute -112 dBm relative to the antenna port or include the nominal 30 dB conversion gain -82 dBm referenced to the ADC input. If the ADC full scale is 4 dBm, SFDR is about -86 dBFS.

IP3 requirements: For the case of the two-tone tests, gain is still at the maximum 42 dB and a NF of 3.1 dB. In this case as noted in the SFDR Requirements section, the in-channel spurious power is allowed to be –110 dBm (referenced to the antenna). Because multiple devices contribute to this performance, the ADC allocation is 6 dB below this level or –116 dBm. After the conversion gain of about 42 dB, the spurious level for the ADC is about –74 dBm or about –78 dBFS.

The IMD of this condition can be calculated with these conditions. Remember that as the input levels increase, the gain reduces and the IP3 also shifts. Additionally, ADCs do not have a true IP3 performance curve because most converters clip well before their third order products become as significant as noise energy. However, an equivalent IP3 can be computed for ADCs.

Spurious products need to be at -74 dBm relative to the ADC input, while the input tones to the ADC need to be near -2 dBm (-7 dBFS). Using the classic third-order intercept equation, the IP3 for the ADC alone is 34 dBm.

IP2 requirements: The source of spurious is unimportant but the results must be similar. Therefore, the spurious generated by the IP2 terms should fall to the same degree of performance. Specifically, overall spurious must fall somewhere around –110 dBm depending on the gain conditions where the problem occurs. Assumming that the ADC IP2 is 6 dB greater than the overall system, the goal is –116 dBm referenced to the antenna or –74 dBm at the ADC. However, because the slope of the intercept equation is lower for second-order terms (two vs. three), the second-order intercept is higher. Therefore, under these conditions, the required intercept point for the ADC alone can be about 68 dBm.



Figure 4.

For the receiver to meet the overall specification, the total system IP2 relative to the antenna must be at least 20 dBm. This is found by looking at two signals at -45 dBm with the resulting spurious being -110 dBm (again referenced to the antenna -45 + (110 - 45)). Using this as a reference, the IP2 requirements for the LNA, guadrature demodulator, and baseband amplifiers can also be calculated using the same ADC requirements applied to the corresponding gain to either the input or output of the stage in question, and allowing sufficient margin to account for the allowable contributions. For example, if an LNA has a gain of 15 dB, the requirement for total IP2 output of that stage is 35 dBm (20 dBm + 15 dB). This is also be the input referred IP2 of the stage after the LNA plus the required contribution margin.

Component selection: Although higher conversion gain has some benefits, the downconversion block must have a nominal, variable conversion gain between 30 dB and 42 dB, and a NF of 3 dB at the maximum gain. Additionally, the input SFDR must be greater than 80 dBFS (FS set to -30 dBm with additional dynamic range beyond that point). Finally, an input referred IP3 of -12.5 dBm is needed. These are minimums, typicals are higher. If the receiver is a direct conversion architecture, IP2 must be considered, as discussed in the IP2 Requirements section.

Synthesizer: A number of synthesizers are available that are suitable for this design. As shown in Figure 2, these include the ADF4106 ultralow noise PLL and the ADF4360x family of integrated synthesizers and VCOs. The ADF4360 family of synthesizers is well suited for applications where narrow-band blockers are moderate, which does not include many deployments for CDMA2000. However, the ADF4106 with an external VCO is an ideal candidate. Phase noise from the LO is mixed with the nearby blockers and appears as inband noise. As in the prior discussion, this noise must not cause the total noise of the channel such that reception is impaired. When noise from mixing must be at least 6 dB below antenna referenced noise of -174 dBm (not accounting for NF of the receiver), the overall contribution is minimized. If the neighbor blocker is at -30 dBm (-117 dBm + 87 dBc), the noise density must be -180 dBm/Hz. If the phase noise is considered to be flat, a requirement of -150 dBc results for the phase noise of the synthesizer. Because the blocker is located at an offset of 900 kHz and the channel edge is at about 625 kHz from the center, this number must be met by an offset of 275 kHz. Therefore, the phase noise spec should be -150 dBc (or better) at an offset of 275 kHz and beyond. In considering the 750 kHz blocker (50 dBc), the same analysis can be performed. In this case, the results are found to be about -115 dBc at 100 kHz offset.



Figure 5. Effects of Reciprocal Mixing Between an LO and a Nearby Strong Blocker

ADC: In order to implement a receiver without an AGC, the ADC SNR must be greater than 79 dBFS, such as in the AD9446. This allows the noise floor of the ADC to be below that of the analog front end. While some compromises can be made without true loss of sensitivity, the performance lost is in power measurement accuracy because the ADC contributes to the noise floor and to the ability to greatly exceed the required minimums (that is, margin). For details see the reference sited earlier. The amount of AGC and filtering determines which ADC must be used. If no AGC is that SNR of up to 83 dB should be used. However, with 6 dB to 12 dB of AGC, many 12-bit and 14-bit ADCs sampling from 61.44 MSPS to 122.88 MSPS can be used. These ADCs have SNRs ranging from 65 dBFS to 75 dBFS. At 74 dBFS, there is a about 15 dB between the ADC noise floor and the analog front-end noise floor when the AGC sets the gain to 42 dB under small signal conditions. Because only 10 dB is required, some headroom exists to allow lower performance without sacrificing performance. In this range, there are a number of converters. For IF sampling, products such as the AD9444, AD9445, AD9244, AD9245, AD6645, AD9236, AD9432, AD9433, AD9430, and AD9446 are ideal choices across the price and performance range. For baseband sampling, a number of low cost duals make ideal candidates. These include the AD9238 and AD9248, which are dual 12-bit and 14-bit converters respectively, in a pincompatible CSP package that can be specified in the bill of materials without a change in the PWB. In addition to duals and a variety of 12-bit singles not mentioned here, a quad 12-bit family, the AD9228 and AD9229, feature four ADC channels that are capable of diversity baseband sampling in a single package.

DDC: The AD6636 offers a 4-channel or 6-channel DDC option. Each of the devices has four ADC inputs and is therefore easily configured as either diversity, diversity sectored, or phased array. Because many CDMA2000 sites are configured in groups of three channels, the AD6636 can provide effective coverage including diversity with redundancy in the event of primary failure of the signal path. Because each antenna consists of an RF downconversion plus ADC, it feeds a primary DDC and a redundant DDC. Additionally, the diversity signal path

is connected to a different primary DDC and secondary DDC. In this manner, if either the main signal or diversity signal chain fails, the other can singly continue to support 3 channels. If necessary, the primary path that fails can switch over to a secondary path by sharing channel resources with another sector that has less traffic. This provides the additional redundancy needed to prevent loss of any group of channels even with multiple signal path failures. In this manner, both the main signal and diversity signal paths have redundancy in the event of a single failure. In addition, some portions of the signal path are supported by double redundancy. The redundant DDC is only used if the primary fails at which time the controlling software can reallocate resources from a different sector to augment the failed path, if required.

In addition to the channelization capabilities, other functions are provided in the DDCs. The first is power estimation. The mean square power, peak power, and the number of times the signal crosses user-specified amplitude can be measured for each ADC input. Additionally, when used in complex mode (I and Q), these measurements are done on the complex signals as well. This information can be used with the gain control of the analog front end to monitor signal levels and set the appropriate gain within a feedback loop.

Other key features include dc offset correction, IQ gain adjustment, IQ phase adjustment, and complex digital tuning. All of these features are required when implementing IQ sampling for multicarrier applications. **Integrated functions**: Currently, 14-bit ADCs are under export restriction to key countries. The AD6654 provides integration of the ADC and DDC function by combining the AD6645 and AD6636 cores in a single device. This device is classified as a receiver function and is not subject to export control. In addition, the combined Rx functions are available that integrate both transmit and receive in a single package. Devices such as the AD9863 include dual, high speed ADCs and DACs suitable for single carrier applications. This device is an excellent option for low capacity systems. Other devices are available in this family (AD986x) that offer a variety of bit precisions and speeds with many options.

Validation: With a desired sensitivity of -117 dBm in key bands, and with no blockers in band, the front-end nominal gain should be 42 dB and the NF 3.1 dB. In this condition, the signal-to-noise ratio of the full receiver chain is:

Signal = $-117 + 42 = -75 \ dBm$ Noise = $-174 + 61 + 42 + 3.1 = -67.9 \ dBm$ Resulting SNR = $-7.1 \ dB$ before despreading After despreading SNR = $13.9 \ dB$

Anything above 5 dB is excess SNR. As a result, the sensitivity of the receiver can be reduced and signals smaller than those called for in the specification can still be accommodated.



Figure 6.

Table 3.											
				Effective SNR	Nominal Gain						
Gain	AFE NF	Total NF	0 dB SNR	@ –117 dBm	Trip Point	ADC Clip Point					
42 dB	3 dB	3.1 dB	130.5 dB	13.9 dB	-42	–38 dBm					
36 dB	4.5 dB	4.9 dB	129.1 dB	12.1 dB	-36	–32 dBm					
30 dB	6 dB	7 dB	127.0 dB	10 dB	-30	–26 dBm					

Up to the two-tone test level (-45 dBm per tone or -42 dBm total), the conversion gain stays fixed. In this configuration, multiple CDMA2000 carriers can be received up to a power level of about -50 dBm without gain changes (accounting for signal peaking). If divided between 3 CDMA carriers, a power level of about -55 dBm/CDMA carrier occurs. Because the AD6636 includes hysteresis in the gain control loop, once the gain has changed, it does not continue to immediately track the envelope of the signal until the hysteresis conditions are satisfied. Additionally, it does not increase the gain until the signal level stays below the threshold for a predetermined time that can be synchronized to any signal framing information.

While the gain reduces to 12 dB in 6 dB steps, sensitivity reduces until the minimum gain setting is reached. Table 3 shows the sensitivity for each gain setting. This table shows that even in the lowest gain setting, the reference sensitivity can be met, even with multiple carriers.

Validation of SFDR sensitivity is more difficult. However, for a linear system, CW testing is clearly a more stringent test than a CDMA2000 signal. Therefore, if a CW signal at the ADC input is driven to the ADC full scale of 4 dBm (-26 dBm CW at the antenna with 30 dB of conversion gain), worst case spurious should be greater than about -86 dBFS. CDMA2000 signals with the same peak power as a sinewave exhibit a much lower rms level that the sinewave, which results in better spurious performance over the sinewave. Typical minimum SFDRs for 14-bit converters are specified at 86 dB or greater depending on frequency, and overlap well with the requirement. With –86 dBFS at the ADC, this corresponds to either –111 dBm, –117 dBm, or –123 dBm at the antenna depending on the gain setting. After the rake receiver, this is the equivalent of –172 dBm/Hz, –178 dBm/Hz or –184 dBm/Hz. Given the noise contribution of the system, these are lower than the above conditions and only begin to contribute noticeably once the spurious increases above –169 dBm/Hz (or –80 dBFS).

TRANSMIT DISCUSSION

There are several options for the architecture of the transmit signal path. Figure 7 shows a direct conversion architecture for an initial point of reference only. Section 4 of 3GPP2 C.S0010-B describes the transmit signal requirements used throughout this section. Throughout all of the architectures to be reviewed, there is an assumption that there is a channel filter at the output of the power amplifier, which is sharp enough to not desensitize the receive path and to ensure spurious emissions, when colocated, are filtered sufficiently.









Carrier configurations: CDMA2000 radio transmission technology (RTT) represents an evolution from the CDMAOne and IS95 standards. Consequently, it retains backwards compatibility with the legacy standards while also introducing updated features. A CDMA2000 base station can be deployed in the same frequency allocation as an IS95 system with different bandwidth options. The base CDMA2000 chip rate is 1.2288 mega chips per second (MCPS) with 1.25 MHz carrier spacing. Carriers modulated with a 1.2288 MCPS are referred to as having a 1× spreading rate, or being SR1 carriers. A second chip rate of 3.6864 MCPS, 3× spreading rate or SR3, is also available; both spreading rates are full-duplex.

A base station can deploy multiple SR1 carriers within a band. Figure 8a shows a typical 5 MHz bandwidth with three adjacent SR1 carriers and two 625 kHz guard bands. Multiple SR1 carriers can also be generated in nonadjacent frequency allocations. Regardless of adjacency, SR1 carriers have a finite number of code channels. Alternatively, an SR3 multicarrier (SR3-MC) deployment can be used with three adjacent carriers (see Figure 8b). An SR3-MC deployment allows more code channels and therefore, higher data rates, but it does require three adjacent frequency allocations. An added benefit of SR3-MC is its ability to overlay on SR1 carriers (see Figure 8c). The flexible SR1/SR3 approach enables existing CDMAOne and IS95 operators to migrate smoothly to CDMA2000. For example, an IS95 operator could first migrate one 1.25 MHz IS95 carrier to a CDMA2000 SR1 carrier. As data services become more popular, it could then overlay a multicarrier system on top of three 1.25 MHz carriers and progressively migrate all users to the multicarrier SR3 mode while still supporting legacy SR1 and CDMAOne users.

The original CDMA2000 specification allows an SR3 direct sequence configuration that occupies a single 3.75 MHz frequency allocation. This has since been dropped by the CDMA2000 specification and is handled as part of the CDMA2000/W-CDMA harmonization activity.

Frequency error: Each base station is required to center carriers at their assigned frequency allocation in accordance with the Band Class Specification 3GPP2 C.S0057.

Frequency allocations are based on geographic locations with different RF emission requirements for frequency allocations above 1 GHz and below 1 GHz. The placement of the carriers is subject to a ± 0.05 ppm frequency error. With such a frequency placement requirement, base stations typically derive all timing from the same reference clock, which is an integer multiple of the SR1 chip rate, 1.2288 MHz. As a result, converter sample rates of 30.72 mega samples per second (MSPS), 61.44 MSPS, 122.88 MSPS and 245.76 MSPS, representing multiplication factors of 25, 50, 100, and 200, are common in CDMA2000 systems.

Synchronization: All CDMA2000 base stations' forwardlink transmission timings are synchronized to CDMA system time, which is related to the Universal Coordinated Time (UTC). Synchronization can be achieved through several techniques including self synchronization, radio beep, or through satellite-based systems such as GPS. When all base stations are synchronized, each can be identified through a common short PN code residing in a common pilot channel. The short PN code is divided into 512 offsets with each base station adopting a specific part number (PN) offset for its identity. The short PN code allows mobile terminals to acquire the network quickly and using a common base station time reference and pilot channel allow easy hand-off of mobiles from one base station to another. A timing scheme derived from GPS also has the added benefit of providing emergency location services. Once synchronized, the base station has a basic frame length of 20 ms. Additionally, there is a 5 ms frame structure for signaling bursts, and 40 ms and 80 ms frames structures for nonreal time services.

Should the base station external time reference become disconnected, the specification requires that the base station transmit time reference be maintained at $<\pm10 \ \mu$ s error for at least eight hours. It also requires that the time accuracy of each carrier in a multicarrier base station, be $<1\mu$ s with respect to each carrier. Furthermore, the time error between the common pilot channel and code channels within a carrier must be $<50 \ ns$. These last two requirements are made easier if there is a single sample clock driving a single DAC to generate multiple carriers and a single path from the DAC to the antenna.

		Walsh Code Length											
SR	RC	256 Bits (Walsh 256)	128 Bits (Walsh 128)	64 Bits (Walsh 64)	32 Bits (Walsh 32)	16 Bits (Walsh 16)	8 Bits (Walsh 8)	4 Bits (Walsh 4)					
1	1	N/A	N/A	9.6 kbps	N/A	N/A	N/A	N/A					
	2	N/A	N/A	14.4 kbps	N/A	N/A	N/A	N/A					
	3	N/A	N/A	9.6 kbps	19.2 kbps	38.4 kbps	76.8 kbps	153.6 kbps					
	4	N/A	9.6 kbps	19.2 kbps	38.4 kbps	76.8 kbps	153.6 kbps	307.2 kbps					
	5	N/A	N/A	14.4 kbps	28.8 kbps	57.6 kbps	115.2 kbps	230.4 kbps					
3	6	N/A	9.6 kbps	19.2 kbps	38.4 kbps	76.8 kbps	153.6 kbps	307.2 kbps					
	7	9.6 kbps	19.2 kbps	38.4 kbps	76.8 kbps	153.6 kbps	307.2 kbps	614.4 kbps					
	8	N/A	14.4 kbps	28.8 kbps	57.6 kbps	115.2 kbps	230.4 kbps	460.8 kbps					
	9	14.4 kbps	28.8 kbps	57.6 kbps	115.2 kbps	230.4 kbps	460.8 kbps	1036.8 kbps					

T.I.I. 4

Radio configurations: Radio configurations (RC) define the physical channel configuration based upon a specific channel data rate. Each RC specifies a set of data rates based on either 9.6 kbps or 14.4 kbps, and each is determined by the spreading rate. RC1 and RC2 are provided for backward compatibility to CDMAOne and IS95. RC3 is the first CDMA2000 radio configuration with all the new coding features. Table 4 shows the possible data rates determined by spreading rate (SR) and radio configuration. Base stations can transmit channels with different RCs at the same SR.

All channels are mutually orthogonal because the bits they carry are spread with mutually orthogonal, variable length Walsh codes. A CDMA2000 system orthogonal spreading code is chosen from a Walsh tree that can grow from Dimension 4 to Dimension 256. The Walsh code length varies to accommodate the different data rates and spreading rates of the different radio configurations. When the data rate increases, the symbol period is shortens. For a specific spreading rate the chip rate is constant; therefore, fewer Walsh code chips are accommodated per symbol period, that is, the Walsh code length is shorter. One effect of using variable length Walsh codes for spreading is that a shorter code precludes using all longer codes derived from it (see Figure 9a). If a high data-rate channel uses a 4-bit Walsh code such as 1, 1, -1, -1, all lower data rate channels using longer Walsh codes starting with 1, 1, -1, -1 need to be inactive. Figure 9b shows the code domain where the high data rate channel power is spread over the lower data rate code channels (the cyan color is a single high rate channel). Individual Walsh codes are identified by Wn^N, where N is the length of the code and n is the row in the N \times N Hadamard matrix. For example, W₂⁴ represents Code 2 of the 4 × 4 Hadamard matrix (4-bit Walsh code). Therefore, W_2^4 precludes using W_2^8 and W_6^8 , W_2^{16} , W_6^{16} , W_{10}^{16} , W₁₄¹⁶, and so on. Walsh codes have the disadvantage of being able to become code-limited, whereby all codes in the Walsh tree are used. To overcome this, CDMA2000 defines a set of quasi-orthogonal functions (QOF) as an extension to the orthogonal code set. QOFs are another orthogonal code set that minimizes the correlation with the original orthogonal code set.







Figure 10.

Code domain formation: The code domain consists of a number of common channels and user specific traffic channels. The forward common pilot channel (F-PICH), or pilot channel, is a channel continuously transmitted by all CDMA2000 base stations. It consists of a constant value of 1 (see Figure 10) scrambled by the short PN code as previously described. The pilot channel is used for acquisition and as a reference for coherently demodulating the other forward link channels; it always occupies Walsh Code 0. When using transmit diversity, a transmit diversity pilot channel (F-TDPICH) is transmitted from the diversity antenna. The F-TDPICH then enables the mobile terminal to estimate the channel and recover information transmitted from the diversity antenna. A mobile terminal uses the pilot channel to demodulate the forward synchronization channel (F-SYNC) or sync channel. The sync channel is scrambled with the same sequence as the pilot signal; it can be coherently demodulated and decoded. The sync channel carries system information such as system identities, code offset, system time, diversity mode, and paging channel information. The sync channel repeats every 26.666 ms and is synchronized with the pilot channel. The sync channel spans exactly three pilot channels and is used by the mobile terminal to acquire the 20 ms frame boundaries. The sync channel always occupies Walsh Code 32. When idle, the mobile terminal should be powered down to minimize power. However, the mobile terminal also has to regularly monitor the network

for incoming traffic. In CDMA2000, traffic is divided into a paging indication phase and a message transmission phase; the page indication is very short so that the mobile terminal can process it very quickly, minimizing power use. The mobile terminal wakes up and decodes the message transmission only if it is targeted at the terminal; the information to determine this is contained in the quick paging channel (F-QPCH). There can be 16 quick paging channels at mobile terminal registration, where they tell the network its preferred paging channel.

The traffic channels can include several physical channels. The fundamental channel (F-FCH) transports medium rate data or voice at any rate from 750 bps to 14.4 kbps. The supplemental channel (F-SCH) supports high rate data services and can be allocated on a frame by frame basis. A dedicated control channel (F-DCCH) can also support bursty user data or signaling. Figure 11 contains a channel flow diagram for an SR1, RC3 F-FCH. The full-rate data bits have an added CRC, and are upsampled to 38.4 kbps where they are combined with a decimated long code applied to the user long code mask. The result is normalized to a fixed code channel gain followed by an adjustment for closed loop power control. The output is converted to two polar data trains where they are spread with the Walsh code assigned to this channel. Finally, they are scrambled by the base stations short code. The two polar outputs are then filtered before upconversion.





The 3GPP2 specification defines a nominal test model for the main transmit path in nondiversity mode, as shown in Table 5. The model combines pilot, sync, a single paging channel and six traffic channels; it is intended to provide a real-life loading scenario. The location of the channels can be seen on the code domain plot (see Figure 12). The specification also defines a minimum code domain metric called code domain power that can be considered code domain noise. If there is too much code domain noise, the receiver's ability to correctly decorrelate the signal channels is reduced. The code domain power is a measure of code orthogonality and needs to be maintained

Table. 5									
Channel Type	Numbers of Channels	Fraction of Power (dB)	Comments						
Forward Plot	1	-7.0	W0 ⁶⁴						
SYNC	1	-13.3	W ₃₂ ⁶⁴						
Paging	1	-7.3	W1 ⁶⁴						
Traffic	6	-10.3	Variable Full Rate Code Channels						

at a minimum level to ensure quality of service for each user. For SR1 and Walsh-64 codes, the code domain power in each inactive code channel is 27 dB below the total output power of each carrier; for SR1 and Walsh-128 codes it is 30 dB, and for SR3 and Walsh-256 it is 33 dB.

Although the 3GPP2 specification does not call for an error vector magnitude (EVM) requirement, it is useful to relate code domain power to the EVM. This can be done with Equation 1, where SF is the spreading factor and is the Walsh code.

Code domain error (CDE) = $10\log^{10}(EVM^2/SF)$ (1)



Figure 12.

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Power control: Power control enables users to transmit just enough power to meet their quality of service requirements in varying channel and loading conditions. This strategy increases overall system capacity because the dominant resource allocated among users in CDMA systems is neither time nor frequency slots, but transmit power. Additionally, power control prolongs the battery life of mobile terminals. From the base station's perspective there are three types of power control. Forward closed-loop power control is operated at 800 Hz for both forward and reverse paths. Its main purpose is to ensure the base station transmits just enough power to achieve the desired signal-to-noise ratio for the target code channel. The mobile terminal feeds information about signalto-noise ratios to the base station in the receive link, requesting it to adjust the power level; the base station instructs the mobile terminal to adjust its power until the desired signal-to-noise ratio is satisfied, thereby closing the loop. Closed-loop power control aims at reducing the effects of fast fading. The forward link's power control bits are punctured into the channel data stream (see Figure 11); the punctured power control bits do not appreciably affect the error rate. Forward outer-loop power control is used to set the closed-loop power control's bit error rate thresholds based on quality of service (QoS) requirements for the mobile terminal code channel. It is monitored by looking at the frame error rates received from the mobile terminal and aims at reducing fading fluctuations. Open-loop power control is used to combat slow fading effects; the base station adjusts its power to be inversely proportional to the received signal power. It also acts as a safety fuse when the closed-loop power control fails. When the forward link is lost, the closed-loop reverse link power control can freewheel and the mobile terminal can interfere with an adjacent cell. The open-loop reduces the terminal power as it gets closer to adjacent cells limiting the possible impact.

In addition to controlling the power delivered to the mobile terminal, the base station has control the RF total mean power delivered to the antenna. The specification requires this to be controlled to within +2 dB to -4 dB from the manufacturers rated power level over all environmental conditions. There is an additional requirement for the ratio of the pilot channel power to the total mean power expressed which needs to be maintained to within ±0.5 dB of the configured value.

Peak-to-average ratio (crest factor): The power amplifier that drives the antenna has opposing performance metrics when considering efficiency and linearity. The amplifier is most efficient when driven into saturation, however, it also has its worst linearity in saturation. Conversely, an amplifier driven for linearity is highly inefficient. Typically, a compromise is found between linearity and efficiency, which results in amplifiers operating in a mode where the average operating point is set such that the signal crests are slightly less than the maximum saturated output power that the amplifier can deliver. Determining and maintaining the peak-toaverage ratio (PAR) and power amplifier linearity is one of the largest challenges in base station design.

The carrier waveform is usually pulse-shaped in nature to form a band-limited waveform. This waveform, depending on the number of users and type of information being transferred, can cause very high PAR waveforms if the component signals are added in phase. Combining multiple carriers further increases the probability of phase alignment, and increases the PAR. The increased PAR lowers the power amplifier efficiency if a certain level of linearity is to be maintained.





Figure 13.



Because the PAR is heavily dependent upon the traffic in the channel, the 3GPP2 nominal test model is used for conformance tests. To help determine the PAR of a waveform, the complementary cumulative distribution function (CCDF) is used to show the probability of a peak happening within this frame. A common metric of acceptability is the 10⁻⁴% probability level. Peaks with lower probability than 10⁻⁴% contribute very little to the actual intermodulation performance of the amplifier and are usually handled by allowing the amplifier to go into saturation or by clipping within the digital processing. For the single carrier case using the nominal test model, a peak-to-average ratio of approximately 9.6 dB results for a 10⁻⁴% probability. Figure 13 shows the measured CCDF of the code domain plot of the nominal test model (see the Code Domain Formation section). As previously mentioned, if multiple carriers are combined with little attention paid to the resulting PAR, the resulting PAR can be very high. Figure 13 shows simulated CCDF plots for multiple adjacent, equal power, RC3 nominal test model carriers. By selecting the Walsh codes carefully, the PAR can be minimized across carriers.

Peak-to-average power reduction: The lower the PAR, the higher the average power can be made for the same efficiency. Peak-to-average power reduction techniques (PAPR) can be used to reduce peaking without introducing out-of-band distortion. The typical method of PAPR is clipping followed by filtering. Clipping has the negative impact of significantly reducing the modulation accuracy and creating new spectral signals that must be filtered. The AD6633 provides PAPR without clipping the baseband or IF signals. It uses a technique that selectively introduces in-band distortion to reduce the peaks without causing distortion in adjacent bands. This allows modulation accuracy to trade-off directly with compression and without adjacent channel distortion. Additionally, in multichannel applications, the amount of modulation accuracy degradation can be allocated differently for each carrier, facilitating quality of service differentiation between carriers. For example, voice carriers can be allocated low modulation accuracy in favor of high speed data carriers that need higher modulation accuracy for the higher data rates. This can not be achieved by clip and filter techniques.

Figure 14 demonstrates the performance of the AD6633 with three, equal power, RC3 nominal test model carriers apart by 1.25 MHz. The time domain plot (see Figure 14a) clearly shows the effect of the PAPR in action. The CCDF plot (Figure 14b) shows an uncompressed sum exhibiting peaks approximately 4 dB greater than the compressed sum for a probability of 10^{-4} %; the more carriers the greater the reduction in PAR for a given probability. Figure 14c shows the out-of-channel spectra unaffected by the PAPR algorithm.

Power amplifier linearization: Another method of increasing the efficiency of the power amplifier is allowing the amplifier to move closer toward saturation, which increases efficiency, but also compensates for the resulting distortion. There are two main approaches to PA linearization. Analog feedforward uses linear feedforward compensation amplifiers around the main power amplifier to counter the distortion problems and provide sufficient linearity so that spectral regrowth does not pollute adjacent channels. This approach typically results in efficiencies less than 10% and is a complicated, but tractable, analog problem where the feedforward amplifier linearity also needs to be considered.







A second approach to PA linearization comes in the form of digital predistortion. This method uses the simple concept that a digital numerical representation is very linear and highly predictable, with no effect from environmental operating conditions. Therefore, if the transfer function of the PA can be determined, summation with an equal and opposite transfer function, (see Figure 15), results in a highly linear system response, which introduces no noise or distortion. Furthermore, the manufacture of the analog feedforward amplifiers is no longer needed and a cheaper digital process can be used.

Consider the impact on the converters for a syttem implementing digital predistortion. In the forward path, any signal passed through a power amplifier is disturbed in two ways: first, additive noise is introduced to the signal, and second, a nonlinear PA transfer function leads to even-and-odd order intermodulation products; the odd-order products need careful consideration. Thirdorder intermodulation products spread the distortion over three times the bandwidth of the carrier; fifth-order intermodulation spreads it over five times the bandwidth, and seventh-order intermodulation spreads it over seven times the bandwidth. For a single carrier needing carrier bandwidth of BMHz, third-order distortion occupies a band between (B/2) MHz and (3B/2) MHz on either side of the wanted carrier center (see Figure 16b). Recalling that the intent of digital predistortion is to create antidistortion, a system employing digital predistortion needs control over a bandwidth three, five or seven times the signal bandwidth to completely

null out third-, fifth-, or seventh-order intermodulation products. In the case of three CDMA2000 carriers (signal bandwidth 3.75 MHz), control over a bandwidth of 18.75 MHz is required if fifth order IM products are of interest. Additionally, a few decibels of extra dynamic range are usually required for predistortion algorithms.

In the observation path, a sample of the RF output signal is mixed down and converted back to digital baseband data where it is compared to the transmitted data. To remove fast-moving power profiles, the downconverted signal is averaged over many hundreds of samples. The algorithms used to create the corrected transfer function can be based on either a polynomial multiplication or a look-up table. A DSP function can be used to implement the algorithm in which the downconverted and averaged result is compared to the transmitted signal to determine the amount of distortion added by the forward path upconversion process. Once determined, the inverse distortion is computed and then used to modify the future look-up table or polynomial coefficients. The coefficient update can take seconds to complete and captures not only distortion due to power profiles of the carriers, but also temperature and aging effects.

There are a number of approaches to capture the distortion. One approach mixes the transmitted signal down close to dc and uses a high speed ADC to sample a bandwidth equal to the order distortion times the RF spectrum bandwidth. Thus, if fifth-order terms are to be corrected, a Nyquist band of 37.5 MHz is required for six CDMA2000 carriers; a sample rate of 92.16 MSPS could be used for this function (see Figure 17a).



Figure 17.

An alternate approach mixes down to a low intermediate frequency (IF) and undersamples the transmitted signal. With this approach, the ADC samples the signal and the third-order distortion components without aliasing; the fifth- and higher order distortion terms alias over the third-order terms and are compensated by the coefficient control, (see Figure 17b.) For the six carriers of CDMA2000 and an IF of 76.8 MHz, a 61.44 MSPS converter is sufficient.

The ADC limitation is that it must introduce less distortion than the distortion measured at the antenna while having a noise spectral density less than the antenna wideband emission requirements. Typical SFDR requirements range from -70 dBc to -75 dBc. Because much averaging is taking place the ADC quantization noise can be averaged over multiple samples. Worst-case Category B emissions require that antenna wideband noise at output frequencies above 1 GHz need to be less than -30 dBm/1 MHz or -90 dBm/Hz. The antenna signal is normally attenuated between 40 dB to 50 dB to reduce the maximum PA output to that of the fullscale ADCs; the directional coupler can provide a significant part of the loss from the antenna to the ADC input. This puts the spectral density of ADC input at about -135 dBm/Hz. Across a 46.08 MHz Nyquist band this corresponds to an ADC SNR of about 58 dB or greater. The AD9215 provides mid-to-high 70 dBc of SFDR up to Nyquist with an SNR of 58 dBc when sampling at either 61.44 MSPS or 92.16 MSPS.

Transmit diversity: Diversity techniques are usually employed to counter the effects of channel fading. The base station's signal is transmitted through multiple antennae that are spaced far enough apart that the signals emanating from each antenna can be assumed to undergo independent fading paths. If one of the paths undergoes a deep fade at the mobile terminal, an auxiliary path is unlikely to be in deep fade and the mobile terminal could recover the signal. Antenna spacing and mobile terminal velocity affects the degree of correlation between the signals at the mobile terminal. Large antenna spacing on the order of several carrier wavelengths leads to uncorrelated fading, which leads to maximum performance gain at the mobile terminal when the velocity of the mobile terminal is slow (pedestrian environment); this channel is characterized as having a flat fading profile. Beamforming methods use antenna spacing less than the carrier wavelength, typically half the wavelength, and are most suitable for fast moving mobile terminals (vehicular environment); this channel is characterized as having a frequency selective profile.

There are two generic approaches to transmit diversity. Temporal (delay) diversity, transmits a bit streamon one antenna and the same bit stream is delayed by one or more sample instants on another antenna (see Figure 18a). The effect of delay diversity on a slowly fading channel is that the mobile terminal coherently combines the two fading channels into a stronger received signal. This approach suffers from low throughput due to multiple transmissions of the same symbol over time. Frequency diversity, shown in Figure 18b, employs transmission of multiple symbol replicas over multiple carriers, each separated by a sufficiently large amount of frequency to ensure independent fading. The effect of frequency diversity for a slow fading channel is similar to temporal diversity in that the mobile terminal coherently combines the two fading channels to aid demodulation. Frequency diversity has the added cost and complexity at both the transmitter and receiver to detect two frequency allocations, and is difficult to implement in a band-limited spectrum.

Transmit diversity in CDMA2000 systems is generally based on temporal diversity, exploiting the fact that Walsh codes are orthogonal and can be slipped by one symbol period to put the delay element in the temporal diversity scheme.



Figure 18.





There are two classes of transmit diversity used in CDMA2000. Orthogonal transmit diversity, Figure 19a, is an example of open loop transmit diversity. The encoded data stream is split into two different streams for simultaneous transmission over different transmit antennae. Different Walsh codes are used for both streams to maintain the orthogonality. To maintain the effective number of Walsh codes per user as in the single antenna configuration, the spreading length is doubled. In addition to the normal pilot channel (F-PICH) on one channel, the transmit diversity pilot channel (F-TDPICH) is transmitted on the other antenna to aid in coherent detection at the receiver. The second class of transmit diversity is closed loop transmit diversity; selection transmit diversity, Figure 19b, is an example. The power received by the mobile terminal may not yield the highest signal-to-noise ratio under fading conditions. Ideally, the transmitter chooses the antenna that yields the highest received signal-to-noise ratio. However, this is not possible because the transmitter does not know the state of the channel between the base station and the mobile terminal, hence a feedback channel is used from the mobile terminal to the base station indicating which of the two antennae has a higher received signalto-noise ratio.

Of the two classes of transmit diversity available to CDMA2000, open-loop schemes offer greater advantages to fast moving mobile terminals; the close-loop schemes are better at overcoming flat fading channels (which are more common to slow moving mobile terminals). The implication for the converters is that the number of DACs should match the number of antennae being used, preferably with a matched transfer function; single-chip, dual DACs, such as the AD9767, AD9777, and AD9779, are ideal for two-antenna systems. **Adjacent channel power ratio:** An integrated power in a bandwidth at frequency f_{OFF} from the center of the carrier contains both broadband noise and distortion, (see Figure 20a). The integrated power can be expressed as both a ratio with respect to the carrier power (adjacent channel power ratio (ACPR)) or as an absolute value.

If a second carrier is added at the same mean output power of the PA, (see Figure 20b), the distortion bandwidth occupies the order of distortion multiplied by the signal bandwidth. Third-order distortion occupies a bandwidth from B'/2 MHz to 3B'/2 MHz, where B' is twice B. Hence, the total distortion bandwidth occupied increases linearly with the number of carriers added (with respect to the single carrier case). For the two carrier case and the same PA mean output power, the mean power per carrier is reduced by 10log₁₀(#carriers), 3 dB in the two carrier case. Each carrier's distortion is also reduced by 10log₁₀(#carriers), but because there are two adjacent carriers, the distortion components intermodulate to increase the total distortion by 10log₁₀(#carriers). Consequently, if a multicarrier ACPR measurement is taken at the same frequency offset as the single carrier case, the signal power decreases by 10log₁₀(#carriers) and the integrated distortion power stays the same; the ACPR is degraded by 10log10(#carriers) everytime a carrier is added with respect to the single carrier case. Furthermore, if the frequency offset is multiplied by the number of carriers added, (see Figure 20c), the noise power spectral density in the same integration bandwidth is the same as the single carrier case, resulting in the same ACPR. This can be used to its advantage by recognizing that multicarrier integrated bandwidths at frequency offset, f'_{OFF}, can be referred to a single require-





Figure 21.

ment by dividing the multicarrier frequency offset, f'_{OFF} , by the number of carriers. These observations are consistent regardless of the shape of the distortion, provided the PA operates at the same mean output power.

The importance of reducing the PAR of the composite signal has been highlighted in Figure 21. Note that the power statistics of the signal to determine the power level of nonlinear blocks in turn determine the ACPR for a given intercept point. Current literature suggests that improving the PA's effective IP3 by around 15 dBm is possible with peak-to-average ratio reduction and digital pre-distortion techniques. For a nonlinear element, the linearity is dominated by third-order distortion. The distortion around a single carrier of CDMA2000 can be approximated by the following equation:

$$ACPR \approx 16.12 + 10 \log_{10} \left(\frac{P_0^2 \Delta f}{48 \times OIP3^2 B} (3 - \Omega_0)^2 (3\Omega_0^2 - 8\Omega_0 + 9) \right)$$
(2)

where:

 Δf is the integration bandwidth (normally 30 kHz)

 $\Omega_0 = 2f_0/B$

 f_0 is the offset frequency from the center of the carrier

B is the chip rate (1.2288 MHz for SR1).

 P_0 is the channel power measured in a 1.2288 MHz integration bandwidth, as per the 3 GPP2 specification, and both P_0 and OIP3 are expressed in watts.

The OIP3 can be referred to the intermodulation distortion (IMD) by the following equation:

$$OIP3 = P_o + \frac{IMD}{2}$$
(3)

Using Equation 2 and Equation 3 with the previous observations about referring multicarrier frequency offset ACPR measurements to a single carrier, it is possible to determine the linearity requirements of the signal chain elements from the 3GPP2 specification. To verify the accuracy of Equation 2 and Equation 3, the third-order intercept (TOI) of a signal generator is measured, (see Figure 21a). The measured OIP3 is used with a nominal test model RC3 SR1 carrier to calculate an expected 750 kHz offset ACPR of -72.72 dBc and an expected 1.98 MHz offset ACPR of -84.89 dBc. These calculated results compare favorably with the measured results (see Figure 21b).

Equation 2 does not capture the effect of the noise floor on the ACPR. Figure 22 is a sweep of the channel power for a single WCDMA carrier with Test Model 1 for the AD8349 (a CDMA2000 plot exhibits a similar behavior). With channel powers down to about –15 dBm, the ACPR is dominated by linearity. While the channel power drops, the ACPR becomes dominated by the noise, degrading ACPR.



Figure 22.





Modulation accuracy (rho): rho is a measure of correlated power to total power. The correlated power is computed by removing frequency, phase and time offsets, and by performing a cross correlation between the corrected measured signal and the ideal reference. If a transmitted signal correlates perfectly, a rho of 1.00 results; as the correlation becomes less than ideal rho drops below 1.00. If some of the transmitted energy does not correlate, excess power appears as added noise that can interfere with other users; rho is therefore, the ratio of signal power to signal power plus error power. The 3GPP2 specification defines the waveform quality using a single pilot channel only and requires rho to be greater than 0.912. Frequency error, time offset, and I/Q origin offset (carrier feedthrough) are often measured in conjunction with rho to provide insight into the overall health of the base station's transmitted signal (see Figure 23a).

Frequency error measures how close the specified carrier frequency allocation is to the measured waveform. As previously mentioned, the 3GPP2 specification requires a ±0.05 ppm frequency error. As a result, a carrier in-band 8 (1800 MHz) requires greater than 90 Hz frequency accuracy. The time offset measures the PN short code offset; the 3GPP2 specification recommends less than 10 μ s. The I/Q origin offset gives an indication of the carrier feed through; if it is too high, the I/Q origin offset can corrupt the constellation and dominate the value of rho. Composite rho can also measure the modulation accuracy with multiple code channels and a pilot channel (see Figure 23b). The measurement involves descrambling and despreading the measured signal to calculate the reference signal. It accounts for all spreading and scrambling problems in the active channels and for all baseband, IF and RF impairments. If rho is determined only by component linearity, the following equation provides a good approximation:

$$\rho = 1 - \frac{4P_o}{3OIP3}$$

Modulation accuracy (EVM): Although it is not specified in the 3GPP2 specification, the error vector magnitude is a useful measure of the modulation accuracy. By examining the constellation and taking the displacement of each measured dot from the reference position as an error vector modulation accuracy can be assessed (see Figure 24). The reference position is determined from a reference signal that is synthesized by demodulating the received signal to symbols and then remodulating these symbols perfectly to form the reference constellation. The rms of the error vectors is expressed as a percentage of the overall signal magnitude, called the error vector magnitude.



Figure 24.

EVM can be calculated as either uncoded or coded EVM. For uncoded EVM, the reference signal is computed from the received bits, therefore it does not detect coding errors. It is sensitive to any impairments that occur in the baseband filters, I/Q modulator, and IF and RF sections of the transmitter. The 3GPP2 specification measures waveform quality with a single pilot channel. This waveform maps directly to a QPSK constellation. Like composite rho, coded EVM is computed by descrambling and despreading the measured signal to obtain a reference.

(4)

The difference between rho and coded EVM is that coded EVM calculates the error as the vector difference between the measured and reference signals, while rho performs a cross correlation between them. EVM can be related to rho by the following equation:

$$EVM(\%) = 100 \times \sqrt{\frac{1}{\rho}} - 1 \tag{5}$$

Limitations on emissions: Spectral emissions, other than in-band signals, can become interferers to adjacent carriers, adjacent cells, and even the base station receiver. The 3 GPP2 specification (excluding the PAMR bands) defines two emissions groups based upon whether the carrier is above or below 1 GHz. Band classes 0, 2, 3, 5, 7, 9, and 10 are <1 GHz frequency bands whereas band classes 1, 4, 6, and 8 are >1 GHz. Within each emissions group there are two ITU categories, A and B. ITU categories are mainly governed by the country of deployment. For example, Korea and USA predominantly adhere to ITU category A emissions, whereas Europe mainly uses category B emissions. The emissions requirements determine the linearity, wideband noise, and dynamic range requirements of the converters (and other components). To best illustrate this, two examples will be considered, both for a 30 W total mean output power. The examples are based on the simplified signal chain in Figure 25, where the mixer can either be a quadrature modulator or a real mixer.



Figure 25.

Three carriers < 1 GHz with ITU Category B emissions: Consider first the emissions requirements that determine linearity. Figure 26a is a single carrier using the nominal test model; the mean output power is 30 W (44.77 dBm/1.2288 MHz). Close in to the carrier, there is a separation requirement of 45 dBc measured in a 30 kHz integration bandwidth with respect to the carrier power integrated over a 1.2288 MHz bandwidth of 750 kHz to 1.98 MHz offset from the center of the carrier. For a single carrier, this represents the bandwidth occupied by thirdorder distortion terms, 614.4 kHz to 1.8432 MHz from the center of the carrier; higher order distortion terms will occupy this bandwidth, but are typically of lower magnitude than the third. The 3GPP2 specification also requires -60dBc/30kHz at offsets from 1.98 MHz to 4 MHz; this band contains no third order distortion, but contains fifth order distortion. For a single carrier, the linearity requirements are therefore set by the 750 kHz offset requirement of -45 dBc/30 kHz, which if 3 dB margin is added over the specification, requires -48 dBc/30 kHz. For three carriers, as shown in Figure 26b, the antenna power is constant so the power per carrier drops by 10log₁₀(#carriers) to 40 dBm per carrier with a signal bandwidth of 3.7288MHz. Third-order distortion terms occupy a bandwidth of 614.4 kHz to 4.3432 MHz from the center of the outermost carriers. The single carrier close-in requirement does not apply to multiple carriers, so the first emission limit is determined by ITU Category B emissions of -36 dBm/1 kHz at a 4 MHz offset from the center of the outer most carriers; adding 3 dB margin over the specification gives a -39 dBm/1 kHz requirement at a 4 MHz offset. This requirement sets an ACPR of -64.23 dBc/30 kHz at a 4 MHz offset with three carriers. This ACPR can be referred to a single carrier requirement by dividing the offset from the carrier edge by three, which gives an approximate 1.129 MHz offset requirement from the edge of a single carrier (1.743 MHz from center) of -64.23 dBc/30 kHz; see Figure 26c. Examining the linearity requirements for the single carrier and three carrier case finds that the three carrier requirement of -64.23 dBc/30 kHz at 4 MHz offset dominates slightly over the single-carrier requirements.





Next, consider the requirements for noise. The single carrier case has an integrated carrier power of 44.77 dBm/ 1.2288 MHz (see Figure 27a). It has a peak-to-average ratio of 9.67 dB that is reduced by peak-to-average power reduction by 2.5 dB, which allows 3 dB more dynamic range for digital predistortion and puts the DAC full scale (0 dBFS) at 54.94 dBm/1.2288 MHz. Assuming there is no channel filter within 16 MHz offset of the center of the carrier, a -36 dBm/100 kHz ITU Category B emissions requirement is at 16 MHz offset. This allows 3 dB specification margin and gives a -83.05 dB dynamic range, or expressed differently, a -143.94 dB/Hz noise power spectral density. For the three carrier case, shown in Figure 27b, the peak-to-average ratio is slightly higher, but the peak-to-average power reduction engine does better on more carriers, yielding a 55.44 dBm/1.2288 MHz DAC full scale. The ITU requirements are absolute values giving the same requirements as the single carrier case; the dynamic range requirement becomes -83.55 dB or -144.44 dB/Hz.

In Figure 27, the linearity is determined by the -39 dBm/+1 kHz at the 4 MHz offset, whereas the noise is determined by the -39 dBm/+100 kHz wideband requirement. If a mixer/modulator similar to the AD8349 is used at the complete signal chain (see Figure 28), it

should have an output channel power around -15 dBm. Allocating 20 dB gain to the VGA requires a gain of 40 dB in the PA to deliver approximately 45 dBm from the output of the DAC. It is assumed that PA linearization is used, giving a 15 dBm OIP3 improvement in the PA. The AD8349 has an OIP3 of approximately 18 dBm and VGAs such as the ADL5330 have OIP3s exceeding 20 dBm for 20 dB of gain. Calculating the cascaded OIP3 at the output of the PA gives 65.55 dBm and suggests that the overall OIP3 is dominated by the PA and that it is quite insensitive to the linearity of the DAC. If the preceding stages are assumed distortion-free, then the cascaded OIP3 results in -38.62 dBm/+1 kHz at the 4 MHz offset.

The AD8349 quadrature modulator has a noise contribution of approximately –156 dBm/Hz. Setting the DAC and synthesizer noise contributions equally at –157 dBm/Hz means that to achieve the wideband noise requirement of –39 dBm/100 kHz with this gain planning, the VGA and PA are required to have a NF of 3 dB. With this level plan the DACs mean output is at –15 dBm; with an 11 dB due to peak-to-average overhead the DACs full-scale output is at –4 dBm, and the DACs dynamic range therefore needs to be –153 dBFS/Hz. With this signal chain an approximate rho of 0.9883 dB and code domain power of –37.32 dB results.



PA		VGA		MIXER			DAC		SYNTHESIZ		ZER
OUTPUT POWER	45	OUTPUT POWER	5	OUTPUT POWER	-15		OUTPUT POWER	-15			
INPUT POWER	5	INPUT POWER	-15	INPUT POWER	-15		INPUT POWER	-15			
GAIN	40	GAIN	20	GAIN	0	1	GAIN	0			
IIP3	26	IIP3	20	IIP3	18	1	IIP3	29			
OIP3	66	OIP3	40	OIP3	18	1	OIP3	29			
NF	3	NF	3	NSD	-156		NSD (dBm/Hz)	-157		NSD	-157
							IMD3	70		4MHz OFFSET	
TOTAL OIP3		NOISE		4MHz OFFSET			PAR OVERHEAD	11			
(dBm)	65.55	(dBm/100kHz)	-38.23	(dBm/1kHz)	-38.62		0dBFS (dBm)	-4			
Rho	0.9883	EVM (%)	10.896	CDP (dB)	-37.32		NSD (dBFS/Hz)	-153			

Figure 28.



Figure 29.

Six carriers >1 GHz with ITU Category A emissions: The single carrier case for linearity is shown in Figure 29a. For carriers in bands above 1 GHz, there is a different set of emissions limitations; the first requirement is -45 dBc/+30 kHz from 885 kHz to 1.25 MHz; the second is a -45 dBc/+30 kHz requirement at 1.25 MHz offset or -9 dBm/+30 kHz, whichever is more stringent. The next limitation is at 1.98 MHz, but because a single carrier's third-order distortion does not occupy 1.98 MHz, the defining limitation on a single carrier's linearity for a 44.77 dBm/1.2288 MHz carrier is the -9 dBm/+30 kHz requirement. For the six carriers case shown in Figure 29b, per carrier power is now 36.99 dBm/1.2288 MHz, occupying a distortion bandwidth of 7.479 MHz from the edge of the outermost carriers. For multiple carriers, the -9 dBm/30 kHz at 1.25 MHz is a requirement, but does not define the linearity. There is a requirement starting at 2.25 MHz offset of -13 dBm/1 MHz that limits. With 3 dB margin over the specification, the ACPR requirement becomes -68.21 dBc/30 kHz at 2.25 MHz offset. Referring back to the single-carrier case, divide the frequency offset from the edge of the carrier by six including a defining linearity requirement of -68.21 dBc/30 kHz at 887 kHz frequency offset. This is a more difficult linearity requirement than the single carrier case (see Figure 29c).



Figure 30.





For Category A emissions, the noise requirements for both the single carrier and the six carrier cases are almost identical for the same output power. In Figure 30a, the single carrier case has a 9.67 dB peak-to-average ratio with 2.5 dB reduction for peak-to-average power reduction and 3 dB extra dynamic range for digital predistortion, which gives the carriers a peak of 54.94 dBm/ 1.2288 MHz. Category A emissions limit the noise to -13 dBm/+1 MHz at a 4 MHz offset. After adding 3 dB of margin, this requires 70 dB of dynamic range or -130.94 dB/Hz noise power spectral density. In Figure 31b, the six carrier case has 12.9 dB of peak-to-average ratio, but can be reduced by 6 dB with peak-to-average power reduction. Allowing 3 dB extra dynamic range for digital pre-distortion puts the peaks at 54.67 dBm/ 1.2288 MHz, which is approximately the same as the single carrier peak.



Figure 32.

The linearity requirements are determined by the six carrier requirement of -16 dBm/+1 MHz at 2.25 MHz offset. The wideband noise is defined by the -16 dBm/+1 MHz Category A emissions plus margin requirement. Using the same mixer and DAC as the three carrier design, shown in the signal chain (see Figure 31), the noise requirements are more relaxed than the three carrier requirements, but the linearity requirements are more difficult to achieve. As the PA and to lesser degree, the VGA, dominate the linearity, the majority of effort should be placed at the expense of noise performance. In this design, the DAC's noise requirement is -150 dBFS/Hz, with a slightly greater linearity requirement of 75 dBc IMD3. This system has an overall OIP3 of 75.152 dBm and produces a rho of 0.9987 with a code domain power of -46.96 dB. The modulation accuracy figures reflect the higher linearity required to meet the 2.25 MHz offset requirement for spectral emissions.

Superheterodyne single upconversion: Superheterodyne single upconversion relies on low noise, high performance, IF output DAC technology (see Figure 32). If PA linearization is used with correction for the fifth order intermodulation products, five times the signal bandwidth is required; for six adjacent carriers, this requires approximately 40 MHz. A convenient IF at the DAC output is a decade away from the final RF frequency, 80 MHz to 200 MHz. There are many options to synthesize carriers at these frequencies. The first, shown in Figure 33a, is a high sample Nyquist rate converter such as the AD9726 or AD9736. The update rate of the DAC, f_{DAC}, is the same as the input data rate, f_S. For sample rates above 250 MSPS, LVDS data inputs should be considered. As the carriers in the first Nyquist zone increase in frequency, the second Nyquist zone images decrease. Thus, the higher the output carrier frequency for the same sample rate, the more aggressive the analog reconstruction filter needs to be. An alternative to using high speed LVDS inputs is lower speed CMOS inputs and interpolating the DAC output (see Figure 33b). This approach uses a digital low-pass filter to suppress the second and third input Nyquist zone image; the interpolation image is further suppressed by the analog reconstruction filter. For the same DAC update rate as the Nyquist rate DAC, the interpolating DAC has slightly less than half the usable bandwidth and produces an image that needs consideration. If an image of the input sample rate is needed, the interpolation filters can be operated in high-pass mode (see Figure 33c). The analog reconstruction filter requirements between the Nyquist and interpolation approaches for the same DAC sample rate are comparable with the interpolation approach suffering from the added interpolation image. For a fixed input sample rate, the interpolation approach allows the analog reconstruction filter to relax while the unfiltered image is pushed higher in frequency. The AD9772A is a good fit for 2× interpolation up to 320 MSPS update rate.



Figure 33.

Another approach for generating IF signals is to digitally mix a baseband signal to an IF. A single DAC always outputs a real signal and is mirror symmetrical around 0 Hz in multiples of $f_{DAC}/2$. Consequently, when a real signal is subjected to a real digital mix, the negative frequencies move into positive frequency and interpolation images fold on top of the desired signal (see Figure 34). Fortunately, the interpolation images are in phase with the desired signal and do not cause any distortion. This approach creates a congested spectrum that requires a bandpass filter to select the desired signal.



Figure 34.

If a complex baseband is available, a complex interpolation is possible (see Figure 35a); a complex spectrum is no longer mirror symmetrical around dc, but is still mirror symmetrical around f_s . With a digital complex mix, the entire complex spectrum undergoes a frequency shift, with no aliasing (see Figure 35b). However, the DAC still only produces a real signal, so if the complex mix output drives a DAC, any asymmetric around dc spectrum potentially causes interpolation images to fold on top of the desired signal and be out of phase with the signal, which causes distortion (see Figure 35c).

The AD9786 has a single DAC and accepts either a real or complex input, and does a complex mix with the ability to reject interpolation images folding out of phase. The AD9777 and AD9779 are dual DAC devices with two channels of interpolation filtering. They can perform either real or complex mixing; a single DAC output can be used if a real output is needed, or the device can operate as two, single-transmit chains for a two antenna diversity system. With the exception of the AD9777 and AD9772A, all mentioned DACs have approximately -160 dBm/Hz noise power spectral density and greater than 70 dBc IMD over the desired frequency range. The LVDS input DACs are capable of producing at least a 300 MHz Nyquist band. The AD6633 can still be coupled to the AD9786, AD9777, and AD9779 to provide peak-toaverage power reduction and fine frequency tuning. The AD6633 also has the ability to act as a control interface to a DVGA for power control.

If the DAC produces a high IF, the DAC's sin(x)/xresponse needs considering. The DAC has a zero order hold of the data that produces a frequency domain response with a sin(x)/x characteristic (see Figure 36a). The response has deep nulls at multiples of the DAC sample frequency, f_{DAC}, and at half the DAC sample rate there is a 3.92 dB loss. This is important for multicarrier signals at high frequencies with respect to the DAC sample rate, because it causes inband roll-off that effects the EVM and therefore rho and code domain power; the effect is worse the higher the output frequency. The sin(x)/x response can be digitally compensated (see Figure 36b). When synthesized by the DAC an inverse sin(x)/x transfer function can be superimposed on the data such that the response is essentially flat. The disadvantage of this is that the final output signal is attenuated by approximately 4 dBFS and the inverse sin(x)/x filter is only bound up to a fraction of the Nyquist rate (0.42 f_{DAC} in the previous example). Consequently, using images in higher Nyquist zones is usually not realized with simple sin(x)/x filters. The sin(x)/x compensation can be implemented at almost any stage of the transmit path and if digital pre-distortion is being implemented, the overhead to add sin(x)/x compensation is trivial. If the sin(x)/x compensation in the DAC is desired, the AD9779 has an inverse sin(x)/x compensation filter.











Direct conversion: This technique is desirable for its simplicity, flexibility, and relative low cost of implementation (see Figure 37). The carriers are synthesized by the DACs as a complex pair and then mixed to RF by a quadrature modulator, which performs a complex frequency translation, but only outputs the real component of the mix. The baseband carriers shown in Figure 38a can either be centered on dc or offset from dc; the DAC outputs are filtered to remove any images before upconversion in the quadrature modulator, (see Figure 38b). For an ideal quadrature modulator, a perfect single sideband upconversion results.



Nonidealities in the complex-to-real translation can lead to LO feedthrough and unsuppressed sidebands at the RF frequency. By using a low-IF direct upconversion approach, the LO feedthrough and unsuppressed image are moved away from the desired sideband, allowing them to be filtered. For an odd number of permanently on carriers, the carriers can be placed on dc, thereby minimizing the effect of unsuppressed sidebands and LO feedthrough. For an even number of permanentlyon carriers, the carriers can be placed symmetrically around dc, thereby making the LO feedthrough appear



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as an adjacent interferer that is subject to emissions limitations. For any number of carriers in which carriers can be turned off, the frequency allocation of the turnedoff carrier can be filled with an unsuppressed sideband, which is also subject to emissions limitations. The cause of the LO feedthrough and unsuppressed sideband can be compensated for. If a digital predistortion loop is used, the correction can be a part of that loop. Alternatively, the output of the quadrature modulator can be mixed back down to baseband and corrected independently.

There are two main error components that can cause poor sideband rejection. Figure 39a shows the effect of

a quadrature gain error in the complex path's constellation. As expected, the nonideal constellation causes poor EVM and consequently, poor rho and code domain power. To achieve sideband suppression in the 60 dBc to 70 dBc range, the quadrature gain error has to be less than a couple of tenths of a percentage point (see Figure 39b).

The second main error component is quadrature phase errors. These errors tend to twist the constellation, degrading rho and code domain power (see Figure 40a). To achieve sideband suppression in the 60 dBc to 70 dBc range the quadrature phase error needs to be less than a couple of tenths of a degree (see Figure 40b).



Figure 40.





Figure 41.

The cause of LO feedthrough is predominantly due to quadrature offsets in the complex path. Offsets shift the origin of the demodulated constellation, degrading EVM, as shown in Figure 41a. Figure 41b shows the degradation from an ideally matched quadrature path. LO feedthrough is subject to the emissions limitation and typically needs to be 70 dBc to 80 dBc below the total mean output power of the base station.

Because modulators can only be rated to a sideband rejection of -40 dBc, a phase accuracy of 0.5 degrees, and DAC outputs may only match to 1%, it is important to be able to adjust the IQ balance. This can be accomplished by either adjusting the baseband digital data or the gain and offset of the DAC output. If done in the digital baseband, this can be part of the baseband predistortion or through a standalone routine. However, 1% or more of the total dynamic range of the DAC and modulator can be consumed. Digital adjustment of the gain, offset, and phase can be done using the AD6633. The most suitable DAC to partner the AD6633 is a pair of AD9786s, which have sufficient dynamic range that a 1% degradation should not effect system performance. Alternatively, a DAC that includes gain and offset adjustment functions can be selected such as those found in the AD9777 and AD9779. Using the AD9777 or AD9779 does not reduce the dynamic range of the DAC but does require a dynamic interface between the controller and the DAC control port. Additionally, the AD9779 has the ability to ac couple the DAC outputs to the modulator

and still have offset adjustment on the modulator side of the ac coupling.

In summary, the AD9777 or AD9779 and AD8349 are recommended for direct conversion architectures. In addition to the features and functions mentioned, these devices are optimized to work together by providing a smooth interface between devices, including matched common-mode input levels. Following the modulator, an RF VGA is typically used to maintain the PA output level as operating conditions change. The ADL5330 has a gain adjust range of 60 dB and is well suited to this application. In conjunction with the RF VGA, a power detector is required. Devices such as the AD8362 are matched to the power control range of this RF VGA with a detection range of 60 dB.

CDMA2000 1xEV-DO: The requirements for high rate packet data access are detailed in the 3GPP2 specification C.S0032-0. The carriers overlay existing CDMA2000 1xRTT carriers providing improved data services. The channel formation is fundamentally different from 1xRTT, however the radio requirements are very similar. The limitations on emissions are the same as discussed in this document, but the waveform quality factor, rho, is improved to 0.97. The impact of this is that the system has to be more linear with similar noise requirements. As shown by the radio designs, the linearity is dominated by the PA and has minimal impact on the converter performance requirements.

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