ANALOG DEVICES

AN-775
APPLICATION NOTE

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Implementing the Auto-Offset Function on the AD9880

by Del Jones

Introduction

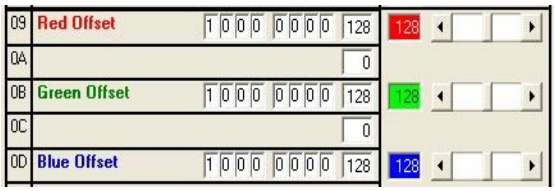
The AD9880 incorporates an auto-offset function. The auto-offset works by monitoring the output of each ADC during the clamp period and then calculating the required offset setting to yield a given output code. When auto-offset is enabled (Register 0x1C:7 = 1), the settings in the "target code" Registers (0x09, 0x0B, 0x0D) are used by the auto-offset circuitry as desired clamp codes. The circuit compares the output code after clamp (but still during the "back porch") to the target code and adjusts the offset up or down to compensate. In auto-offset mode, the Offset Registers (0x08, 0x0A, 0x0C) are 8-bit twos complement words, with Bit 7 of their respective registers being the sign bit.

Changes to Register Definitions

The definition of Registers 0x08 to 0x0D change depending on whether the automatic clamp feedback function is enabled or not. Figure 1 and Figure 2 describe these differences. The target code and offset adjust registers are independent. The target code registers are disabled when auto-offset is turned off.

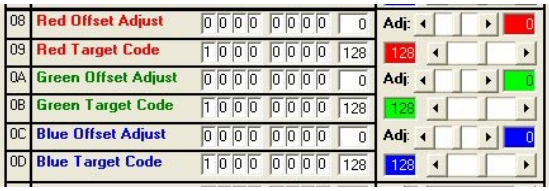
More Auto-Offset Related Register Definitions

In addition to the offset and target code registers, the registers defined in Table I also support the auto-offset function.



OFFSET REGISTERS CONSIST OF 8 BITS (BINARY NOTATION) THAT ARE USED TO ADJUST THE OFFSET OF THE ADC.

Figure 1. AD9880 with Auto-Offset Disabled



REGISTERS 0x09, 0x0B, 0x0D ARE TARGET CODES (8-BIT BINARY) IN THIS MODE. OFFSET REGISTERS ARE MOVED TO 0x08, 0x0A, 0x0C AND ARE IN TWOS COMPLEMENT NOTATION.

Figure 2. AD9880 with Auto-Offset Enabled

Brightness Adjustment

If auto-offset is disabled, the Offset Registers (0x09, 0x0B, 0x0D) control the absolute offset added to the channel. The offset control provides ±85 LSBs of adjustment range (code 0 = –85 bits of offset, code 128 = 0 offset, code 255 = +85, and so on) with 1 LSB of offset corresponding to 2/3 LSB of output code.

Table I. Auto-Offset Related Register Definitions

Register	Function	Bits	Description	
0x1C	Auto-Offset Control	7	Auto-Offset Enable	1 = Auto-offset enabled 0 = Auto-offset disabled
		6:5	Update Mode	00 = Update every clamp 01 = Update every 16 clamps 10 = Update every 64 clamps 11 = Not valid
		4:2	Unused Bits	Use default setting 001
		1:0	Test Bits	Must be set to 10 for proper operation
0x1D	Test Bits	7:0	Must be set to 0xFF for proper operation	

With auto-offset enabled, Registers 0x09, 0x0B, 0x0D contain target codes for the auto-clamp feedback circuit. The Offset Registers (0x08, 0x0A, 0x0C) are still used to adjust brightness. The difference is that when auto-offset is enabled, the offset register values are in twos complement notation with Bit 7 being the sign bit. The effective range for adjusting offset (used for brightness control) is +63/–64 LSBs. When developing software to control brightness, this must be taken into consideration.

Using Auto-Offset

To activate the auto offset mode, set Register 0x1C, Bit 7 to 1. Next, the Target Code Registers (0x09, 0x0B, 0x0D) must be programmed. The values programmed into the target code registers should be the output code desired from the AD9880 during the back porch reference time. For example, for RGB signals, all three registers would normally be programmed to a very small code (4 is recommended), while for YPbPr signals, the green (Y) channel would normally be programmed to a very small code and the blue and red channels (Pb and Pr) would normally be set to 128. Any target code value between 1 and 254 can be set, although the AD9880's offset range may not be able to reach every value. Intended target code values range from (but aren't limited to) 1 to 40 when ground clamping and 90 to 170 when midscale clamping.

The ability to program a target code for each channel gives users a large degree of freedom and flexibility. While in most cases all channels will be set to either 4 or 128, the flexibility to select other values allows for the possibility of inserting intentional skews between channels. It also allows for the ADC range to be skewed so that voltages outside of the normal range can be digitized. (For example, setting the target code to 40 would allow the sync tip, which is normally below black level, to be digitized and evaluated.)

Finally, when in auto offset mode, the manual Offset Registers (0x08, 0x0A, 0x0C) have new functionality. The values in these registers are digitally added to the value of the ADC output. The purpose of doing this is to match a benefit that is present with manual offset adjustment. Adjusting these registers is an easy way to make brightness adjustments. Although some signal range is lost with this method, it has proven to be a very popular function. To be able to increase and decrease brightness, the values in these registers in this mode are signed twos complement. The digital adder is only used when in auto-offset mode. Although it cannot be disabled, setting the offset registers to all 0s will effectively disable it by always adding 0.

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Table II. Example Register Settings for Enabling Auto-Offset

	RGB Auto-Offset Clamping			YPbPr Auto-Offset Clamping		
Reg.	**Value**	**Description**		**Value**	**Description**	
0x08	0x00	Red offset	Registers used for brightness control: +63/–64 LSB range	0x00	Red offset	Green register only for brightness cntl: +64/–64 LSB range
0x0A	0x00	Green offset		0x00	Green offset	
0x0C	0x00	Blue offset		0x00	Blue offset	
0x09	0x00	Red target code	Ground clamped targets = 4	0x80	Red target code	Red, Blue targets = 128; Green target = 4
0x0B	0x04	Green target code		0x04	Green target code	
0x0D	0x04	Blue target code		0x80	Blue target code	
0x1C	0xCE	Enables auto-offset and updates the auto-offset every 64 clamps		0xCE	Enables auto-offset and updates the auto-offset every 64 clamps	
0x1D	0xFF	Values for proper operation		0xFF	Values for proper operation	