ANALOG DEVICES

AN-774
APPLICATION NOTE

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Implementing the Auto-Offset Function on the AD9981

by Del Jones

INTRODUCTION

The AD9981 is the first display electronics (DEPL) device to incorporate the auto-offset function. The auto-offset function works by calculating the required offset setting to yield a given output code during clamp. When auto-offset is enabled (Register 0x1B:5 = 1), the settings in Registers 0x0B – 0x10 are used by the auto-offset circuitry as desired clamp codes (or target codes) rather than an offset value. The circuit compares the output code after clamp (but still during the "back porch") to the target code and adjusts the offset up or down to compensate. In auto-offset mode, the target code is an 11-bit twos complement word, with Bit 7 of 0x0B being the sign bit for the red channel (Bit 7 of 0x0D for green; Bit 7 of 0x0F for blue).

Changes to Register Definitions

The definition of registers 0x0B – 0x10 changes depending on whether the auto-offset function is enabled or not. Figure 1 and Figure 2 describe these differences.

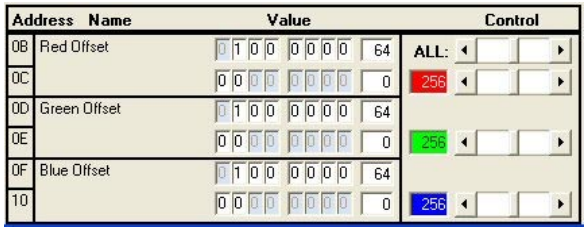


Figure 1. AD9981 with Auto-Offset Disabled

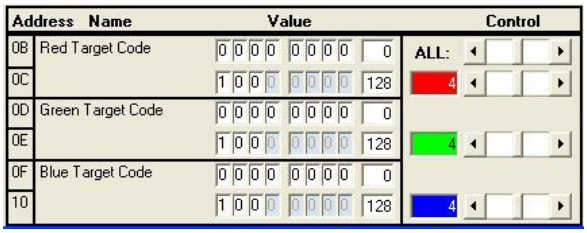


Figure 2. AD9981 with Auto-Offset Enabled

Brightness Adjustment

If auto-offset is disabled, the lower 9 bits of the offset registers control the absolute offset added to the channel. The offset control provides a + 255/–256 LSBs of adjustment range, with 1 LSB of offset corresponding to 1 LSB of output code.

With auto-offset enabled, Registers 0x0B – 0x10 now contain target codes instead of offset values. These registers can still be used to adjust brightness. The difference is when auto-offset is enabled, the exact black code output is now being adjusted so that the user knows exactly to what code the black level is being set. This is particularly useful for applications that desire to match NTSC or other video specifications that use less than full-scale code ranges. For example, if there is a requirement to only use 75% of the code range (code range of 128 – 896) for the Y input of a component video system, the Y (green) target code can be set to 512 and the gain adjusted to achieve the 896 maximum output code. When developing software to control brightness, this must be taken into consideration.

Target Code Value Restrictions

Even though there are 11 bits in the target code registers (10 bits plus 1 sign bit), there are only 9 bits of actual adjustment range. Also, a target code of 0 is invalid. So, the range of valid target codes is as follows:

- For ground-clamped inputs:

  –255 (111 0000 0001) to –1 (111 1111 1111)

  1 (000 0000 0001) to +255 (000 1111 1111).

- For midscale-clamped inputs:

  256 (001 0000 0000) to 767 (010 1111 1111).

This should also be taken into consideration when developing software for brightness control.

Using Auto-Offset

To activate the auto-offset mode, set Register 0x1B, Bit 5 to 1. Next, the Target Code Registers (0x0B – 0x10) must be programmed. The values programmed into the target code registers should be the output code desired from the AD9981 during the back porch reference time. For example, for RGB signals all three registers would normally be programmed to a very small code (4 is recommended but any code between ±255, except 0, is valid), while for YPbPr signals the green (Y) channel would normally be programmed to a very small code (4) and the blue and red channels (Pb and Pr) would normally be set to 512. For midscale-clamped inputs, any target code value between 256 and 767 is valid, although the AD9981's offset range may not be able to reach every value. Example register settings for the auto-offset mode are shown in Table I.

The ability to program a target code for each channel gives users a large degree of freedom and flexibility. While in most cases all channels will be set to either 4 or 512, the flexibility to select other values allows for the possibility of inserting intentional skews between channels. It also allows for the ADC range to be skewed so that voltages outside of the normal range can be digitized. (For example, setting the target code to 160 would allow the sync tip, which is normally below black level, to be digitized and evaluated.)

Table I. Example Register Settings for Enabling Auto-Offset

	RGB Auto-Offset Clamping			YPbPr Auto-Offset Clamping		
Reg.	**Value**	**Description**		**Value**	**Description**	
Rx0B	0x00	Red offset MSB	Red target code = +4	0x40	Red offset MSB	Red target code = +512d
Rx0C	0x80	Red offset LSBs		0x00	Red offset LSBs	
Rx0D	0x00	Green offset MSB	Green target code = +4	0x00	Green offset MSB	Green target code = +4
Rx0E	0x80	Green offset LSBs		0x80	Green offset LSBs	
Rx0F	0x00	Blue offset MSB	Blue target code = +4	0x40	Blue offset MSB	Blue target code = +512d
Rx10	0x80	Blue offset LSBs		0x00	Blue offset LSBs	
Rx18	****000*	Bits 3:1 = '000'. This sets all three channels to ground clamp.		****101*	Bits 3:1 = '101'. This sets the red and blue channels to midscale clamp and the green channel to ground clamp.	
Rx1B	**1*****	Bit 5 = '1'. This enables the auto-offset clamping.		**1*****	Bit 5 = '1'. This enables the auto-offset clamping.	
Rx1B	***xx***	Bits 4:3 = '10'. This sets the auto-offset circuits to operate every 64 clamps. '00' = every clamp: '01' = 16 clamps; '11' = every VSYNC.		***xx***	Bits 4:3 = '10'. This sets the auto-offset circuit to operate every 64 clamps. '00' = every clamp; '01' = 16 clamps; '11' = every VSYNC.	

Clamp Timing

The internal logic for the auto-offset circuit requires from 16 to 40 data clock cycles (programmable in 8-clock steps via Bits 4:3 of Register 0x2E) to perform its function. This operation is executed immediately after the clamping signal is deactivated. Therefore, it is important to deactivate the clamp signal at least 16 to 40 (depending on 0x2E – 4:3) data clock cycles before active video. This is true whether using the AD9981's internal clamp circuit or an external clamp signal illustrated in Figure 3. So, given these requirements, it must be ensured that

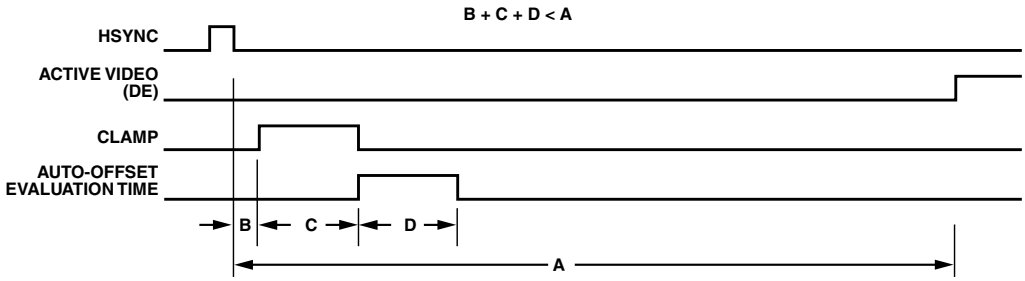
Clamp Placement + Clamp Duration + Auto-Offset Evaluation Time < Back Porch Time

Or, referring to Figure 3

The definition of Bits 4:3 of Register 0x2E is shown in Table II. To provide the maximum amount of clamping time, it is recommended to program these bits to "00".

Table II. Auto-Offset Evaluation Time Register Bit Definition

Register	Bits	Description	
0x2E	4:3	Auto-Offset Evaluation Time	00 = 16 clocks 01 = 24 clocks 10 = 32 clocks 11 = 40 clocks



A: BACK PORCH TIME—VARIABLE, DEPENDING ON VIDEO MODE.
B: CLAMP START TIME (CLAMP PLACEMENT)—PROGRAMMABLE IN THE AD9981.
C: CLAMP TIME—PROGRAMMABLE IN THE AD9981.
D: TIME REQUIRED BY THE AUTO-OFFSET CIRCUIT—PROGRAMMABLE IN 8-CLOCK STEPS FROM 16–40 PIXEL CLOCK PERIODS.

Figure 3. Clamp Timing Requirements

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