AN-751
APPLICATION NOTE

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High Speed Universal Op Amp Evaluation Board with Exposed Paddle

by John Ardizzoni

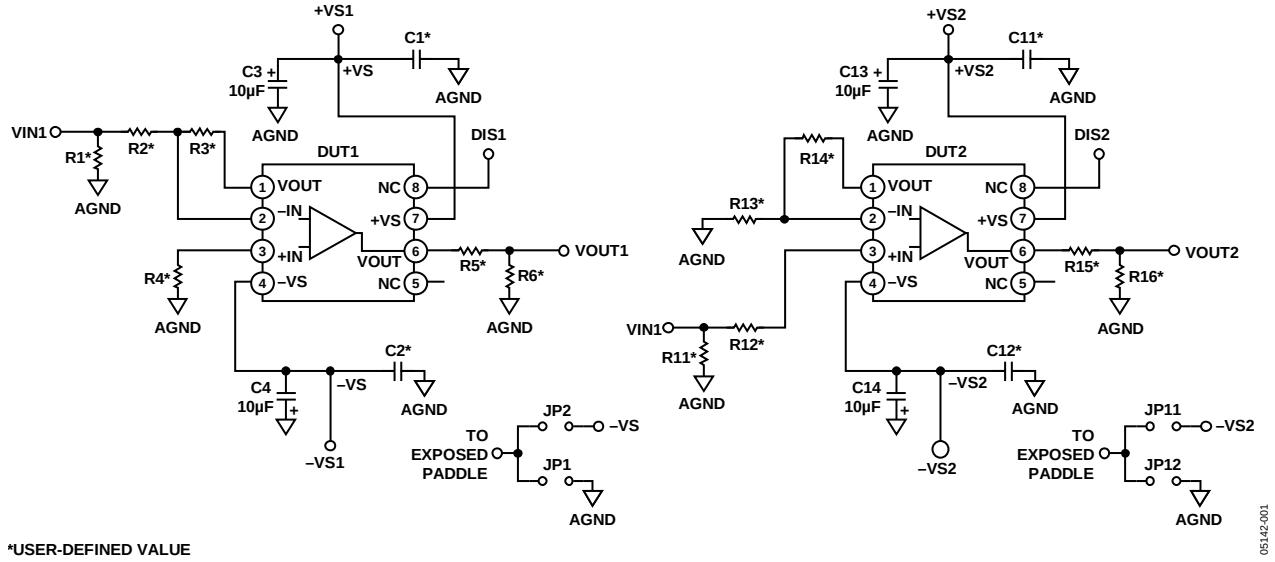
The Analog Devices, Inc., high speed, universal evaluation boards are designed to help customers quickly prototype and evaluate new designs. This application note covers two evaluation boards, the EVAL-ADOPAMP-1REZ (for 8-lead SOICs) and the EVAL-ADOPAMP-1CPEZ (for 8-lead LFCSPs). These evaluation boards are designed for amplifiers that require a voltage potential on the exposed paddle, such as the AD8045. However, these boards can also be used with standard SOIC and LFCSP packages. These evaluation boards, unlike other evaluation boards, have both an inverting and noninverting amplifier circuit on the same board. The two amplifier circuits are completely independent.

The separate sections allow for optimal performance in inverting or noninverting configurations and offer the designer even greater circuit flexibility. The schematics for the evaluation boards are shown in Figure 1 and Figure 2.

These evaluation boards are 2-layer board that accommodate edge-mounted SMA connectors on the inputs and outputs. The SMA connectors allow for efficient connection to test equipment or other circuitry. The boards also have pin connectors for supply voltages, grounds, and power-down. The assembly drawings are shown in Figure 3 through Figure 6.

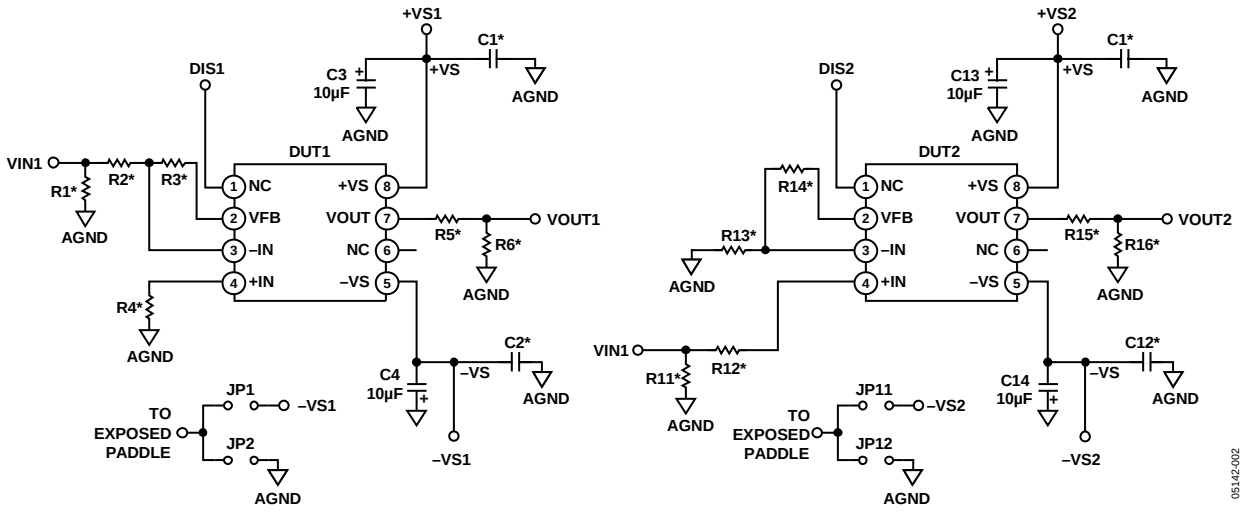
The ground plane, component placement, and supply bypassing are laid out to minimize parasitic elements and provide optimum high frequency performance. The board SMT components are primarily 0603 case size, with the exception of the electrolytic bypass capacitors, C1 and C4. If designers want to incorporate any of the aspects of the evaluation board layout into their design, the board layout patterns are included as shown in Figure 7 through Figure 10.

The evaluation boards allow the designer three options for the exposed paddle voltage: floating (or no connection to a voltage potential), ground, or to the negative power supply. The exposed paddle voltage is selected via the solder jumpers JP1, JP2, JP11, and JP12. The jumpers are shown in Figure 1 and Figure 2. To connect the exposed paddle to the appropriate voltage, simply apply solder between the two jumper pads; the pads are close enough that the solder makes the actual connection between the pads. There is no need for any additional components. This is one of the only times when a solder bridge is a good thing.



*USER-DEFINED VALUE

Figure 1. Universal Evaluation Board Schematic (SOIC)



*USER-DEFINED VALUE

Figure 2. Universal Evaluation Board Schematic (LFCSP)

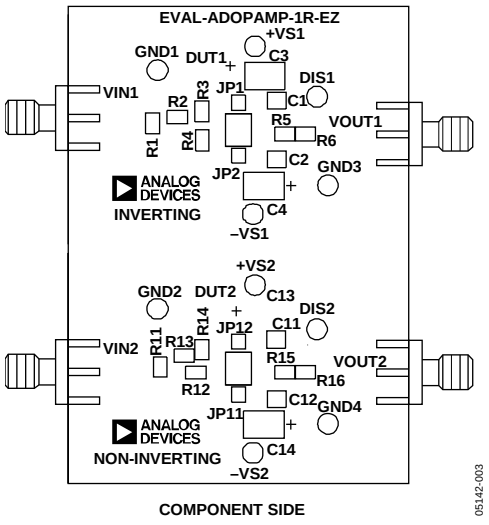


Figure 3. Board Assembly Drawing (SOIC)

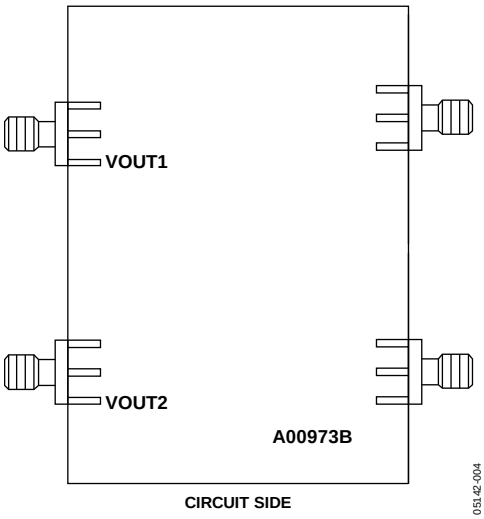


Figure 5. Board Assembly Drawing (SOIC)

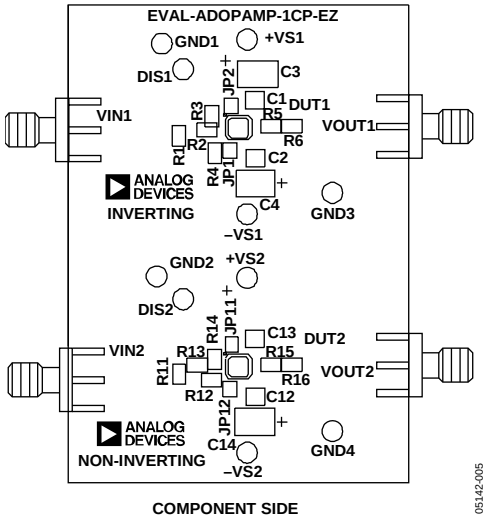


Figure 4. Board Assembly Drawing (LFCSP)

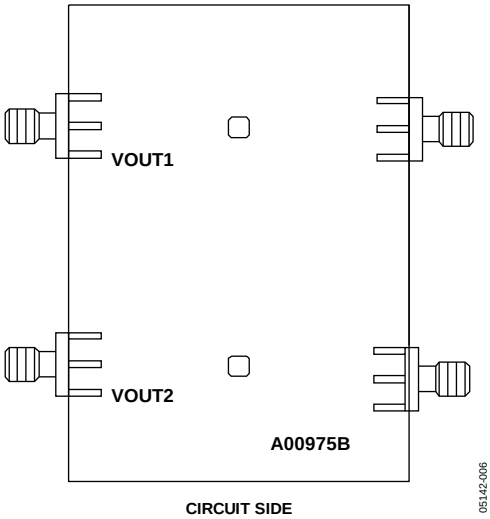


Figure 6. Board Assembly Drawing (LFSCP)

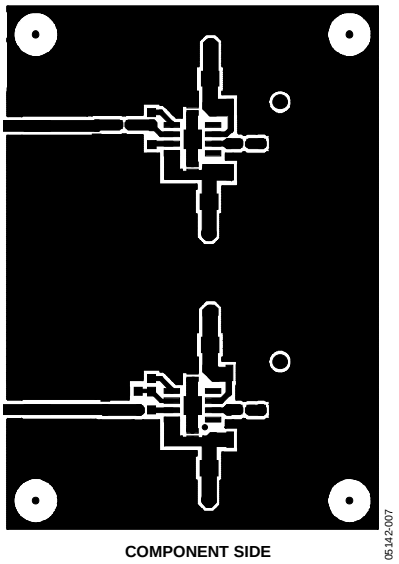


Figure 7. Board Layout Patterns (SOIC)

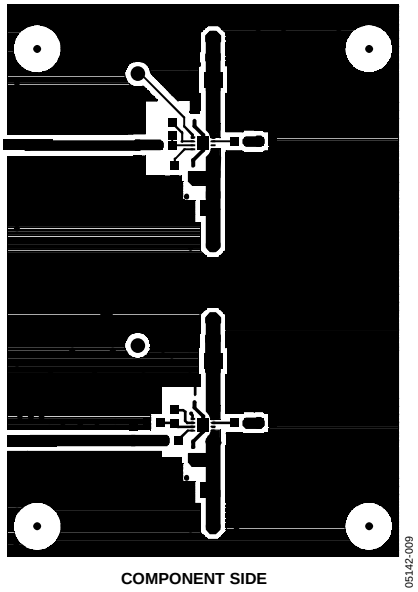


Figure 8. Board Layout Patterns (LFCSP)

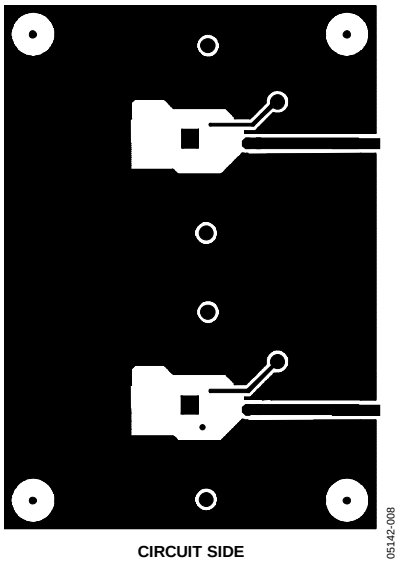


Figure 9. Board Layout Patterns (SOIC)

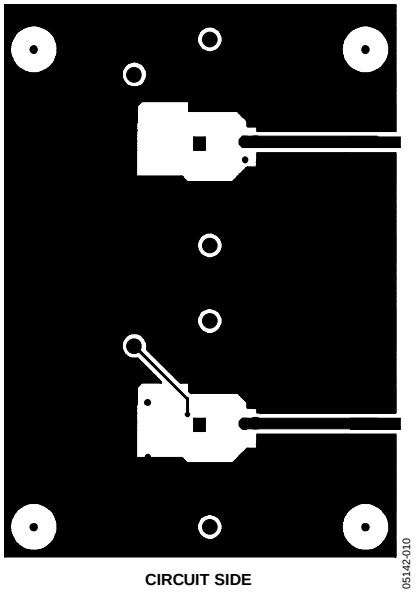


Figure 10. Board Layout Patterns (LFCSP)

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