

AN-667 APPLICATION NOTE

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Up/Down Sequence of Supplies Using the ADM1060

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INTRODUCTION

The ADM1060 is a fully programmable supply sequencer and supervisor. It can be used as a complete supply management solution in any system using multiple voltage supplies. Such applications include line cards in telecommunications infrastructure equipment (central office, base stations, etc.) and "blade" cards in servers.

One very powerful function of the ADM1060 is the ability to sequence the turn-on of as many as seven supplies in any order the designer requires. Furthermore, the ADM1060 can be used to sequence the turn-off of the supplies, in an order independent of the power-up sequence. This application note describes how to easily program this function using intuitive GUI based software available from Analog Devices. This note should be referred to in conjunction with the ADM1060 data sheet and the ADM1060 Evaluation Tools note.

THREE-SUPPLY UP/DOWN SEQUENCE

Suppose the user wants to sequence three supplies (3.3 V, 2.5 V, and 1.8 V) so that they turn on in order, starting with the supply with the highest voltage and continuing in descending order, with a 100 ms delay between each supply. Some time later, they are to turn off in the reverse order. The 3.3 V is always available on the board, while the 2.5 V and 1.8 V are generated by LDOs on the board, using the 3.3 V supply as a voltage input.

The sequence described is shown in the timing diagram below.

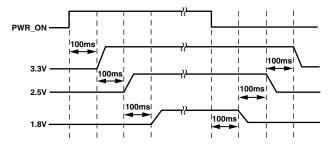


Figure 1. Power-Up and Power-Down Sequence

We will use the programmable reset generator inputs (supply fault detectors, or SFDs) of the ADM1060 to ensure that the supplies are in tolerance. These can be assigned as follows:

Table I. Supply Fault Detector Assignment

Supply	ADM1060 Input Pin	Fault Type	Minimum Threshold Voltage (V)
3.3 V	VP1	Undervoltage	3.135
2.5 V	VP2	Undervoltage	2.375
1.8 V	VP3	Undervoltage	1.71

We will use the programmable driver outputs (PDOs) on the ADM1060 to enable all of the supplies. These can be assigned as follows:

Table II. Programmable Driver Output Assignment

Supply	Driver Output	Output Configuration		
3.3 V	PDO1	Charge Pump*		
2.5 V	PDO2	Logic		
1.8 V	PDO3	Logic		

*PDO1 is configured as a charge pump output because it is required to drive the gate of a FET.

With the resources of the ADM1060 assigned as outlined above, the hardware can be configured as described below.

Since PDO1 is to be used to turn on and off the 3.3 V supply, we will use PLB1 to program the logic required to control the 3.3 V supply. We will use Function A to control the power-up and Function B to control the power-down. Similarly, for programming PDO2 and PDO3, we will use PLB2 and PLB3.

POWER-UP SEQUENCE

The following sequence occurs at power-up:

- 1. PWR_ON goes high.
- 2. 100 ms later, the 3.3 V supply to the rest of the board is enabled when the FET is turned on.
- 3. The voltage on the source of the FET rises to a minimum threshold level, for example, within 5% of nominal (i.e., 3.13 V).

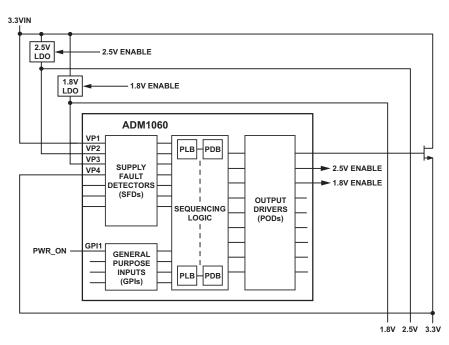


Figure 2. Sequencing of Three Supplies, Controlled by the ADM1060

- 100 ms after the threshold voltage is reached, the 2.5 V LDO is enabled.
- 5. The 2.5 V LDO output rises to a minimum threshold level, again say, within 5% of nominal (i.e., 2.375 V).
- 6. 100 ms after the 2.5 V supply reaches its minimum threshold, the 1.8 V LDO is enabled.

The power-up sequence logic is shown in Figure 3.

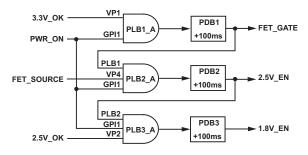


Figure 3. Logic Diagram for Three-Supply Power-Up Sequence

POWER-DOWN SEQUENCE

The following sequence occurs at power-down:

- 1. PWR_ON goes low.
- 2. 100 ms later, the 1.8 V supply is disabled.
- 3. 100 ms after the 1.8V supply drops below its minimum threshold (say 5% below nominal, or 1.71 V), the 2.5 V supply is disabled.
- 4. 100 ms after the 2.5 V supply drops below 2.375 V, the 3.3 V supply is disconnected from the board when the FET is turned off.

When PWR_ON goes low, the 2.5 V and 3.3 V supplies must stay on. If just the function shown in Figure 3 were used, all the supplies would turn off once PWR_ON—and therefore GPI1—went low. We need to make the control of 2.5 V_EN and 3.3 V_FET_GATE dependent on a different set of conditions. To achieve this we will use the B function. We therefore need to switch control of the outputs from Function A to Function B. The easiest way to achieve this is using the GPI1 signal; when this is high (i.e., when power is on), Function A is in control; when GPI1 is low (i.e., we want the system to power down), Function B is in control. We therefore make Function B dependent on GPI1, which is high, when GPI1 is low.

The power-down sequence logic is shown in Figure 4.

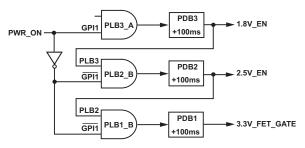


Figure 4. Logic Diagram for Three-Supply Power-Down Sequence

PROGRAMMING THE ADM1060

An example of how the SFD is programmed is shown below. All of the SFDs are programmed in a similar manner.

Supply Fault Detectors	>
VH VP1 VP2 VP3 VP4 VB1 VB2	
VP 1	- 20
Eval Board Input Voltage Target UV Threshold of +3.3V - 5% Target UV Threshold 3.134V Actual UV value 48h UV Threshold Code Range 2V to 6V Fault Type Gitch Filter 100us Delay	

Figure 5. Programming the Supply Fault Detectors The setup required for the PWR_ON signal (GPI1) is shown in Figure 6.

PI1	GPI2	GPI 3	GP14				
Enable	Input Pulldov	F		n Disabled			
Invert/Invert Input			Input NOT Inverted				
Detect Level or Edge			Detect LEV	EL at Input			

Figure 6. Programming the PWR_ON Signal Input

The setup required for the PDOs and the PLBs controlling them for each supply is shown in Figures 7–9.

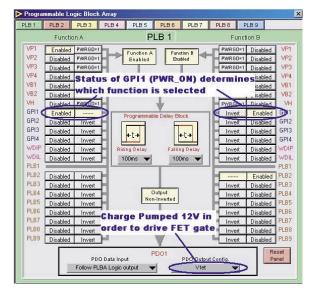


Figure 7. Programming Power-Up and Power-Down Sequence for 3.3 V Supply

PLB 1	PLB 2	PLB 3	PLB 4	PLB 5	PLB 6	PLB 7	PLB 8	PLB 9	
	Functio	on A		P	LB 2		Fund	tion B	
VP1	Disabled	PWRGD=1	hi . r	Function A	1	tion B	PWRGD=	Disabled	VP1
VP2	Disabled	PWRGD=1		Enabled		ibled	PWRGD=	Disabled	VP2
VP3	Disabled	PWRGD=1	H '				PWRGD=	Disabled	VP3
VP4	Enabled	PWRGD=1	Sour	ce vol	Itage	for the	PWRGD=	Disabled	VP4
VB1	Disabled	PWRGD=1		on +3.			PWRGD=	Disabled	VB1
VB2	Disabled	PWRGD=1	5	on	or at	.bbi3	PWRGD=	Disabled	VB2
VH	Disabled	PWRGD=1	н		*		PWRGD=	Disabled	VH
GPI1	Enabled			rogrammab	le Delav Bl	ock	Invert	Enabled	GPI1
GPI2	Disabled	Invert	HI F				Invert	Disabled	GPI2
GPI3	Disabled	Invert	HI	+t+		+t+	Invert	Disabled	GPI3
GPI4	Disabled	Invert	HI -				Invert	Disabled	GPI4
WDIP	Disabled	Invert	Risi	ng Delay	Fallir	ng Delay	Invert	Disabled	WDIF
WDIL	Disabled	Invert	F 1	Ooms 🔻	100	Dms 🔻	Invert	Disabled	WDI
PLB1	Enabled		34		-		Invert	Disabled	PLB1
PLB2									PLB2
PLB3	Disabled	Invert	н					Enabled	PLB3
PLB4	Disabled	Invert	н		Output I-Inverted		Invert	Disabled	PLB4
PLB5	Disabled	Invert	H .	_ Non	- moched		Invert	Disabled	PLB5
PLB6	Disabled	Invert	H		1.00	ic En	-vert	Disabled	PLB6
PLB7	Disabled	Invert	1				VEIL	Disabled	PLB7
PLB8	Disabled	Invert	11		for	+2.5V	vert	Disabled	PLB8
PLB9	Disabled	Invert	J-1		V	1	Invert	Disabled	PLBS
			O Data Inpu BA Logic c	it	002	PDO Outpu VP1 Strong I			eset anel

Figure 8. Programming Power-Up and Power-Down Sequence for 2.5 V Supply

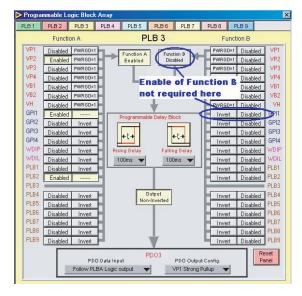


Figure 9. Programming Power-Up and Power-Down Sequence for 1.8 V Supply

For greater detail on how to program the ADM1060, refer to the ADM1060 Evaluation Tools note.

CONCLUSION

The ADM1060, combined with its software, is a very powerful sequencing management solution. The ADM1060 can be used to control the sequence of multiple supplies as they power up and power down. The key to programming a power-down sequence, which is independent of the powerup sequence, is to use Function B in the programmable logic block. A single signal can be used to switch control from Function A to Function B.

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