ANALOG DEVICES

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APPLICATION NOTE

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Build Precise S/H Amps for Fast 12-Bit ADCs

by John Sylvan

TODAY'S FAST, PRECISION IC OP AMPS AND FET SWITCHES BUILD THE LOW-COST SAMPLE-AND-HOLD AMPLIFIERS NEEDED BY SUB-1 μS, 12-BIT A-D CONVERTERS.

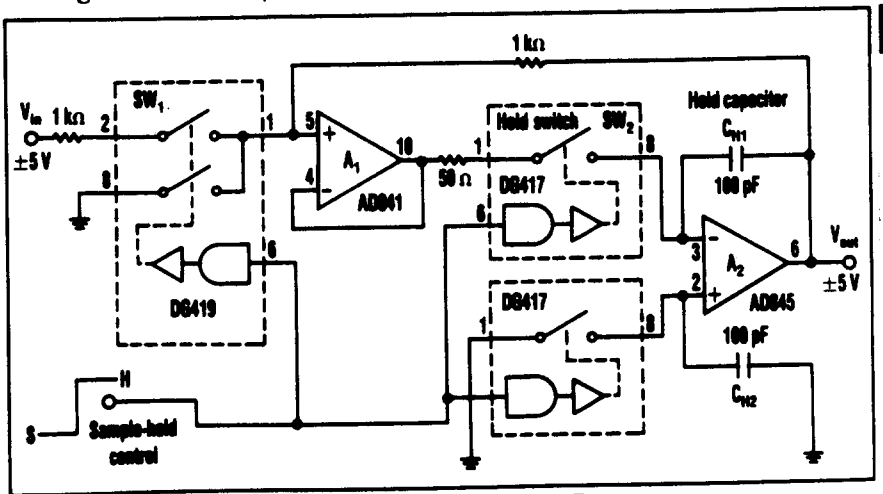
Discrete sample-and-hold amplifiers place heavy demands on operational amplifiers. The op amps must have excellent ac performance and promise good dc specifications. While sampling, they must track the input signal without distortion—a demand for wide, full-power bandwidth. When switching from the hold to sampling mode they should acquire the signal quickly. Here, high slew rates and fast settling times are vital. To ensure 12-bit precision over a wide operating temperature range, dc specifications such as offset voltage and offset voltage drift must be low.

Low input-bias current is a mandatory requirement for an op amp to be used in a s/h amplifier. High bias current leads to excessive droop rates. Therefore, s/h amplifier circuits require FET-input amplifiers. Typical FET designs have delivered settling times of 1 μs to 0.01%. Newer complementary bipolar (CB) processes now used to manufacture FET op amps combine low picoampere bias currents with 35 MHz unity-gain bandwidths and 12-bit accurate settling times under 130 ns. Moreover, they work from standard ±15-V supplies, easily accommodating wide dynamic-range signals.

S/h amplifier circuits will use one of several standard architectures: closed-loop or open-loop, and inverting or noninverting configurations. No matter what circuit type designers employ, they need to incorporate a high-speed amplifier to buffer the input signal and a switch to connect and disconnect the input signal from the hold capacitor. In addition, a FET-input amplifier is needed to buffer the voltage on the hold capacitor and drive an a-d converter.

FAST, SIMPLE SAMPLING

Three low-cost CMOS switches, two CB op amps, and a few resistors and capacitors are all that's needed to build a fast, simple, low-cost s/h amplifier from discrete IC op amps



1. A HIGH-SPEED SAMPLING AMPLIFIER to be used with a 12-bit, 1-ms, a-d converter can be built with a pair of high-speed CB op amps from Analog Devices, three CMOS IC analog switches, and a handful of passive parts.

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(Fig. 1). The circuit's full-power bandwidth is in excess of 250 kHz, acquiring a ±5-V input signal in approximately 1 μs—and it can be built for about $15.

Operating as a unity-gain voltage power, op amp A_1 buffers the input signal and supplies a minimum of 50 mA to charge the 100 pF hold capacitor, C_{H1}. Most older, fast, IC op amps don't have nearly this output current capacity—it's needed to charge a capacitor at high speed. In addition, many fast op amps would be unstable driving even 100 pF. This buffer, an AD841, is unity-gain stable and its full power bandwidth is close to 5 MHz.

Op amp A_2 does the sampling. It keeps the sampled charge on the hold capacitor and drives the next link in the system, for example the input of a high-speed, high-resolution a-d converter. A_2, an AD845 FET-input op amp, has an input bias current of just 500 pA, slews at 100 V/μs, and settles to within 0.01% of final value in under 250 ns for ±5-V output steps.

The circuit's overall design employs a noninverting, closed-loop configuration. Closed-loop designs typically trade off better accuracy and linearity for slower speed. In fast closed-loop designs, the input amplifier usually saturates when it's disconnected from the second stage. This occurs because the feedback loop is broken.

But this circuit overcomes that limitation by having a separate feedback path around A_1 and a double-pole, single-throw switch at the amplifier's input. When the circuit is in the "hold" mode, the noninverting input of A_1 switches to ground, driving the amplifier's output to ground as well. The drawback to the design, however, is that the s/h amplifier must return from zero potential after each hold time. This serves to lengthen the acquisition time.

CMOS Switches

To minimize acquisition time, the circuit's RC time constant, composed of (R_{in} + the on-resistance of the switch) × C_{H1}, should be minimal. This requires switches with low on-resistance. New generations of fast CMOS switches, such as the DG417 and DG419 from Siliconix, Santa Clara, Calif., offer on-resistances of 35 Ω and turn off in just 200 ns. Moreover, these high-speed ICs operate from ±15-V op amp supplies readily accommodating a wide-range of input signals.

The choice of switch is a trade-off between circuit complexity and performance. Complete CMOS switches operate over a wide voltage range, but they typically have higher charge injection than discrete FETs, which leads to larger pedestal errors. They also turn off and turn on slower than discrete FETs. However, CMOS switches operate directly from TTL or CMOS logic signals, eliminating the need for extra level-shifting circuitry.

ALTHOUGH REQUIRING MORE DESIGN WORK, A DISCRETE APPROACH MAY BE A COST-EFFECTIVE ALTERNATIVE TO BUYING AN EXPENSIVE HYBRID.

Pedestal-error is a major error source in high-speed s/h amplifier circuits, especially as the value of the hold capacitor is reduced to lower acquisition time. When the hold-switch opens, it injects the charge held on its gate-to-source parasitic capacitance onto the hold capacitor changing the op amp's output voltage. The change in output voltage, ΔV_O, seen by the amplifier equals:

Equation 1: $\Delta V_O = \Delta Q / C_H$

where Q is the charge in picocoulombs and C_H is the value of the hold capacitor, typically in picofarads. The effects of charge injection are significant. For example, injecting just 5 pC of charge into a hold capacitance of 86 pF causes a change in output voltage of 58 mV—a 24 LSB error for a 12-bit a-d converter with a ±5-V full-scale input range.

To reduce pedestal error, a s/h amplifier can employ a differential mode of operation *(Fig. 1 again)*. When the circuit switches from sampling or tracking the input signal to the hold mode, a second hold switch (SW_2) injects an equal charge onto C_{H2}, balancing the effects of charge injection on C_{H1}. As a result, the pedestal error will be zero if the switches and capacitors exactly match and if the amplifier has high common-mode rejection. The pedestal error is seen as a common-mode error by the op amp and is rejected.

Driving a virtual ground with the hold-switch (that is with the storage capacitor C_{H1} in the feedback loop of an op amp), also lowers the s/h amplifier's pedestal errors. The charge injected into the op amp's summing node—a virtual ground—becomes constant regardless of the input voltage. The pedestal now also becomes a constant that can be trimmed to zero with a potentiometer. Alternatively, in a system autozero mode, the pedestal can be trimmed with a d-a converter. When used in this way, essentially as an integrator, the fast op amp must be stable at a noise-gain of unity.

Feedthrough Errors

Feedthrough of the input signal to the output when in the "hold" mode also haunts s/h amplifiers. Typically, feedthrough is a function of the input signal frequency and its amplitude. If the amplitude is less than 1/2 LSB, feedthrough effects won't show up in the spectrum of the digitized signal because 1/2 LSB is below the quantization noise floor. Feedthrough errors above 1/2 LSB cause erroneous codes, increased total harmonic distortion (THD), and lower signal-to-noise ratios (SNR).

Feedthrough error is determined by the equation:

Equation 2: $\Delta V_O = C_{DS}/C_H \Delta V_{in}$

where C_{DS} is the source-to-drain capacitance of the switch, and V_{in} is the peak-to-peak input voltage.

An obvious method to cut feedthrough is by reducing the peak-to-peak voltage seen by the hold switch. "Turning off" the input buffer amplifier by disconnecting the ac signal from the s/h amplifier's input achieves this with the help of SW_1, a single-pole, double-throw switch. It connects the noninverting terminal of op amp A_1 to ground during the hold mode and to the input signal during the sample mode. Therefore, SW_2 no longer sees a high-frequency ±5-V signal during the hold mode, but rather a "fixed" dc potential, which in this case is ground. As a result, feedthrough is virtually reduced to zero.

Switching the noninverting terminal to ground offers an added benefit. It drops the droop rate. Since the potential across the switch is zero volts (both sides of the switch see a virtual ground), there is virtually no leakage current through the open switch. The droop rate is dependent only on the input offset current of A_2, 20 nA maximum, and charge leaking through the capacitor.

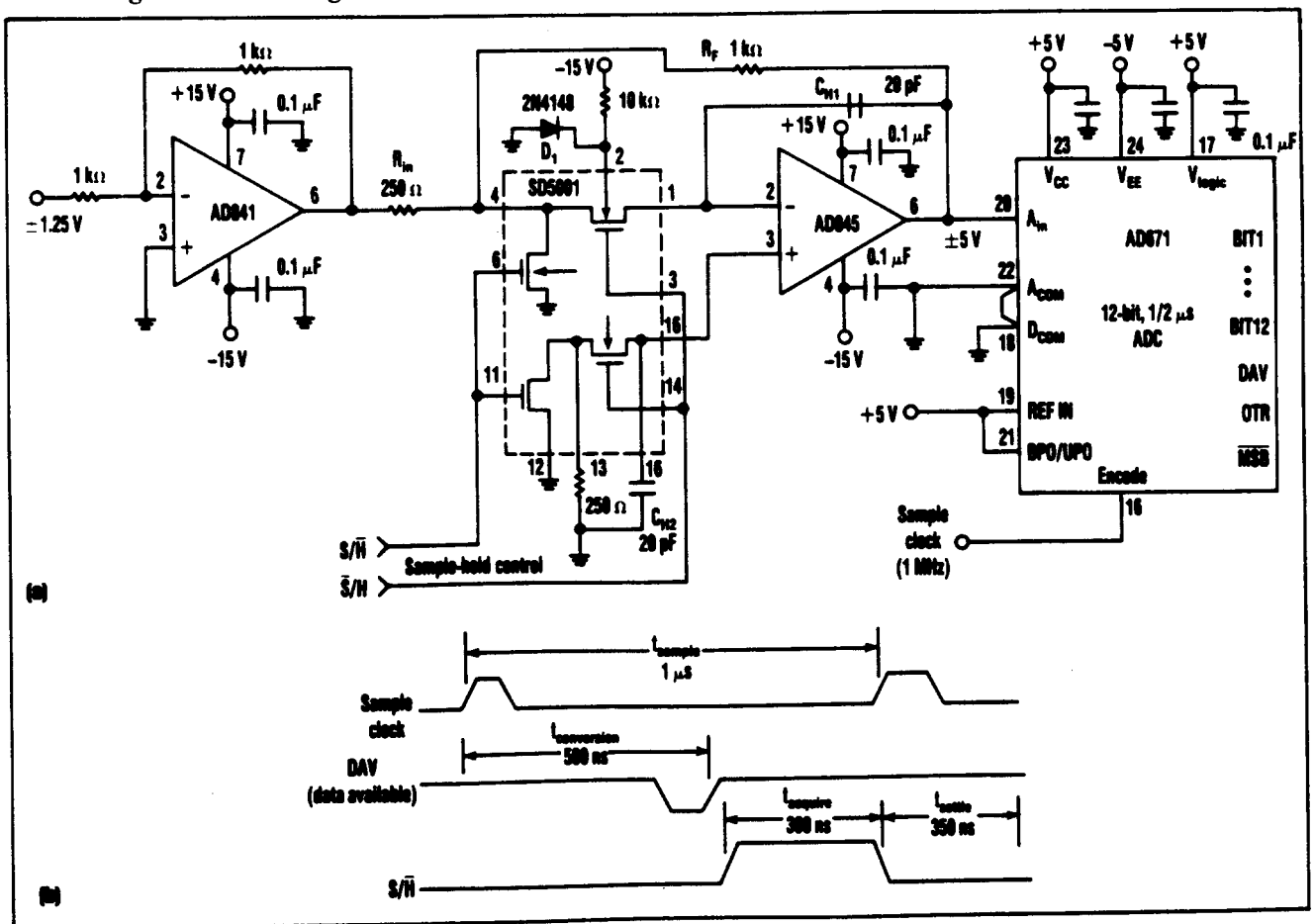
Low-Cost, 1-MHz Sampler

Conversion rates of the latest generation of high-speed monolithic a-d converters have reached 2 MHz. Though hybrid s/h amplifiers can deliver the fast acquisition times demanded by these converters, they usually cost more than the a-d converter itself. Although requiring more design work, a discrete approach may be a cost-effective alternative to buying an expensive hybrid.

Another discrete approach employs two high-speed CB op amps, a DMOS quad switch, and a few passive components *(Fig. 2a)*. The circuit works with a high-speed a-d converter chip, such as the AD671, a monolithic 12-bit, 500 ns converter, and delivers a throughput rate of 1 Msample/s.

Even though a high input impedance would simplify signal conditioning, the s/h amplifier's circuit trades off a 2000-Ω input impedance for the lower distortion of an inverting configuration. Noninverting designs are subject to common-mode errors, pedestal errors that are a direct function of input signal level, and nonlinearities created by the switch. All three of these errors can lead to greater total harmonic distortion from the s/h amplifier.

High-speed acquisition is facilitated by the fast DMOS quad switch—



2. FOR THE ULTIMATE in speed and accuracy while sampling signals for a 12-bit, 1/2 μs a-d converter (for example, the AD671), it's often best to build a s/h amplifier with discrete CMOS transistor analog switches, such as Signetics SD5001 (a). Moreover, the s/h amplifier must be given time to acquire the signal and settle (b).

the Siliconix SD5001 turns on in just 1 ns. Biasing its body one diode-drop below ground with the 2N4148 diode produces a lower switch on-resistance for a given gate-to-source volt-

The switch also boasts a very .ll gate-to-drain capacitance of 1.6 pF, which further helps decrease charge injected onto the hold capacitor. The DMOS switches' control inputs require at least CMOS logic-level complementary voltages to turn them on. However, higher control levels for the gates of the switches will improve performance by lowering the on-resistance of the switches.

Because the AD845 works in a differential mode, droop rate is a function of input "offset" current rather than input "bias" current. The AD845 is specified to have a maximum 20 nA of input offset current. Using the equation:

Equation 3: $\Delta V/\Delta t = i_{offset}/C_{H1}$

where C_{H1} is the value of the hold capacitor, will designate the droop rate.

The voltage droop will be a maximum 1 mV/μs and is typically 1.25 μV/μs. Even if this calculation doesn't factor in the leakage current through the switch; the gate, source, and drain of the switch are all close to 0 V, creating a low differential voltage across it and negligible leakage current.

Minimizing Feedthrough

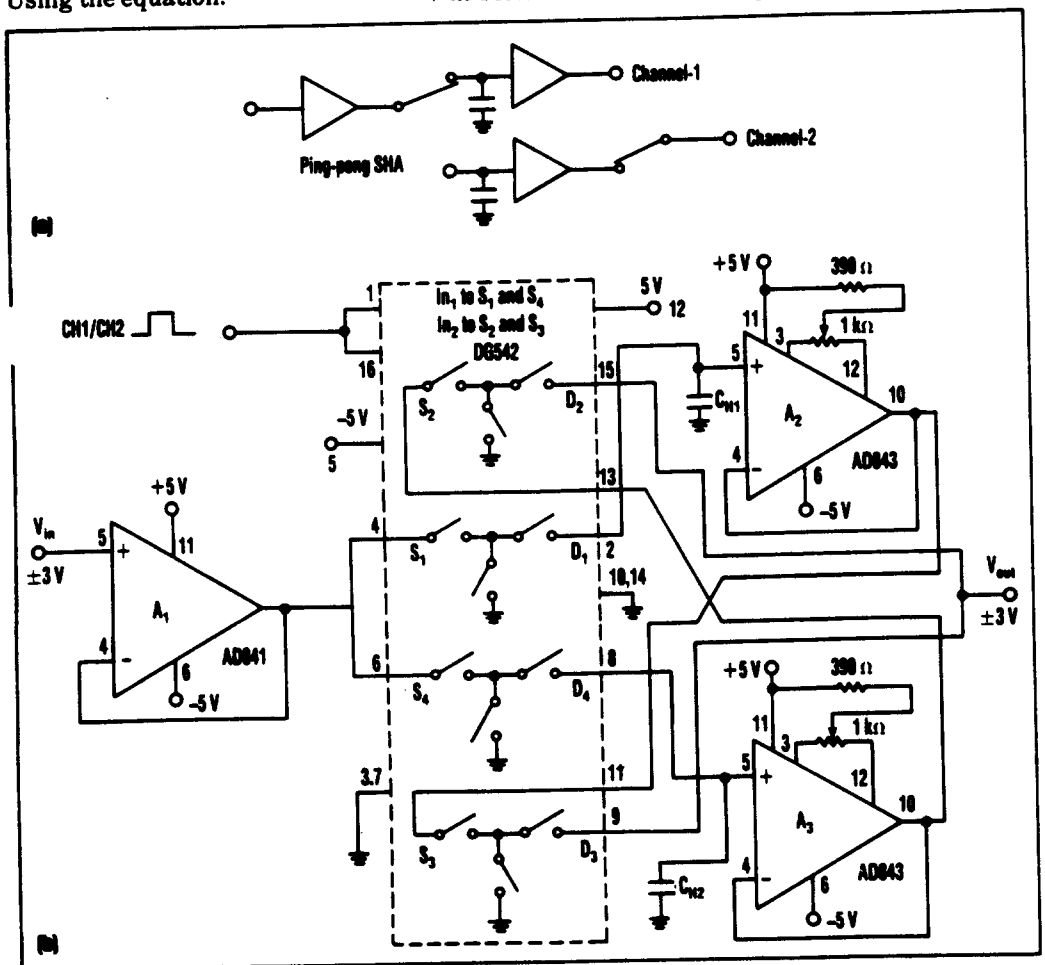
To minimize feedthrough, the fast s/h amplifier uses a T-switch configuration. When the circuit is in the hold mode, the input signal is shunted to ground through one of the SD5001's four switches. The switch in series with the 250-Ω input resistor acts as a voltage divider. With a typical on-resistance of 50 Ω and a ±1.25-V input signal, the maximum feedthrough voltage seen at the source terminal of the "hold" switch is 200 mVpk-pk. The high impedance of the open switch further reduces signal feedthrough more than 60 dB.

Because resistors R_F and R_{in} determine the gain of the s/h amplifier, designers can base their value on the maximum input signal and the full-scale input range of the a-d converter it's feeding. The values shown are chosen for a gain of –4, which increases the input amplitude from ±1.25 V to the ±5-V range of the AD671.

Even though the AD671 can perform a conversion in less than 1 μs, it's necessary to allow the s/h amplifier time to acquire the signal and then settle. However, the timing of the AD671 is not conventional. Its multistep conversion architecture doesn't require the input signal to settle to 12-bit accuracy until 150 ns of its conversion cycle has passed *(Fig. 2b)*.

A ping-pong s/h amplifier architecture improves throughput by employing two sampling circuits. While one is sampling or acquiring a signal, the other is in hold driving the a-d converter or some other load *(Fig. 3a)*. It takes just three high-speed IC op amps and a high-speed IC switch to build a ping-pong configuration.

The AD841 op amp A_1 follows the input signal. The DG542 switch, a dual wideband "T" circuit, alternately connects the input buffer A_1 to one of the two output op amps and its storage capacitor. At the same time, the switch also connects the amplifi-



3. MAXIMUM THROUGHPUT RATE is achieved with a ping-pong s/h amplifier, where one channel samples the input while the other is in hold mode (a). Using the DG542 DMOS video switch, which employs T-type switches, minimizes feedthrough and crosstalk (b).

er's output in hold mode to the circuit's output V_{out}. For example, when pins 1 and 16 of the switch are at logic high, A_2 is tracking the input signal, and its output is disconnected from V_{out}. A_3 and its storage capacitor hold an analog voltage and it's output is connected to V_{out}. When the sample and hold command on pins 1 and 16 of the switch goes to logic low, the two output amplifiers switch jobs.

The ping-pong technique offers more than just greater throughput rates to high-speed s/h amplifier applications. For example, the technique makes it possible for designers to increase the value of the hold capacitors. Because the acquisition cycle occurs in parallel with the hold cycle, the RC time constant resulting from the finite on-resistance of the switch and the hold capacitance no longer limits throughput rate. If the acquisition time is less than the required hold-time for the conversion, then the slew rate and settling time of the output amplifier limit throughput. The two AD843 FET input op amps slew at 250 V/μs and settle to within ±.01% of final value in 130 ns for ±10-V steps.

The choice of the appropriate switch is critical in this type of design. The DG542 utilizes "T" switching techniques on each channel for exceptionally low crosstalk and high isolation.

The device further improves these specifications by locating ground pins between the signal pins. With an input frequency of 5 MHz, crosstalk and isolation are –85 dB and –75 dB, respectively.

The switch is limited to a maximum of –5 V on its negative supply input, making bipolar operation difficult. All three amplifiers should operate from the same –5-V rail as the switch to minimize potential latch-up. This limited supply range will restrict the amplitude of the inputs to video-level signals of ±3 V. If a wider range is needed to maximize the full-scale range of an a-d converter, gain can be taken at the two output amplifiers by operating them as followers with gain. However, they'll have to be run from ±12-V supply rails.

Because the input to the a-d converter consists of the alternating "held" values from the two amplifiers, the mismatch between their offset voltages will show up as nonlinearities and, therefore, distortion in the output signal. This demands that the amplifiers offer excellent ac performance and good dc precision. The AD843's maximum offset voltage is 1 mV, offset voltage drift is 10 μV/°C, and open-loop gain is 94 dB.

However, the AD843's balance pins accommodate offset trims. Users can ground the input and adjust the difference between their outputs through zero. The output is connected to a high gain oscilloscope and the S/H control input is toggled. The square wave created by the difference in offset voltages is adjusted to zero.

If offset voltage drift over temperature becomes a problem, especially with FET-input amplifiers, designers can employ an autocalibration circuit using two d-a converters. A "known" reference voltage, or ground, can be connected to the input op amp and the offset voltage adjusted to zero by manipulating the digital codes of two 8-bit d-a converters connected to the wipers of the op amps' trim-pins.

Choose The Right Caps

When selecting the appropriate types of capacitors for building a s/h amplifier, designers should employ devices with low dielectric absorption and low temperature coefficients (TCs). Silvered-mica capacitors exhibit low (0 to 100 ppm/°C) TCs and operate in excess of 200°C. Users should test the capacitors to ensure that their actual value matches their marked value. Not all manufacturers fully test all of their capacitors for absolute tolerance.

Aperture delay and aperture uncertainty, or jitter, represent two additional vital s/h amplifier specifications. Aperture delay produces an error that's determined by the equation:

Equation 4: $E_a = T_a(dV/dt)$

where E_a is the aperture error in volts, T_a is the aperture delay and dV/dt is the slew rate of the input signal. This error is a result of the finite time it takes a switch to open, and the effect of "averaging" the input signal over the closing-to-opening of the switch. However, as long as the switch opens in a repeatable fashion, the aperture time can be viewed as a phase shift in the input signal, not as an error source in a single-channel system. In fact, it can be calibrated out.

Circuit designers must guard against variable aperture delays or "aperture jitter." The maximum bandwidth of a s/h amplifier with a given aperture jitter (t_a) is determined by the equation:

Equation 5: $f_{MAX} = 1/(2\pi t_a)(2^{(n+1)})$

where n in the expression $2^{(n+1)}$ is the resolution of the a-d converter following the s/h amplifier. For a 12-bit converter and 10-ps aperture jitter, the maximum bandwidth is approximately 2 MHz. This equation illustrates that the s/h amplifier must maintain low jitter to be used with high-speed, high-resolution a-d converters.

Aperture jitter can arise from phase modulation in the sampling clock from either wideband random noise, power-line frequency noise, or digital noise due to poor grounding. Careful board layout can reduce these sources. The pc-board trace between the source of the s/h command and s/h amplifier's circuit should be as short as possible to minimize the effects of parasitic circuit inductance, resistance, and capacitance. Moreover, long runs of digital designers should make sure that control lines are not run parallel to any analog signal paths.□