ANALOG DEVICES

AN-142
APPLICATION NOTE

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Voltage Adjustment Applications of the DAC-8800 TrimDAC®
An Octal, 8-Bit D/A Converter

by Joe Buxton

The DAC-8800, a monolithic octal 8-bit digital-to-analog converter, is a digitally-controlled voltage adjustment device. The DAC's design makes it ideal for replacing trimming potentiometers in many applications. Not only does it replace potentiometers, but the DAC has many advantages over them, such as solid state reliability, very low drift over temperature and time, elimination of shifts due to vibrations, and automating the adjustment process. During manufacture of complex electrical systems, potentiometers must be manually adjusted taking considerable time and cost for labor, or expensive robotic systems must be developed for the same purpose. However, the DAC-8800 can automate the system's voltage adjustments so that a computer can now control the calibration.

This application note first describes the basic architecture and operating modes of the DAC-8800, including the reference input range limits, the load that the DAC places on the references, single supply operation, and serial interfacing. The last half of this note shows many basic circuits for using the DAC in a wide variety of applications, such as two wire interfaces and stand-alone operation for systems not based on digital controllers. Also included are techniques for adjusting the offset of operational amplifiers; using two DAC outputs together for coarse and fine control of a voltage; digitally changing the gain of a voltage-controlled amplifier; and trimming voltage references.

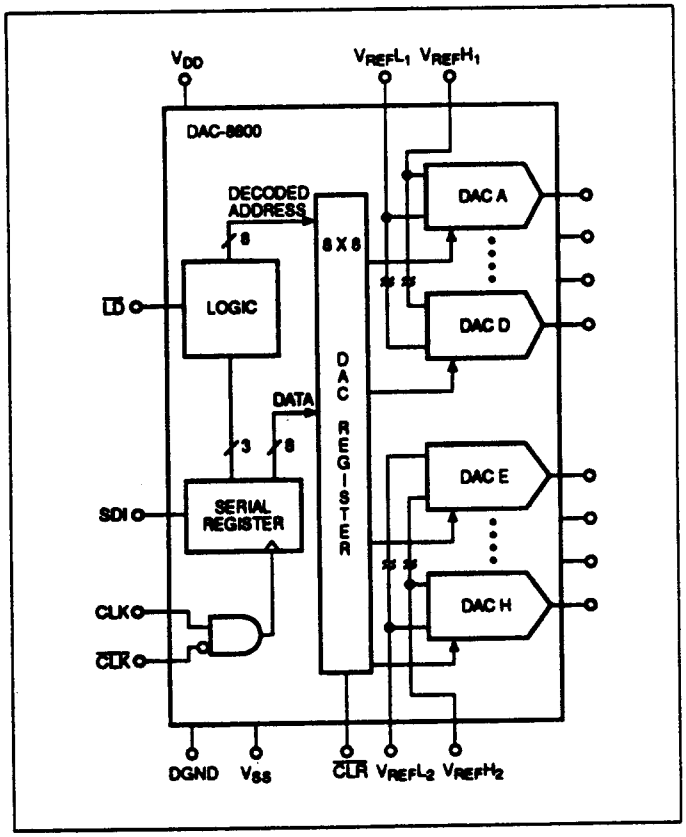

FIGURE 1: *DAC-8800 Block Diagram*

BASIC ARCHITECTURE

As the functional diagram shows in Figure 1, the DAC-8800 has eight individual DACs divided into two groups of four, each group having its own high and low reference inputs. Each DAC's output is independently controlled by a serial interface through which the 8-bit data word and 3-bit address are loaded.

Each of the DACs contains an R-2R ladder connected between the high and low reference inputs as shown in Figure 2. The output voltage is set by the position of the switches according to the formula below:

$$V_{OUT}(D) = D \times (V_{REF}H - V_{REF}L)/256 + V_{REF}L$$

where D is the digital code.

As this equation shows, the output can vary from $V_{REF}L$ to $V_{REF}H$ in 256 steps. It is significant that, while the output voltage can vary over this range, the DAC-8800's output impedance is always equal to a constant R_{OUT}, the characteristic resistance of the ladder. R_{OUT} is typically 12kΩ but can vary between 8kΩ and 16kΩ from device to device. The DAC's accuracy depends not on the absolute value of the ladder resistors but rather on the relative resistor matching. Thus, variations in output impedance do not

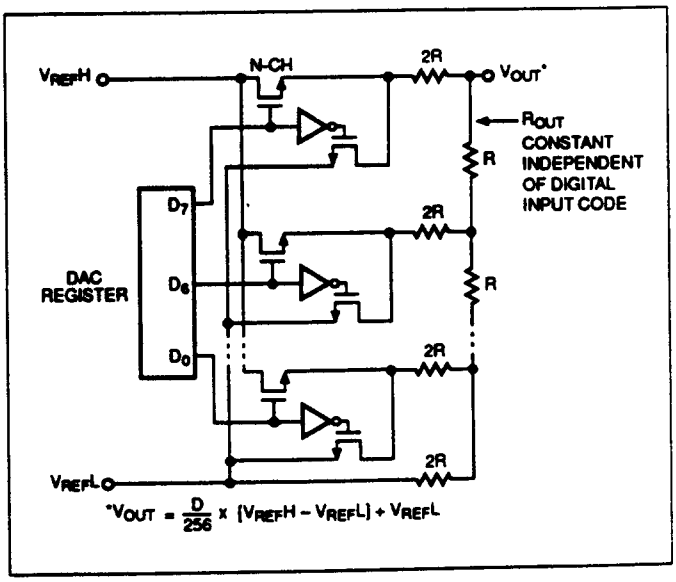

FIGURE 2: *DAC-8800 R-2R Ladder Network*

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iffect the linearity of the DAC. To easily understand the DAC, each output can be thought of as a Thevenin equivalent circuit of a voltage source in series with R_{OUT} as in Figure 3, where R_{OUT} is 12kΩ. The digital code then varies the voltage source between /--eL and $V_{REF}H$.

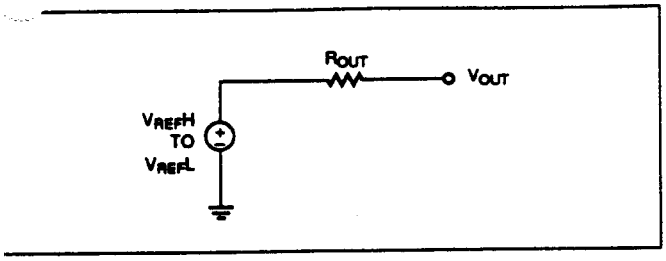

FIGURE 3: *Thevenin equivalent of each DAC output. R_{OUT} is typically 12kΩ.*

REFERENCE INPUT LIMITS

The switches in the R-2R ladder are N-channel enhancement MOSFETs with extremely low ON resistance. To ensure the DAC's linearity, the MOSFETs' gate-to-source voltage (V_{GS}) needs to be greater than the switches' intrinsic threshold voltage, which for the DAC-8800 is 2.5V. When the voltage falls below 2.5V the MOSFETs' ON resistance increases, which causes resistance mismatching in the R-2R ladder. Any mismatching degrades the precise R-2R ratios and thus decreases the linearity of the DAC.

In the DAC-8800, the gate-to-source voltage is equivalent to the voltage difference between V_{DD} and $V_{REF}H$, respectively. Figure 2 shows that $V_{REF}H$ is connected to the drain of the MOSFET switches, and, when the switches are on, the drain voltage is basically equivalent to the source voltage. The gate voltage is ·n by CMOS logic, and when the switch is on, the logic con- the gate to V_{DD}. Thus, $V_{REF}H$ must be at least 2.5V below V_{DD}, as shown in Figure 3 of the DAC-8800's data sheet. However, to guarantee the data sheet error specifications over –55°C to +125°C, the gate-to-source voltage needs to be at least 4V. There is no similar limitation between the reference input and the negative supply, V_{SS}. Thus, the reference inputs can go to V_{SS}. An important note: because of internal protection diodes in the DAC, $V_{REF}L$ should not be allowed to go higher than $V_{REF}H$. Forward biasing these diodes allows large currents to flow between the two references, potentially resulting in permanent damage to the DAC-8800.

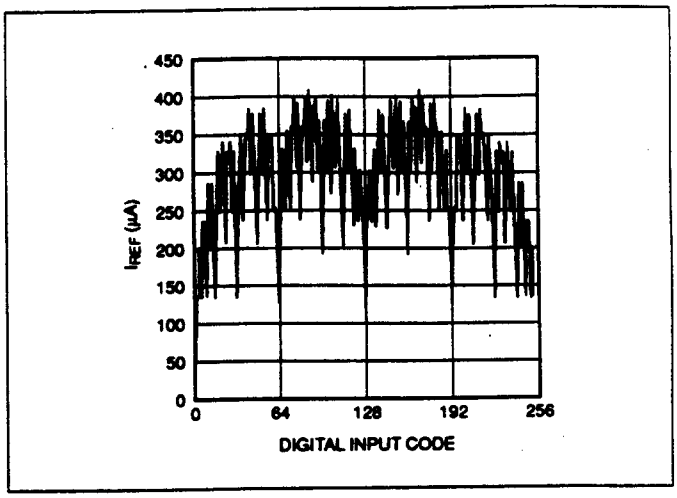

FIGURE 4: *$I_{REF}H$ variation versus digital code. One of four DACs connected to $V_{REF}H$. The other 3 DACs are loaded with zero code.*

REFERENCE INPUT CURRENT CHANGES WITH DIGITAL CODE

As the digital code changes, the resistance looking into the reference input changes significantly. Figure 4 shows the current demand into the $V_{REF}H$ pin as a function of the digital code for one of the four DACs referenced from that pin. This graph was generated with the following conditions: V_{DD} = +12V, V_{SS} = 0V, $V_{REF}H$ = +5V, and $V_{REF}L$ = 0V. As can be seen, the load on the reference varies from zero to 400µA. With all four DACs operating, the load current can go up to a maximum of 1.6mA. It is important to keep in mind that the current changes in abrupt steps. Thus, in applications where speed is important, any device driving the reference pin must be capable of handling these step current changes. A fast recovery op amp (such as the OP-42) or reference is recommended.

THE DAC-8800 CANNOT BE USED AS A VARIABLE RESISTOR

At first glance the DAC-8800 might appear to be ideal for use as a variable resistor from its output to $V_{REF}L$, where $V_{REF}L$ is tied to ground and $V_{REF}H$ left floating. However, its internal structure was not designed for this. The reason is two fold. First, the resistance from the DAC's output to $V_{REF}L$ does not vary linearly with

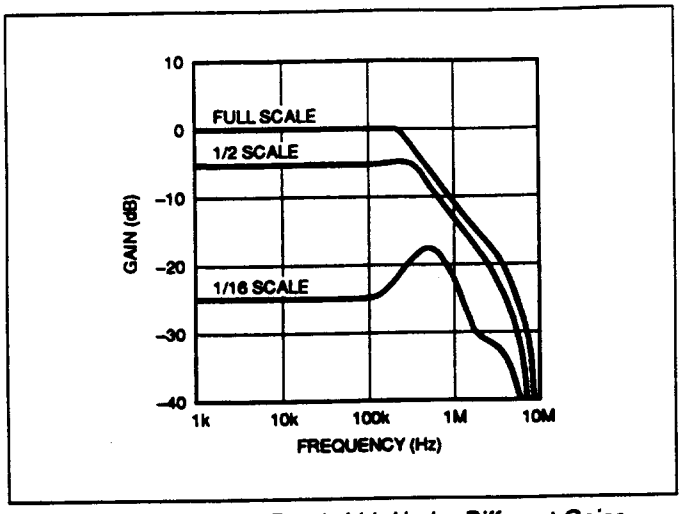

FIGURE 5: *DAC-8800 Bandwidth Under Different Gains*

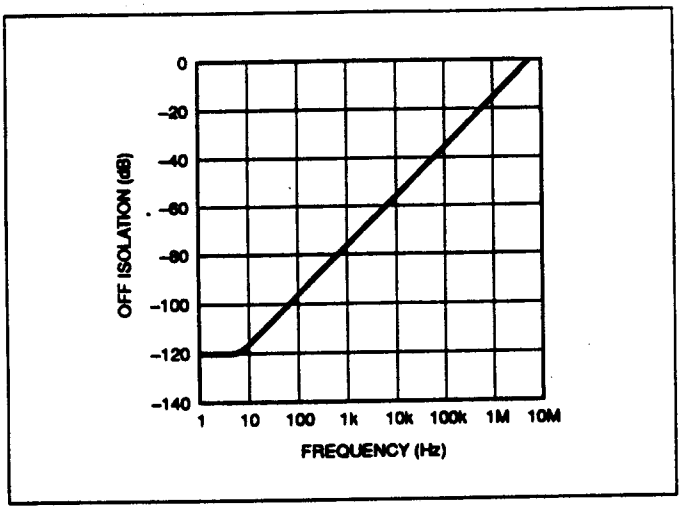

FIGURE 6: *DAC-8800 OFF Isolation*

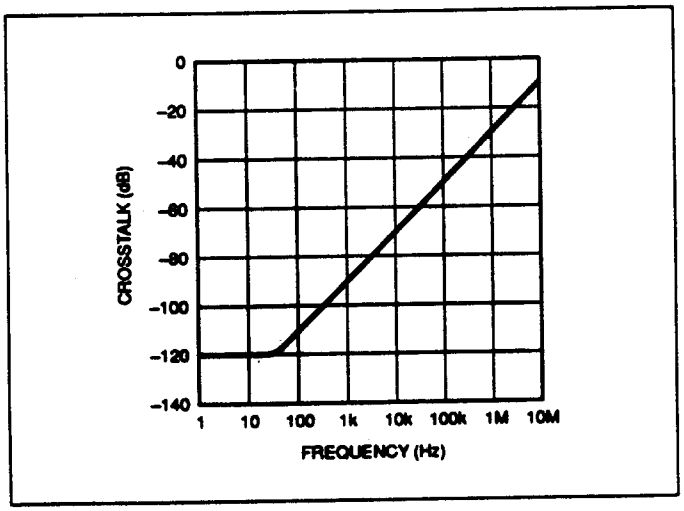

FIGURE 7: *DAC-8800 Crosstalk*

the digital code. Rather, it changes erratically, similar to the way the reference current changes in Figure 4. These seemingly random changes are due to various switches connected to $V_{REF}H$ turning on in binary fashion rather than sequentially and creating alternate current paths from the output to $V_{REF}L$.

Second, the NMOS switches are not bi-directional. In this variable resistor configuration, the switches connected to $V_{REF}H$ would actually have current flowing in reverse direction from the source to the drain. They maintain their low ON resistance only when current is flowing normally from the $V_{REF}H$ side (the drain) towards the output (the source). In backwards operation the source voltage causes changes in the ON resistance. Thus, any change of the voltage on the DAC's output will change the ON resistance and ultimately change the resistance to ground, even at the same digital code. Obviously, the DAC-8800 was designed to work as a voltage attenuator, and not as a variable resistor.

AC MULTIPLYING MODE OPERATION

The DAC-8800 is designed primarily as a DC adjustment device. However, it can also be used in multiplying mode by applying an AC signal to the reference input. In such applications, bandwidth, off-isolation, and crosstalk are important to the circuit's performance. The bandwidth of the DAC-8800 is limited by the ladder resistance and the internal capacitance, which are both specified in the data sheet. The typical resistance of 12kΩ, combined with the reference capacitance of 75pF, limits the bandwidth to 177kHz. Figure 5 shows actual network analyzer measurements of the –3dB bandwidth, which for this particular part occurs at 360kHz. The fact that the measured bandwidth is twice the typical points out how the bandwidth can vary due to varying capacitance and resistance from device to device. The worst case bandwidth is approximately 100kHz based on worst case resistor and capacitor values of 16kΩ and 100pF, respectively. Remember, as mentioned in the reference input limits section, $V_{REF}H$ cannot go below $V_{REF}L$. Any AC signal into $V_{REF}H$ must be biased to avoid this condition.

The off isolation of the DAC-8800, shown in Figure 6, was measured using an AC signal for $V_{REF}H$ and measuring an associated DAC output with all the bits off. The off isolation reveals how much of the input signal will feed through to the output. An interesting correlation can be made between this graph and the bandwidth graph of Figure 5, for the 1/16 scale measurement. The 1/16 scale shows a 10dB rise in the gain above 100kHz. This is actually due to the capacitive feedthrough of the DAC-8800.

The crosstalk versus frequency graph in Figure 7 was measured as the crosstalk from one set of four DACs to the other set of four DACs in the package. In other words, DACs A through D were set to full scale, and a frequency dependent signal was injected into their $V_{REF}H$ input. The crosstalk was then measured on the outputs of DACs E through H. The graph shows DC crosstalk of –120dB rising up to –50dB at 100kHz, revealing excellent performance for DC and low frequency AC signals.

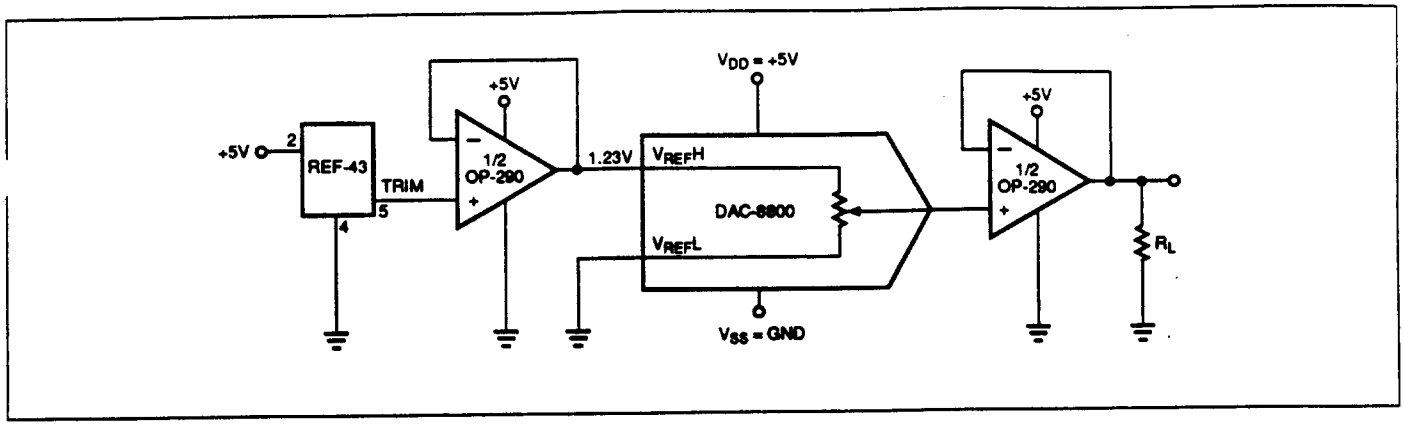

FIGURE 8: *DAC-8800 Single +5V Operation*

OUTPUT NOISE

The DAC-8800 exhibits basic broadband white noise of typically 18nV/$\sqrt{Hz}$. Its dominant noise source is the resistor ladder. Thus, the noise does not exhibit any measurable 1/f noise.

SINGLE +5V SUPPLY OPERATION OF THE DAC-8800

The DAC-8800 is ideal for single supply applications because its output range includes ground. In fact, the DAC-8800 can work well with a single +5V only. Even with this low of a supply voltage, $V_{REF}H$ can be connected to a 1.23V bandgap reference (Figure 8). Although the 1.23V bandgap reference violates the 4V of headroom requirement, the DAC is still within ±1/2 LSB of total unadjusted error. The 4V below the positive supply limit was set with a safety margin of about 0.5V to account for operation over the full operating temperature range.

The 1.23V bandgap reference voltage is derived from the TRIM pin of a precision 2.5V reference device, the REF-43. The buffer amplifier is needed because the TRIM pin's impedance is 50kΩ. The DAC-8800's reference inputs characteristically range from 12kΩ to 40kΩ depending on the digital code, which would load the trim pin excessively. The OP-290's low offset voltage of 75µV and low temperature drift characteristics maintain the reference's accuracy. The OP-290 also has the ability for its output to operate to ground with the addition of a load resistor; 10kΩ works well. The output amplifier is needed to buffer the DAC-8800's high output impedance when the output is connected to a low impedance load.

SERIAL INTERFACING

The digital control of the DAC-8800 is a standard three-wire serial interface with clock (CLK), load ($\overline{LD}$), and serial data input (SDI) (Figure 9). Additionally, an inverted $\overline{CLK}$ input pin is available for negative edge triggered data loading. Either CLK or $\overline{CLK}$ can also be used as a chip select pin. When loading data, 3 address bits are loaded, MSB first, followed by 8 bits of data, again MSB first. Thus 11 bits in all are loaded through the SDI pin to control each DAC. The DAC-8800 can run on a clock as fast as 6.6MHz making it possible to load all eight DACs in as little as 14 microseconds. Furthermore, the DAC-8800 maintains TTL compatibility for positive power supply voltages greater than or equal to +5V.

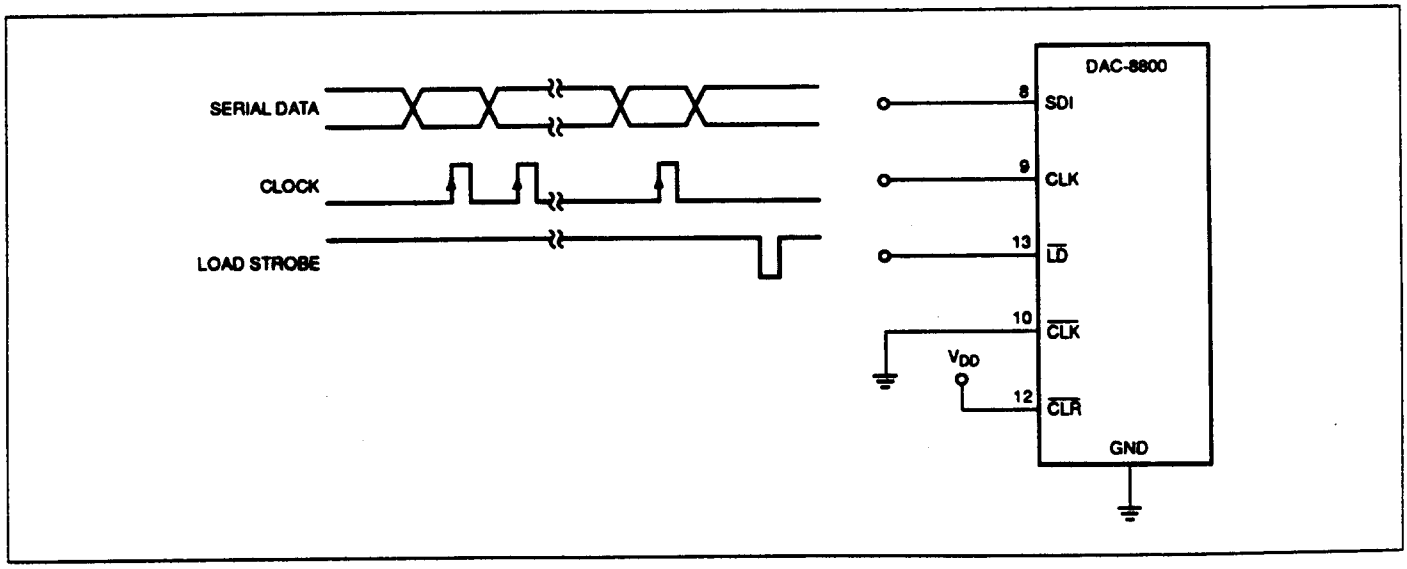

FIGURE 9: *DAC-8800 Serial Interfacing*

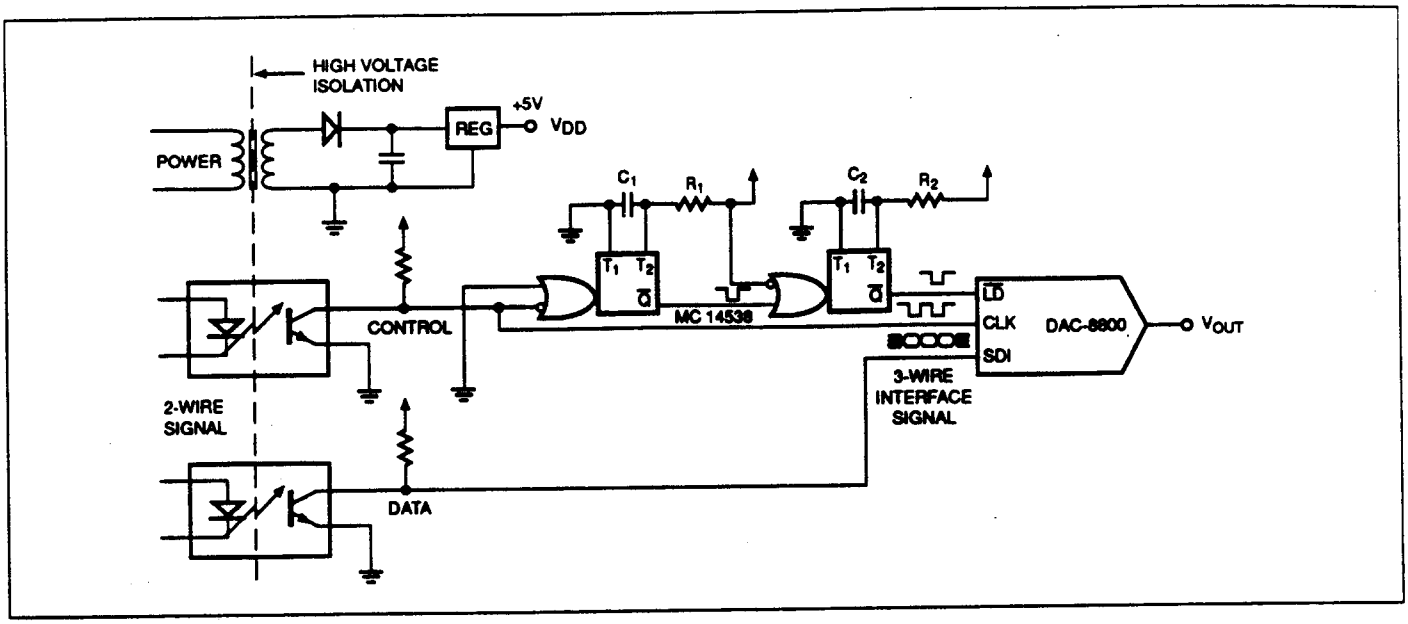

FIGURE 10: *Isolated Two-Wire Serial Interface for the DAC-8800*

TWO WIRE INTERFACES FOR PROCESS ENVIRONMENTS

High voltage isolation using opto-couplers is often necessary for serial interfaces found in process control applications. In these and other applications where minimizing the number of data lines is desirable, two-wire signal interfaces can be used (Figure 10). This simple circuit translates the two-wire interface into the three data lines required to load the DAC-8800. The $\overline{\text{LOAD}}$ signal is generated using two retriggerable one-shots. The first one-shot's timeout should be set longer than the clock period. Each succeeding clock pulse will retrigger the one-shot until all 11 bits are loaded into the DAC. Then the clock must pause long enough to allow the one-shot to time out. When the first one-shot's output goes low, it triggers the second one-shot, which produces the $\overline{\text{LOAD}}$ pulse, and finishes the loading cycle.

There are some common pitfalls when using one-shots. For example, the timeout set by the external resistor and capacitor can vary over temperature and from part to part. Even more significant is the variation due to resistor and capacitor tolerances. A typical capacitor can vary by ±10% which will cause an equivalent ±10% variation in the timing of the one-shot. To avoid the problems of one-shots, a second method using a counter is recommended (Figure 11a). The counter keeps track of the number of clock cycles and, when all the data has been input to the DAC, the external logic creates the $\overline{\text{LOAD}}$ pulse.

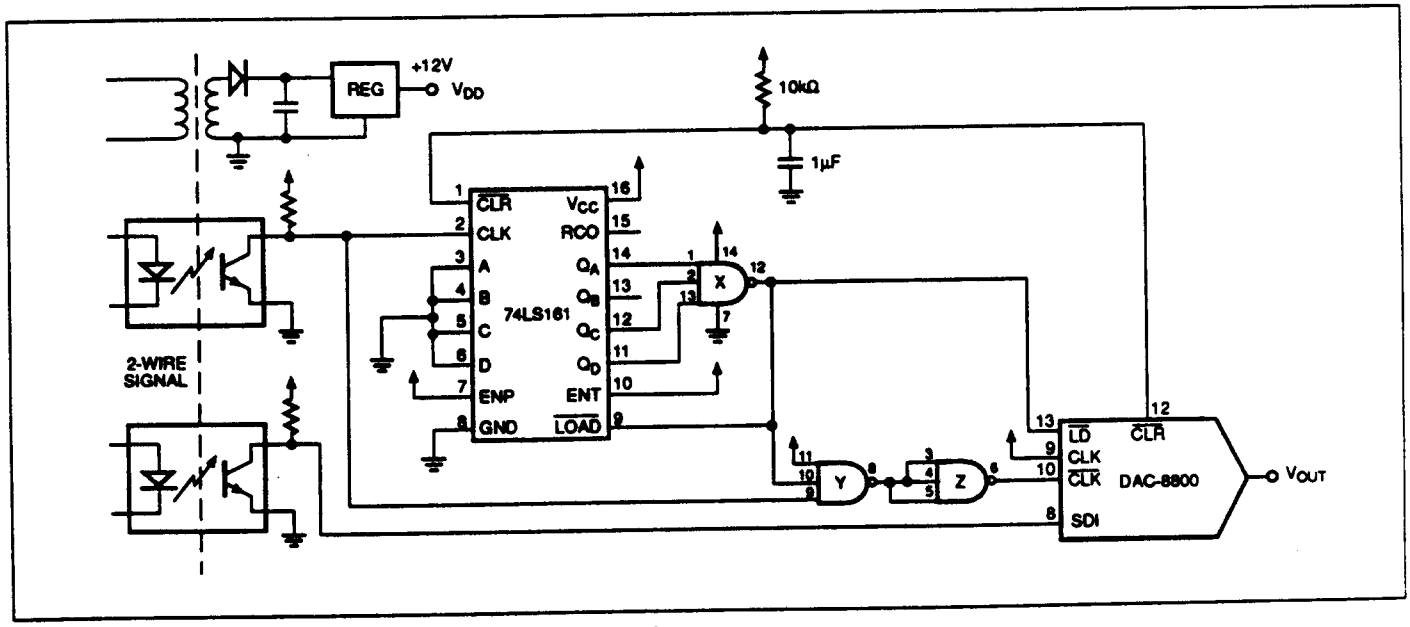

FIGURE 11a: *Isolated Two-Wire Serial Interface Using a Counter*

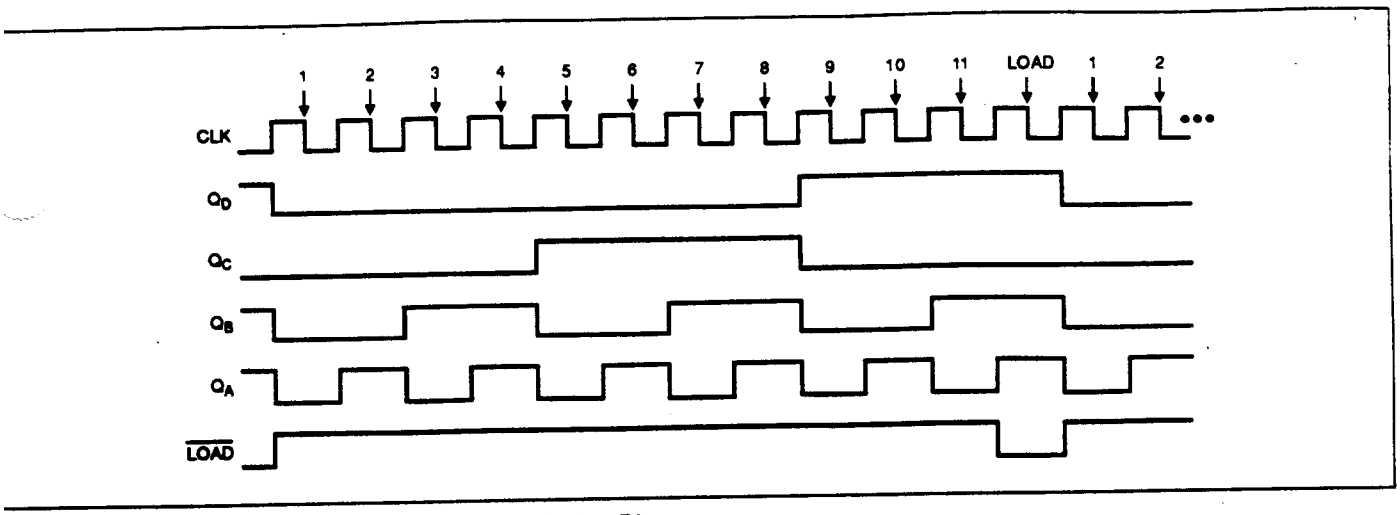

FIGURE 11b: *Isolated Two-wire Serial Interface Timing Diagram*

Referring to the timing diagram (see Figure 11b), the counter is incremented on every rising edge of the clock. Additionally, the data is loaded into the DAC-8800 on the falling edge of the clock by using the $\overline{CLK}$ input instead of the CLK input. The reason for using the $\overline{CLK}$ input becomes apparent after considering the $\overline{LOAD}$ pulse. The timing diagram shows that after the eleventh bit has been clocked, the output of the counter is binary 1010. On the following rising CLK edge the output of the counter changes to binary 1011, upon which NAND gate 'X' goes low to generate the $\overline{LOAD}$ pulse. The $\overline{LOAD}$ signal is connected to both the DAC's $\overline{LD}$ and the counter's $\overline{LOAD}$ pins. Since the counter has a synchronous clear, the $\overline{LOAD}$ pulse remains low until the next CLK pulse. NAND gates 'Y' and 'Z' prevent the twelfth falling CLK edge (labelled 'LOAD' in the timing diagram) from clocking the DAC, which would load false data into the DAC. Using the $\overline{CLK}$ input allows sufficient time from the CLK edge to the $\overline{LOAD}$ edge, and from the $\overline{LOAD}$ edge to the next CLK pulse, to satisfy the timing requirements for loading the DAC-8800.

After loading one address of the DAC, the entire process can be repeated to load another address. If the loading is complete then the CLK must stop after the twelfth pulse of the final load. The $\overline{CLK}$ input will be pulled high and the counter reset to zero. The timing requirements of the system are the same as for the DAC alone, and can be found in the DAC-8800's data sheet. Another feature of this circuit is the R and C on the CLR pins of both the DAC and the counter. This simple RC timing circuit will clear both chips upon system power-up. The 74LS161 was chosen because, like the DAC-8800, it has an asynchronous clear. The RC time constant should be set longer than the power supply turn-on time. The values shown in the circuit give a time constant of 10ms, which should be adequate for most systems. This same two-wire interface can be used for most three-input serial DACs.

STAND-ALONE OPERATION PROVIDING NONVOLATILE SETTINGS

Whenever a system with a DAC-8800 is powered on, the DAC-8800 needs to have all eight of its data words loaded to set the proper DC output voltages. In a system with a microprocessor or microcontroller, this is a straightforward operation. However, in some systems the DAC-8800 may be the only part with a digital interface. In this case, the circuit shown in Figure 12a will automatically load the DAC on system power-up. The core of the circuit is a serial input/output EEPROM device (U_2), preprogrammed with the appropriate data for the DAC. The counter labelled U_4 counts through 8 addresses, which are serially shifted into the EEPROM by U_3, a parallel to serial shift register. The EEPROM shifts out a 16-bit word associated with each address. Only 11 of the 16 bits are actually shifted into the DAC before the $\overline{LOAD}$ pulse arrives.

The second counter, U_7, in combination with the flip-flop U_6, counts the loading of the bits into the EEPROM and into the DAC-8800. When all the bits are loaded the logic sends a $\overline{LOAD}$ pulse which loads the DAC and increments the address on U_4. The timing diagram in Figure 12b gives a detailed description of the loading of one address. The CLK INH logic inhibits the shift register during certain CLK pulses because 9 bits need to be loaded into the EEPROM and only 8 bits are available in the register.

When the system is powered-up, R_1 and C_1 create a $\overline{PWRUP}$ pulse to asynchronously clear all of the counters and the DAC. After the $\overline{PWRUP}$ pulse goes high, the free running clock begins to load all 8 addresses. After the eighth address is loaded, the clock is disabled to remove any digital switching noise in the analog circuitry.

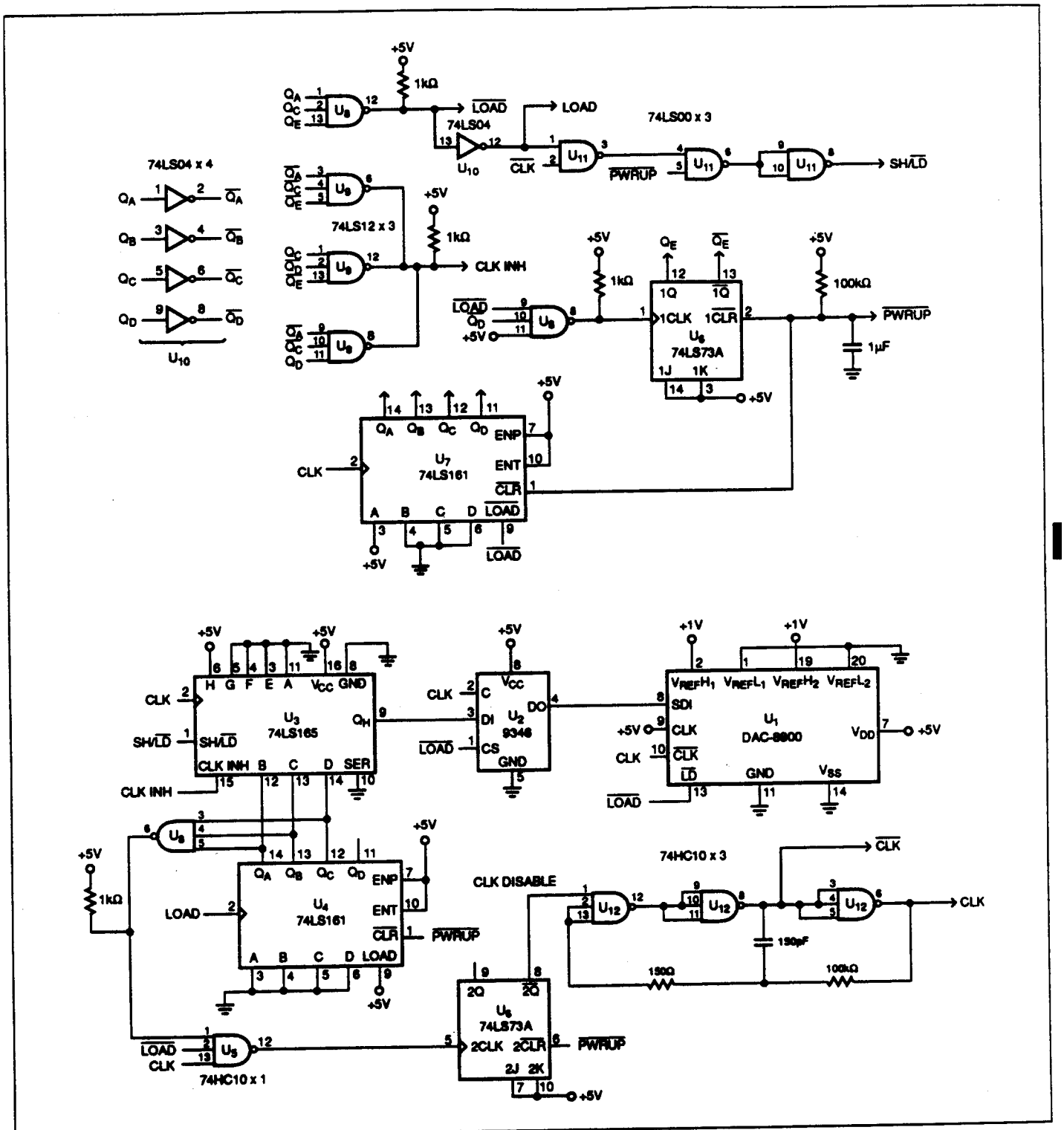

FIGURE 12a: *Stand-alone operation of the DAC-8800. The EEPROM stores data to set the DAC's output voltages on system power-up.*

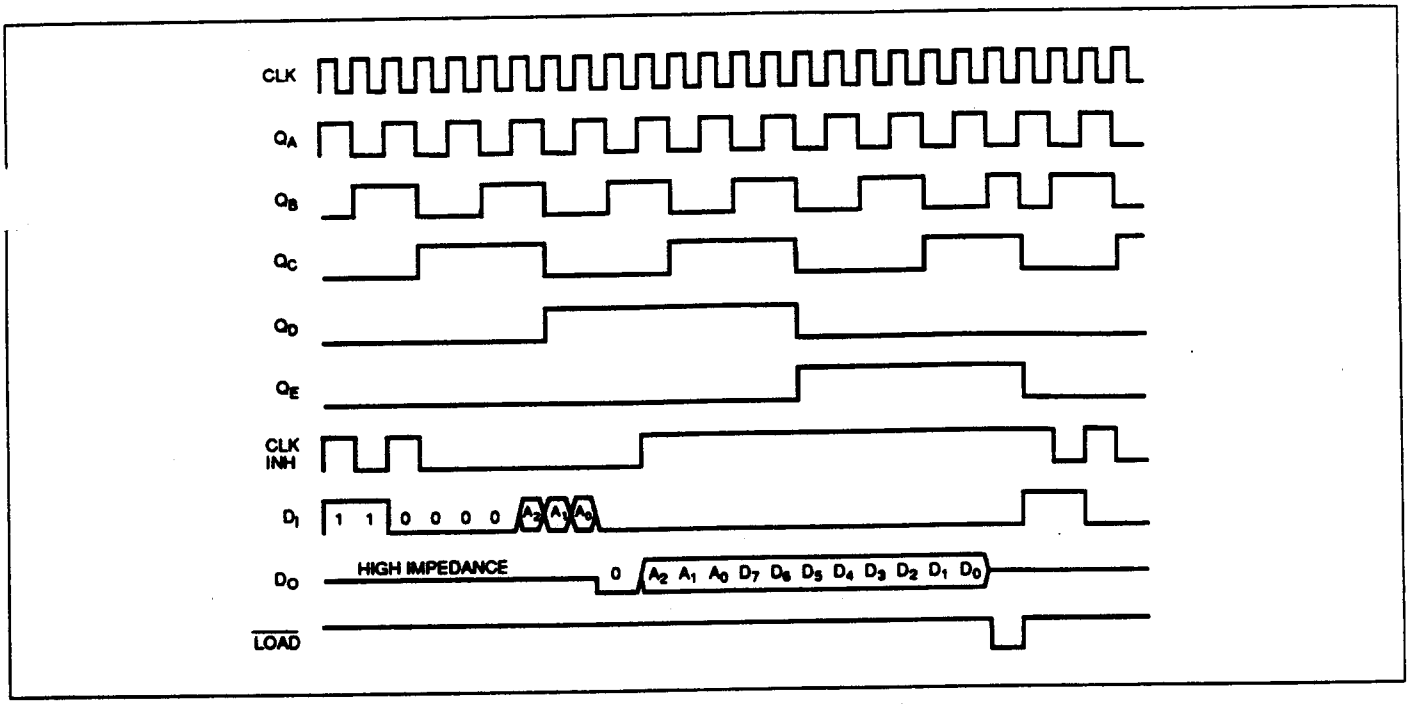

FIGURE 12b: *Stand-Alone Operation Timing Diagram*

DAC-8800 TEST FIXTURE

Figure 13 shows a fixture to test the DAC-8800. The circuit includes switches to set the address and data so that each DAC can be loaded with any digital word. After the switches are set, pressing the push-button activates the monostable multivibrator which generates the clock signal to load the DAC register. The counter selects the successive MUX channels, which switch the bits in proper loading order. After all eleven bits are loaded, the LOAD switch is manually toggled to generate a $\overline{\text{LOAD}}$ pulse. The $\overline{\text{CLR}}$ switch should be high at all times except to clear all eight DACs, in which case $\overline{\text{CLR}}$ needs to be switched low and then back to high. The CS switch should always be set low to keep the DAC selected at all times. The DAC-8800's outputs are buffered by OP-400 operational amplifiers; however, the outputs can be configured many different ways for the actual tests required.

CONDITIONS TO AVOID IN USING THE DAC-8800

The DAC-8800 is very resistant to the most common latch-up conditions.[1] For example, it does not latch-up when the digital inputs go high before the DAC is powered up. Nor is the DAC's own power supply sequencing significant. However, a few conditions still exist that are potentially destructive. In order to prevent damage from latch-up and ESD, the internal DAC-8800 design includes large body diodes placed from many of the pins to ground or either of the supplies, as shown in Figure 14. Looking at the placement of the diodes, it is easy to understand what conditions need to be avoided. The voltage across these diodes should be less than 0.3V, or they will start to turn on.

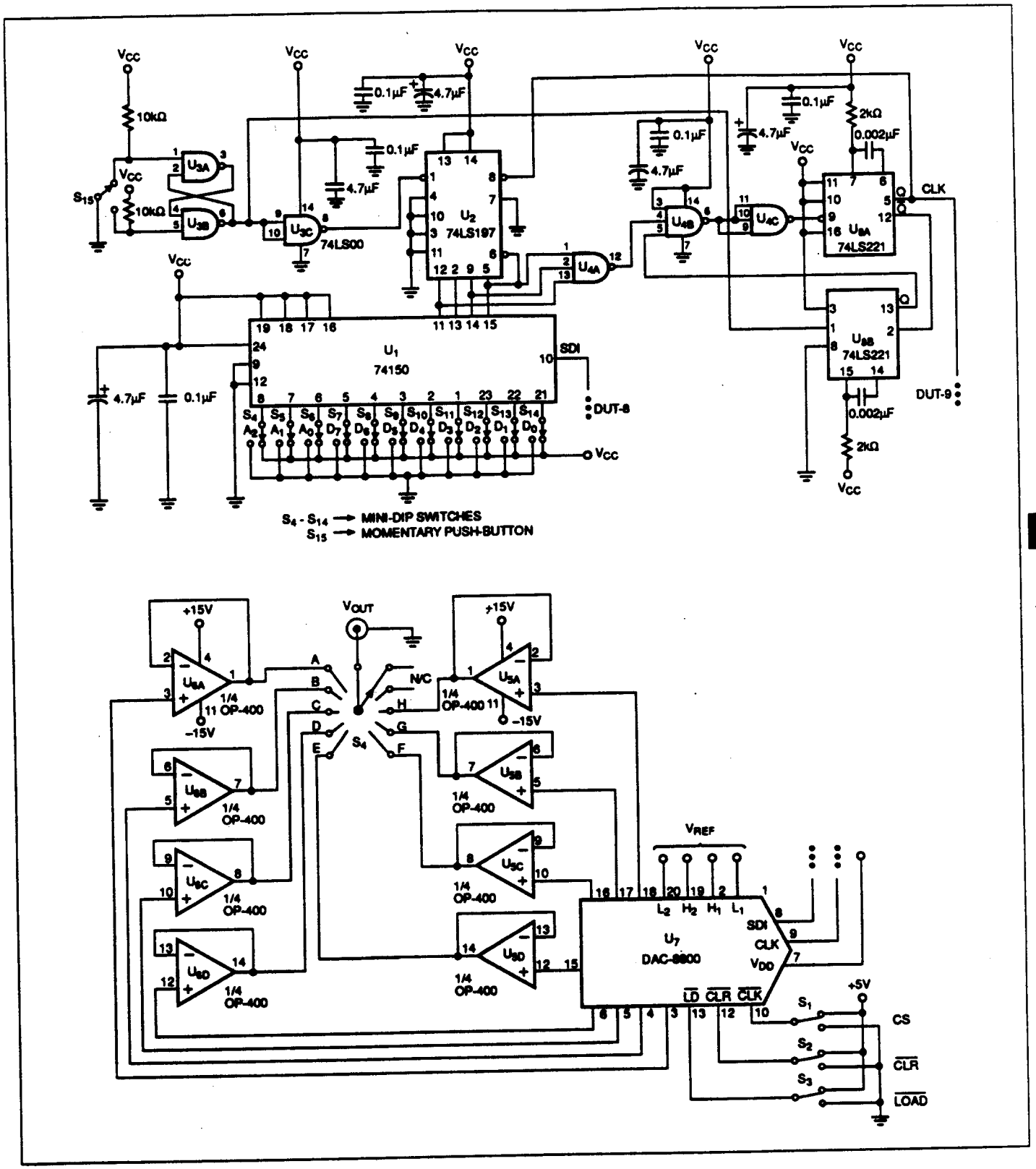

FIGURE 13: *DAC-8800 Test Fixture*

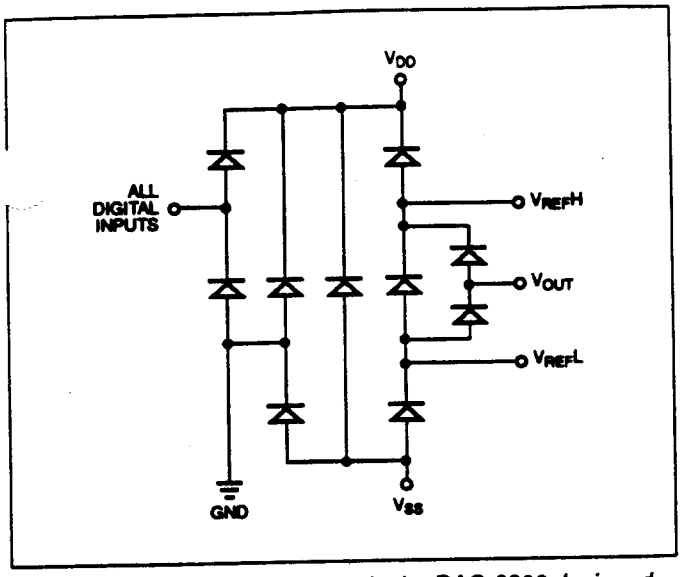

FIGURE 14: *Diagram of diodes in the DAC-8800 designed for ESD protection and latch-up prevention.*

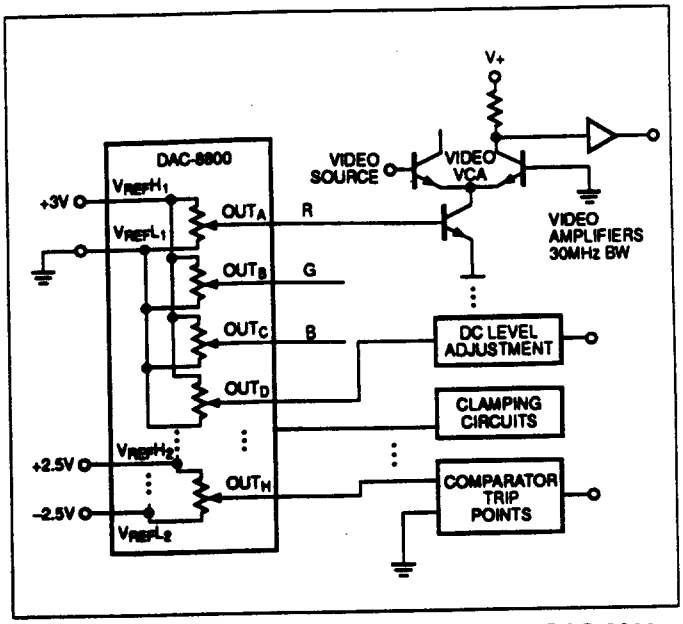

FIGURE 15: *Typical DC Adjustments Using the DAC-8800*

Even if one of the diodes does turn on the condition is not necessarily destructive. For example, the diodes from the digital inputs to V_{DD}, and from ground to the inputs, were made large enough to handle in excess of 200mA of current without being damaged. All the other diodes can handle at least 100mA. Thus, if there is any chance of any of the diodes forward biasing, the pin should be current limited. In the case of the digital inputs, a small series resistor can easily prevent more than 200mA from flowing.

APPLICATION CIRCUIT COLLECTION FOR THE DAC-8800

The DAC-8800 can be used for a wide variety of DC adjustment applications. The main point that needs to be remembered is that the DAC-8800 output is basically a voltage source with a 12kΩ output impedance. Thus, a high impedance load can be directly connected to the DAC's output, however with a low impedance load, the DAC's output may need to be buffered.

Figure 15 suggests numerous basic trimming operations that the DAC-8800 can be used for. Setting comparator trip points is a prime example of using the DAC-8800 to directly drive a high impedance load. The comparator's trip point can be digitally altered for different signal conditions. Another example of a high impedance load is controlling the gain of a video Voltage Controlled Amplifier (VCA) by altering the collector current through the differential pair. The DAC-8800 adjusts the base voltage of the current source transistor thus changing the collector currents. This in turn changes the transconductance of the differential pair transistors, which directly changes the gain.

DIGITALLY-CONTROLLED VCA

The DAC-8800 can also be used in audio systems to control the gain of a low distortion audio VCA such as the SSM-2014 (Figure 16). The SSM-2014 has over 100dB of dynamic range, and its gain is logarithmically proportional to the control voltage, V_C. The DAC can be connected directly to the control port of the VCA, which has a gain sensitivity of –30mV/dB. A reference range from +2.5V to –1.2V will give a gain range of –80dB to +40dB, and the SSM-2014 maintains flat gain and phase response to well above the audio frequency range of 20kHz for all gains. The circuit has a typical control feedthrough of 1.3mV/V at 100Hz. To minimize this effect, capacitor C_S is used to slow down the DAC transitions. Using 1.0µF gives a pole at 13Hz, which will filter out most of the glitch energy and any high frequency noise.

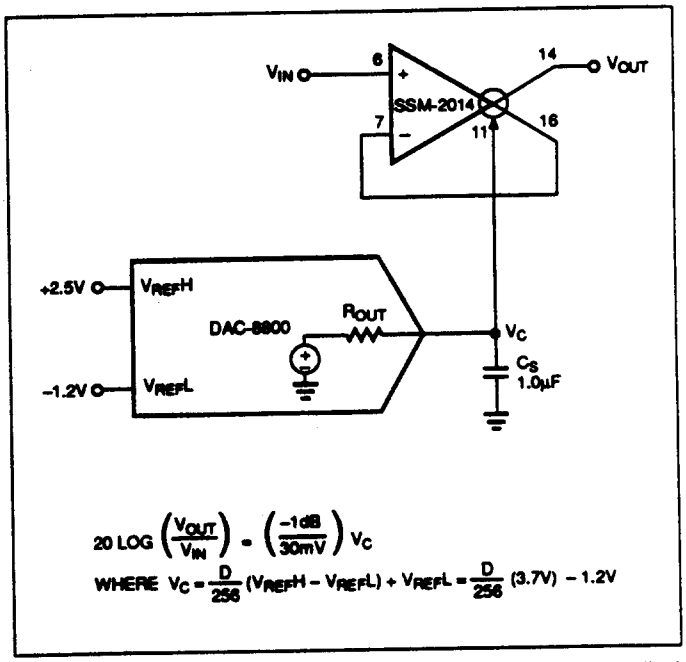

FIGURE 16: *Digital Gain Control Using a Voltage-Controlled Amplifier*

TRIMMING OP AMP OFFSET VOLTAGE

A frequently encountered DC adjustment application is trimming op amp offsets. There are many straight forward methods for trimming; one of which is connecting the DAC-8800 to the op amp's null pins. The DAC-8800 can directly null op amps to the negative supply, provided the supply is −12V or less in magnitude (Figure 17). This limit is because of the maximum 20V limit across the DAC. Since the positive supply needs to be at least +5V for logic interfacing, the DAC-8800's negative supply is safe to around −12V. The references used need to be near the voltage of the op amp's trim pins, which is typically a couple hundred millivolts above the negative rail. The figure shows reference values that work well for trimming the OP-42 over a ±40mV range. The actual voltages can be created using resistor dividers from the negative supply to ground and buffering the reference inputs with op amps. In cases where the op amp is adjusted from the positive rail, one of the alternative methods in the following paragraphs is needed. The reason for this is that the DAC-8800's output would need to be able to go up to the positive supply. However, $V_{REF}H$ is limited to 4V below the positive supply. Thus, the offset cannot be directly adjusted around the positive supply.

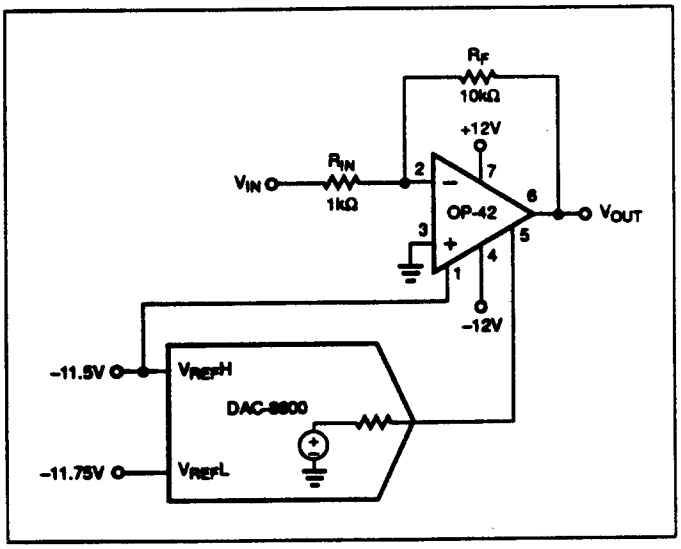

FIGURE 17: *Using the DAC-8800 for offset nulling directly on the op amp's null pins.*

A simpler method of offset nulling that gets around the supply voltage limitation is to connect the DAC-8800's output in series with a resistor to the summing node of the amplifier (Figure 18). This adds a small current that cancels the op amp's offset voltage. The series resistor should be large to provide a fine adjustment. The noise of the DAC and the series resistor might at first appear to be a problem, but it is actually attenuated by the 1kΩ input resistor. Therefore, the 1kΩ noise dominates. For the values in Figure 18, the adjustment range is ±50mV on the output. Figure

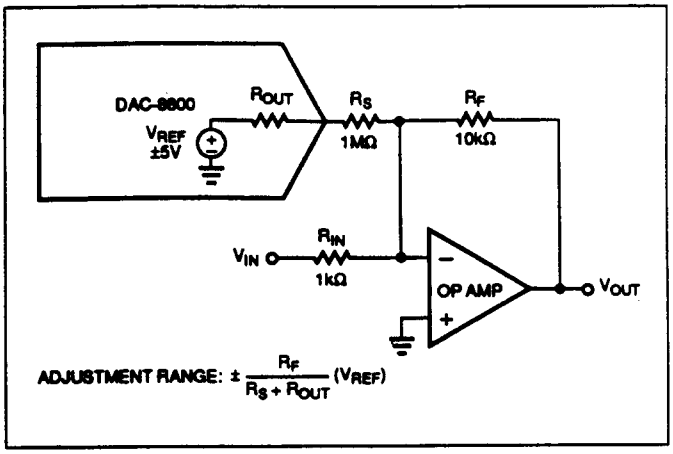

FIGURE 18: *Offset nulling by connecting the DAC-8800 to the summing node of an amplifier.*

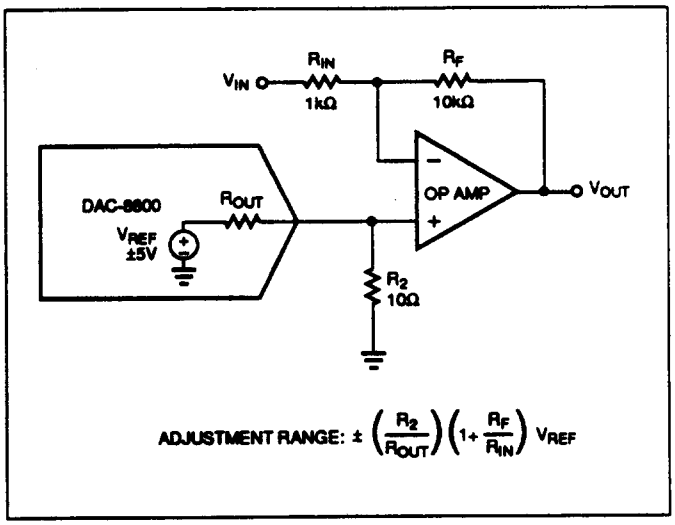

FIGURE 19: *Offset nulling by connecting the DAC-8800 to the noninverting node of an amplifier.*

19 shows an alternative method of offset nulling by adjusting the voltage at the amplifier's noninverting input. The resistor divider is recommended to provide for fine control of the offset. The adjustment range for the values in Figure 19 is ±42mV. The small resistor-to-ground also reduces the DAC's output noise to a point where it is insignificant compared to the op amp's own noise. With R_2 = 10Ω, the input noise caused by the DAC reduces to 15pV/$\sqrt{Hz}$; the noise of R_2 is much larger than this.

In both nulling applications shown, a positive and negative reference is required; however, in certain systems, only one reference may be available. Thus, the DAC-8800 can only adjust the offset in one direction. If this is the case, the amplifier can be forced to offset in either the positive or negative direction by connecting

one of the offset pins to the appropriate power supply voltage. Then the offset only needs to be adjusted in one direction, which the DAC-8800 can easily do with just one reference. Typical op amps have V_{OS} adjustment ranges on the order of ±5mV. Thus, the adjustment range of the DAC-8800 needs only to adjust the output offset by 10mV.

If the op amp is forced to offset in only one direction, the temperature coefficient of V_{OS} (TCV_{OS}) will almost certainly be affected. For a typical op amp, TCV_{OS} is directly proportional to the offset voltage. Thus, if the offset voltage is larger to start with, then TCV_{OS} will also be larger. For example, an op amp with a simple NPN input stage will exhibit a TCV_{OS} equal to V_{OS} divided by the temperature in degrees Kelvin at which that offset was measured. This translates to approximately 3μV/°C of TCV_{OS} for every millivolt of V_{OS}.

TRIMMING VOLTAGE REFERENCES

Figure 20 shows the DAC-8800 being used to trim a voltage reference such as PMI's REF-01. The output of the DAC is connected to the TRIM pin of the reference just as the wiper of a potentiometer would be connected. This entire circuit can easily be used in single supply applications because the DAC-8800's output can go to V_{SS}. Furthermore, this method can be used for all of PMI's references provided there is at least 4V of headroom between V_{DD} and V_{OUT}. The adjustment range of this circuit is the same as the ±300mV specified in the REF-01's data sheet.

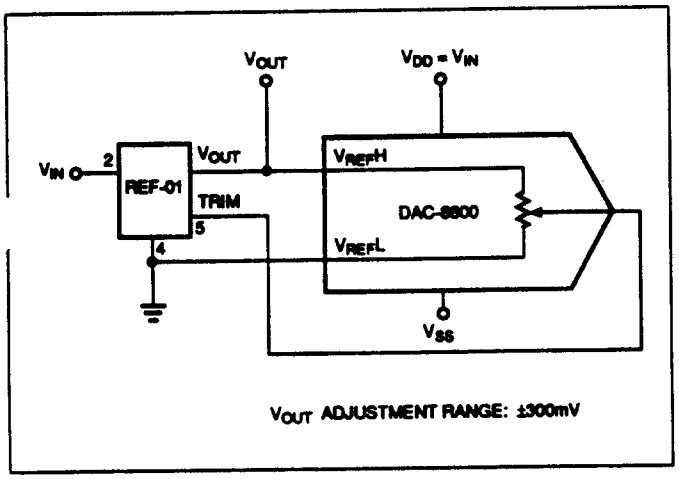

FIGURE 20: *Reference Trimming Using the DAC-8800*

COARSE-FINE CONTROL

Two of the DAC-8800's outputs can be connected together, and the resulting output is the average of the two unconnected outputs (Figure 21). This can easily be seen by thinking of the Thevenin equivalent circuit in Figure 3. The two output resistances in the same package are well matched so they form an accurate resistive divider, which averages the two DAC voltages. Such a circuit could be useful for performing a coarse-fine control, where one of the references is set to 1/10 the other reference. For example, setting $V_{REF}H_1$ to 1.0V, $V_{REF}L_1$ to −1.0V, $V_{REF}H_2$ to 100mV, and $V_{REF}L_2$ to −100mV gives an output adjustment range of ±0.5V ±0.05V.

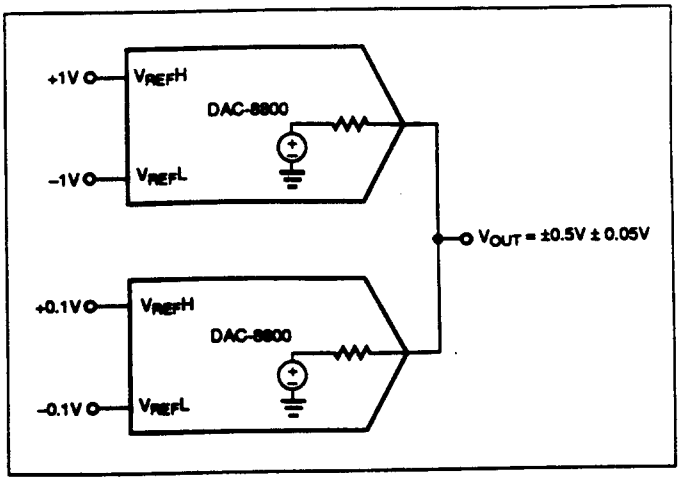

FIGURE 21: *Coarse-Fine Control by Averaging the DAC-8800 Outputs*

This application is limited by the voltage difference between the references. If $V_{REF}1$ is too much larger than $V_{REF}2$, the output voltage goes above $V_{REF}2$, and the switches in $V_{REF}2$ start to turn on independent of the digital code, which causes a significant error. It can even cause $V_{REF}2$ to increase by forcing current back into the reference, causing nonlinearities. The actual threshold for the switches turning on varies depending upon the common mode voltage of the two references, but the worst case is 1.5V between $V_{REF}1$ and $V_{REF}2$. Thus, the above example with $V_{REF}H_1$ = 1.0V and $V_{REF}H_2$ = 100mV works well, but increasing $V_{REF}H_1$ above 1.6V may cause the switches to start turning on. For unipolar applications, this problem can be avoided by connecting both the high references to ground and setting the low references to, for example, −10.0V and −1.0V. Configured this way, the output can never go above the high reference, and the switches will never turn on independent of digital code.

An alternative method that avoids the aforementioned problem is shown in Figure 22. Using this method, the output voltage can never be greater in magnitude than any of the references. To get the maximum output voltage, set both V_1 and V_2 to $V_{REF}H$, then the equation simplifies as follows:

$$V_O = V_{REF}H\,[\,(2R_{OUT} + R_S) / (2R_{OUT} + R_S)\,] = V_{REF}H$$

Thus, the maximum output voltage is equal to the reference of the DACs. Another advantage is that only half as many references are needed. One thing to be careful of is that the percentage adjustment range of each DAC output will vary with changing output resistances from device to device. In Figure 22, with R_{OUT} = 12kΩ, R_S = 96kΩ sets the output to be 10% of V_1 and 90% of V_2. However, if R_{OUT} changes to 8kΩ, then the percentages become 7% and 93%, respectively. If this is unacceptable, then R_S needs to be variable from at least 64kΩ to 128kΩ to cover the entire output resistance range of the DAC.

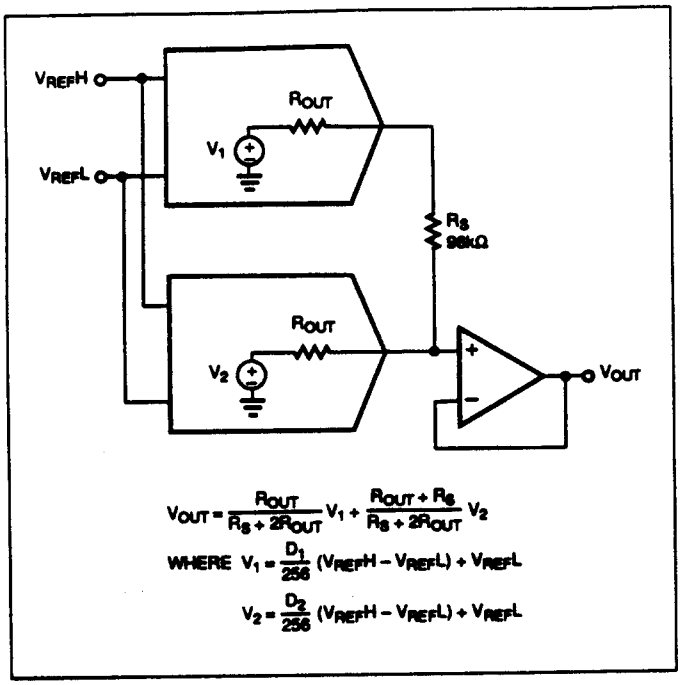

FIGURE 22: *Course-fine adjustment using the same reference for both DACs.*

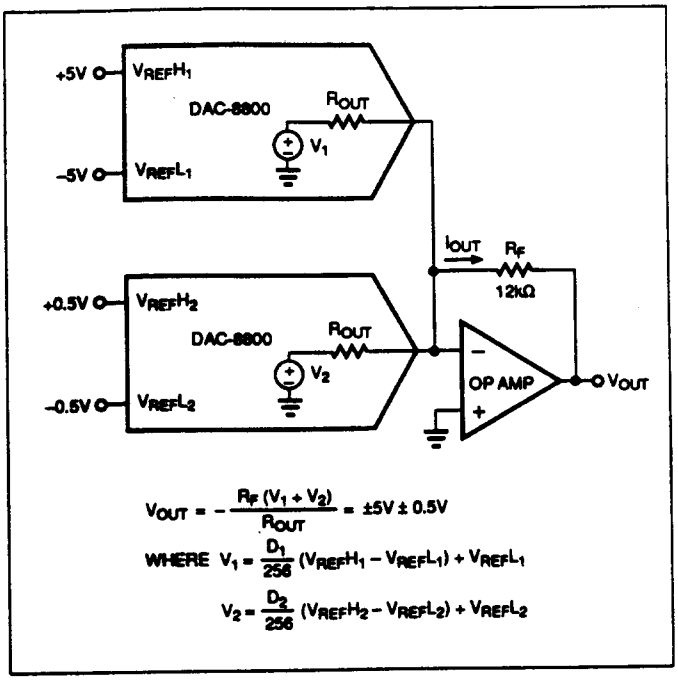

FIGURE 23: *Voltage summer by connecting the DAC-8800 outputs to the summing node of an amplifier.*

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Another method, shown in Figure 23, is current summing. In this case, the DAC outputs are connected to the virtual ground of the op amp, avoiding the problem of the switches being forced on. The feedback resistor should be 12kΩ to match the output impedance of the DAC-8800. As in the above application, the feedback resistor may need to be varied from 8kΩ to 16kΩ depending on variations in the DAC-8800's output resistance. Also remember that the op amp inverts the DAC's reference voltages, so a 5V high reference gives –5V at the output of the op amp.

AN ADJUSTABLE REFERENCE FOR ANALOG-TO-DIGITAL CONVERTERS

In an analog-to-digital conversion circuit the DAC-8800 works well as a digitally-controlled reference (Figure 24). Using the DAC, the reference voltage can be adjusted for different ADC sensitivities. The DAC-8800 output may need to be buffered by an op amp because of the typical ADC's low reference input impedance. For flash converters the typical input impedance is usually well below 1kΩ, which is much too low for the DAC-8800's output impedance of 12kΩ. A separate DAC in the same package can provide the negative reference as well, but it too has to be buffered with an op amp.

As can be seen by the many different application circuits shown in the above section, the DAC-8800 is a very versatile device. Of course, the application examples shown here are only a small selection of the many different ways the DAC-8800 can be used.

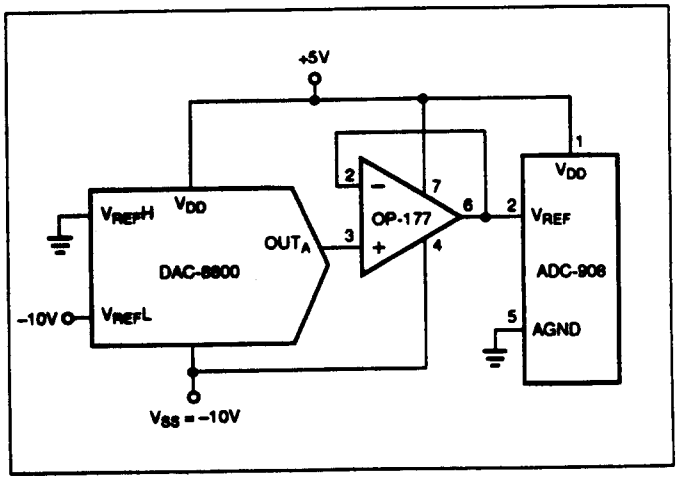

FIGURE 24: *The DAC-8800 as a digitally-controlled variable reference for ADCs. The DAC's output needs to be buffered by an op amp.*

REFERENCES

1. AN-109, Understanding and Preventing Latch-up in CMOS DACs, Analog Devices, Inc., January 1989.