ANALOG DEVICES

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APPLICATION NOTE

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Noise Sources in Low Dropout (LDO) Regulators

by Glenn Morita

WHY THE SOURCE OF NOISE MATTERS

The difference between insignificant noise and significant noise is the degree to which the noise affects the operation of the circuit in question.

For example, a switching power supply has a significant amount of output voltage ripple at 3 MHz. If the circuit it is powering has a bandwidth of only a few hertz, such as a temperature sensor, this ripple may be of no consequence. On the other hand, if the same switching power supply powers an RF phase-locked loop (PLL), the result could be quite different.

Understanding the sources of noise, their spectral characteristics, noise reduction strategies, and the sensitivity of the circuits in question to this noise is crucial to successfully designing a robust system.

This application note also attempts to clarify the difference between power supply rejection ratio (PSRR) and internally generated noise, and describes how to apply the data sheet specifications for each parameter.

NOISE SOURCES

The noise sources in a low dropout (LDO) regulator, or any circuit for that matter, can be separated into two broad categories, intrinsic and extrinsic. Intrinsic noise is like the noise in your head, and extrinsic noise is like the noise from a jet airplane.

Applied to electronic circuits, intrinsic noise is noise that is internally generated by any electronic device, whereas extrinsic noise is noise that is passed on from a source outside the circuit.

LDOs are easy to use; however, PSRR and internally generated noise are often confused. In many cases, the two are simply classified together as noise. This is a misapplication of the specifications because the two types of noise have different characteristics, and the methods for reducing their effect on system performance are different.

Figure 1 is a simplified block diagram of an LDO and shows how the intrinsic and extrinsic noise sources differ from each other. The error amplifier determines the PSRR of the LDO, and therefore, its ability to reject noise at its input. Intrinsic noise, however, always appears at the output of the LDO.

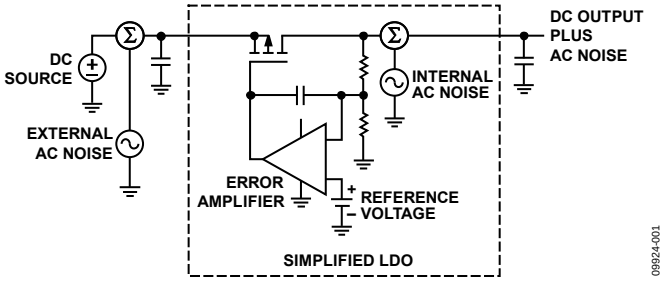

Figure 1. Simplified LDO with Intrinsic and Extrinsic Noise Sources

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REVISION HISTORY

6/11—Revision 0: Initial Version

INTRINSIC NOISE

There are many sources of intrinsic noise, and each has unique characteristics. Figure 2 shows how the noise of a typical device varies with frequency and the contribution of each type of noise to the total. The transition point from the 1/f region to the thermal region is called the corner frequency. The major types of intrinsic noise include the following: thermal noise, 1/f noise, shot noise, and burst, or popcorn, noise.

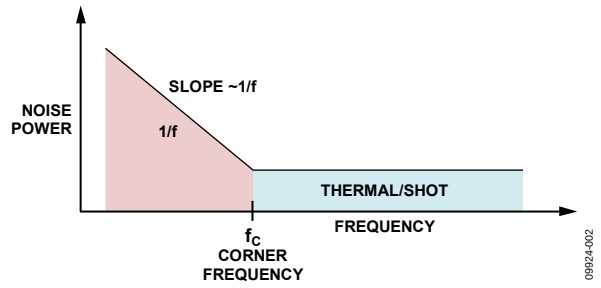

Figure 2. Typical Noise Power vs. Frequency

Thermal Noise

Thermal, Johnson, or white noise results from the agitation of charge carriers (electrons and holes) in any conductor or semiconductor at any temperature above absolute zero. Thermal noise power is proportional to temperature. It is random in nature and therefore does not vary with frequency.

Thermal noise is a physical process, and it can be calculated as

$$Vn = \sqrt{(4kTRB)} \quad (1)$$

where:
k is Boltzmann's constant (1.38^{-23} joules/Kelvin).
T is the temperature in degrees Kelvin (K = 273°C).
R is the resistance in ohms.
B is the bandwidth in Hz in which the noise is observed (rms voltage measured across the resistor is also a function of the bandwidth in which the measurement is made).

For example, a 100 kΩ resistor over a 1 MHz bandwidth, at room temperature, adds noise to a circuit and can be calculated as

$$Vn = (4 \times 1.38^{-23} \times 300 \times 1^5 \times 1^6)½ = 40.7\ \mu V\ rms \quad (2)$$

1/f Noise

1/f noise results from surface defects in semiconductors. 1/f noise power is proportional to the bias current of a device and unlike thermal noise, is inversely proportional to frequency. This inverse proportionality holds true for very low frequencies; however, above a few kilohertz, it is nearly flat. 1/f noise is also called pink noise because it tends to be weighted toward the low end of the frequency spectrum.

1/f noise is highly dependent on device geometry, device type, and semiconductor material. Because of this, mathematical models are extremely difficult to create, and empirical testing of individual cases is used to characterize and predict 1/f noise.

In general, devices with buried junctions, such as bipolar transistors and JFETs, tend to have lower 1/f noise than surface devices such as MOSFETs.

Shot Noise

Shot noise occurs where there is a potential barrier as in a PN junction. Due to the quantum nature of current flow in semiconductor devices, the current flow is not continuous. When the charge carriers, holes, and electrons cross the barrier, shot noise is generated. Like thermal noise, shot noise is random and does not vary with frequency.

Burst or Popcorn Noise

Burst, or popcorn, noise is a low frequency noise that seems to be associated with ionic contamination. Burst noise manifests itself as an abrupt shift in the bias current or output voltage of a circuit. This shift lasts for a short time before the bias current or output voltage suddenly returns to its original state. These shifts are random but seem to be proportional to the bias current and inversely proportional to the square of the frequency ($1/f^2$).

Due to the extraordinary cleanliness of modern semiconductor process technology, burst noise has been virtually eliminated and is not a major factor in device noise.

EXTRINSIC NOISE

Extrinsic noise sources are even more numerous than intrinsic sources. Extrinsic noise sources include the following:

- Electromagnetic fields that couple into sensitive circuits.
- Mechanical shock or vibration that causes piezoelectric materials to generate unintended ac voltages.
- Noise from other circuits that is conducted or radiated into circuits via the power supply or poorly designed PCB layouts.

Electromagnetic Coupling

Electromagnetic fields can induce noise into a circuit by one or more of the following methods: radiative coupling, capacitive coupling, inductive coupling, and conductive coupling. The effects of these types of coupling can be reduced through proper PCB layout and shielding techniques that are beyond the scope of this application note.

Piezoelectric Effects

Some components, such as high value multilayer ceramic capacitors, are sensitive to mechanical shock and vibration (that is, they are microphonic), which is due to the use of high dielectric constant materials in their construction. These dielectrics are highly piezoelectric in nature and can easily transform small mechanical vibrations into microvolt or even millivolt level signals. This is the reasons that high value ceramic capacitors are not recommended for use in low-level signal chain circuits.

Although film capacitors are not piezoelectric, they can also be sensitive to vibration. This is because any mechanical stress on the film dielectric changes the thickness of the film slightly, which causes the capacitance to increase or decrease very slightly. Because the energy stored in a capacitor is constant, the voltage must change slightly to accommodate the change in capacitance. The relationship between energy, capacitance, and voltage is described by the equation

$$E = \frac{1}{2} CV^2 \quad (3)$$

When mechanical stress is removed, the voltage on the capacitor returns to its original state. If the mechanical stress is periodic, a small ac voltage is generated.

Power Supply Noise

After intrinsic noise, power supply noise and ripple are generally the most prevalent noise sources at the output of an LDO. Depending on the spectral content of the noise source, an LDO can greatly improve the quality of the power to downstream circuits.

In many systems, power from the ac mains or batteries is converted to intermediate voltages for distribution throughout the system by highly efficient switch mode power supplies. These intermediate voltages are converted to specific voltages at the point of use.

The noise from a switch mode power supply depends heavily on its topology and load state. The spectral content can be from a few hertz to several tens of megahertz. In many cases, these noisy power distribution buses are cleaned up by LDOs in order to power sensitive analog loads. The ability of an LDO to reject noise from an input source depends on its PSRR and how it varies over frequency.

NOISE IN LDOs

The major sources of intrinsic noise in LDOs are the internal reference voltage and the error amplifier.

Modern LDOs operate with internal bias currents of a few tens of nano amps in order to achieve quiescent currents of 15 µA or less. These low bias currents require the use of large value bias resistors of up to a GΩ in value.

Reference Noise

Because the thermal noise of a resistor is defined as Vn = √(4kTRB), it can be seen that resistors can contribute a significant amount of noise to the reference circuit. Fortunately, the reference voltage of an LDO does not require a bandwidth of more than a few hertz, and on-chip passive filtering is easily achieved to reduce this noise.

For example, a band gap reference with a source impedance of 0.1 GΩ has 407 µV rms of noise from 10 Hz to 100 kHz. By limiting the bandwidth to 10 Hz, the noise can be reduced to 4.1 µV rms. If the bandwidth is reduced to 1.6 Hz, the noise contribution of the reference falls to 1.3 µV rms. A single-pole RC filter with a corner frequency of 1.6 Hz can be built with a 1 GΩ resistor and a 100 pF capacitor. Figure 3 shows how such a 1.0 V ultralow noise reference can be implemented in silicon.

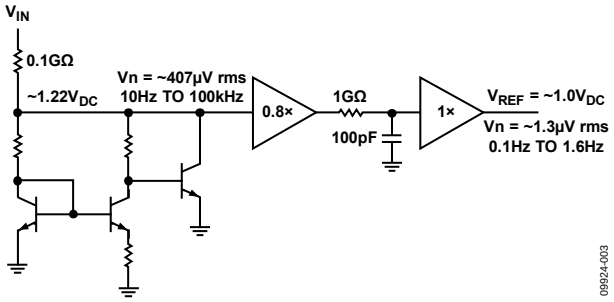

Figure 3. Ultralow Noise, Ultralow Power Reference (ADP223)

Error Amplifier Noise

If a low noise reference is used, the error amplifier becomes an important contributor to the total output noise. The noise contributions from the reference and error amplifier are uncorrelated and must be summed by the root mean square method.

Figure 4 shows an example of a 2.5 V output LDO with a 500 mV reference. The noise of the reference is given as 1 µV rms, and the error amplifier noise is 1.5 µV rms. The total noise of 9 µV rms is calculated as follows:

$$Vn = \sqrt{((G \times 1.5\ \mu V\ rms)^2 + (G \times 1.0\ \mu V\ rms)^2)} \quad (4)$$

$$G = 1 + 400\ k\Omega / 100\ k\Omega = 5$$

$$Vn = \sqrt{(7.5^2 + 5^2)} = 9\ \mu V\ rms$$

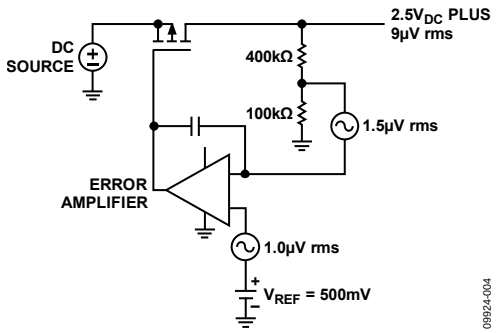

Figure 4. Noise Contributions from Reference and Error Amplifier (ADP223)

Reducing LDO Noise

There are two major methods for reducing the noise of an LDO:

- Filtering the reference
- Reducing the noise gain of the error amplifier

Some LDOs allow the use of an external capacitor to filter the reference. In fact, many so-called ultralow noise LDOs require the use of an external noise reduction capacitor to achieve their low noise specifications. The drawback of using external filtering of the reference is that the start-up time is proportional to the size of the filter capacitor. Figure 3 shows why this is the case. The node to which the 100 pF capacitor is connected is brought out for connection to an external capacitor.

Reducing the noise gain of the error amplifier does not have as dramatic an effect on the start-up time as filtering the reference, thus making the trade-off between start-up time and output noise easier. Unfortunately, reducing the output noise is generally not possible for fixed output LDOs because there is no access to the feedback node. However, the feedback node is readily accessible in most adjustable output LDOs.

If the noise contribution of the error amplifier is greater than the contribution of the reference, reducing the noise gain of the error amplifier can significantly reduce the overall noise of the LDO. One way to determine if the error amplifier is the main noise contributor is to compare the noise of the fixed vs. the adjustable versions of a specific LDO. If the fixed LDOs have much less noise than the adjustable LDOs, the error amplifier is the main noise source.

Figure 5 shows a 2.5 V output adjustable LDO where R1, R2, R3, and C1 are external components. R3 was chosen to set the high frequency gain of the amplifier to 1.5× to 2×. Some LDOs have low phase margins or are not stable at unity gain. C1 was chosen to set the low frequency zero of the noise reduction network (C1, R1, and R3) between 10 Hz and 100 Hz to ensure that the noise in the 1/f region is adequately reduced.

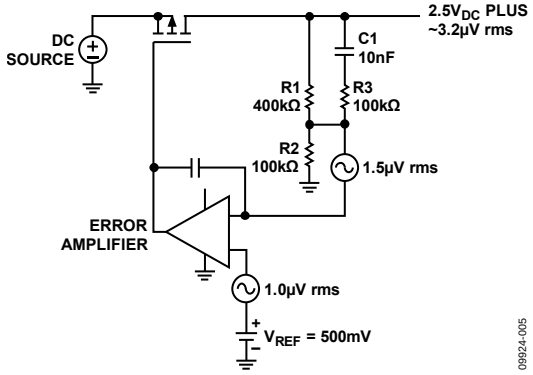

Figure 5. Reducing Noise Gain in an Adjustable LDO

Figure 6 shows the effect of the noise reduction (NR) network on the noise spectral density of a high voltage adjustable LDO. It can be seen in Figure 6 that between 20 Hz and 2 kHz there is an improvement of about a factor of three (~10 dB) in the noise performance. Notice that the two curves converge above 20 kHz, which is because the closed-loop gain of the error amplifier meets the open-loop characteristic of the amplifier, and no further reduction in noise gain is possible.

There is also an improvement in PSRR over the same frequency range (see the Improving PSRR section for more information).

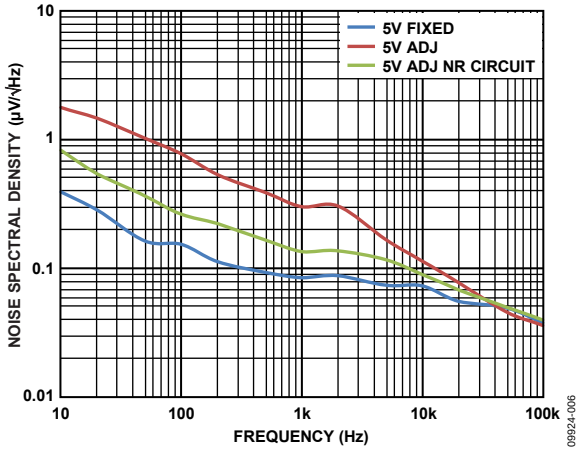

Figure 6. Noise Spectral Density of an Adjustable LDO

Noise Specification in LDO Data Sheets

Typically, the intrinsic noise of an LDO is specified in the data sheet in two ways:

- Total integrated noise over some bandwidth expressed as µV rms (see Figure 7)
- As a noise spectral density curve where the noise is plotted as µV/√Hz vs. frequency (see Figure 6)

Analog Devices, Inc., data sheets specify total integrated noise over a bandwidth of 10 Hz to 100 kHz. Figure 7 shows the relationship between the total rms noise for the ADP223 for various output voltages and load currents over a bandwidth of 10 Hz to 100 kHz.

Typically, the rms noise is lower at light loads because the bandwidth of the LDO is reduced along with the quiescent current. When the load current reaches a few milliamps, the LDO is operating at full bandwidth, and the noise remains constant with load.

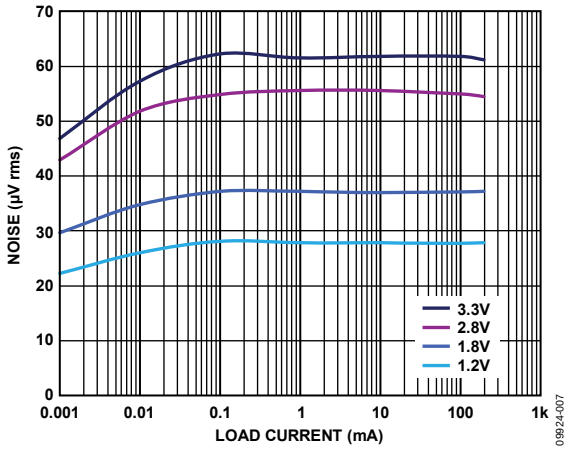

Figure 7. RMS Noise vs. Load Current and Output Voltage Plot (ADP223)

The noise spectral density plot of the ADP223 in Figure 8 shows how the noise spectral density varies with the output voltage over the frequency range of 10 Hz and 100 kHz. Integrating the data in this graph over the same bandwidth yields the rms noise. Use the following formula to estimate the rms noise for an arbitrary frequency range:

$$Vn = \sqrt{BW} \times \sqrt{(N_{FL}^2 \times N_{FU}^2)} \quad (5)$$

where:
$BW = N_{FU} - N_{FL}$.
N_{FL} is the noise in μV/√Hz at the lower frequency limit
N_{FU} is the noise in μV/√Hz at the upper frequency limit

For example, the rms noise between 10 Hz and 100 Hz of the 1.2 V output in Figure 8 is approximately

$$Vn = \sqrt{(100 - 10)} \times \sqrt{(1.18^2 \times 0.8^2)} \quad (6)$$

$$Vn = 8.9\ \mu V\ rms$$

The noise spectral density measurements are taken at a load current that is high enough to ensure that the LDO is operating at full bandwidth but not so high as to induce significant self-heating. For most LDOs with a maximum output current of 1 A or less, 10 mA is sufficient.

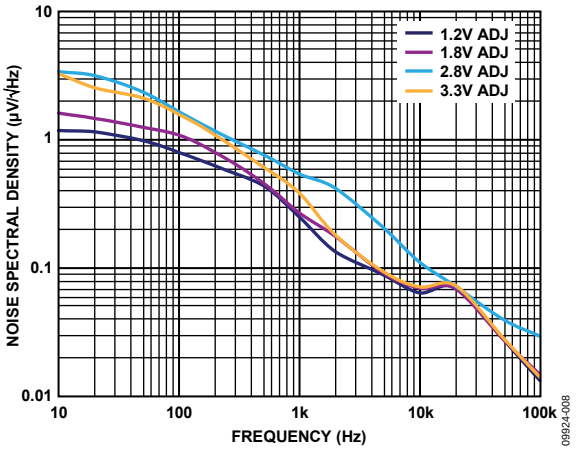

Figure 8. Noise Spectral Density vs. Output Voltage Plot (ADP223)

Comparing LDO Noise Specifications

Because the rms noise is expressed as a single number, it is a useful metric for comparing the performance of different LDOs. However, it is imperative that the noise specifications of the LDOs being compared are made under the same test conditions.

For example, the 1.2 V output ADP223 rms noise is about 27.7 μV rms from 10 Hz to 100 kHz. If the noise bandwidth is reduced to 100 Hz to 100 kHz, the rms noise decreases to about 26.2 μV rms. The rms noise falls because the 8.9 μV rms of noise in the 10 Hz to 100 Hz range is no longer included in the noise measurement.

$$Vn = \sqrt{(27.7^2 - 8.9^2)} = 26.2\ \mu V\ rms \quad (7)$$

It is also important to pay attention to any noise reduction features of the LDOs under consideration. LDOs that require external capacitors for noise reduction can be as much as 100× as noisy without the capacitor. In applications where small footprint and cost are a factor, an LDO that does not require an external noise reduction capacitor, but is slightly noisier than one that does require a capacitor, may be selected due to PCB area and cost savings.

LDO PSRR

The PSRR of an LDO is often confused with its intrinsic noise. Simply put, PSRR is a measure of how well a circuit suppresses or rejects extraneous signals (noise and ripple) appearing at the power supply input and keeps these unwanted signals from corrupting the output of the circuit. The PSRR of a circuit is defined as

$$PSRR = 20\log(VE_{IN}/VE_{OUT}) \quad (8)$$

where VE_{IN} and VE_{OUT} are the extraneous signals appearing at the input and output, respectively.

For circuits such as ADCs, DACs, and amplifiers, this PSRR applies to the inputs that supply power to the inner working of the circuit in question. In the case of an LDO, the input power pin supplies power to the regulated output voltage as well as to the internal circuitry.

PSRR AS A FUNCTION OF FREQUENCY

PSRR is not defined by a single value because it is frequency dependent. Figure 1 shows that an LDO consists of a reference voltage, error amplifier, and a power pass element, such as a MOSFET or bipolar transistor. The error amplifier provides the dc gain to regulate the output voltage. The ac gain characteristic of the error amplifier in large part determines the PSRR of the LDO. A typical LDO can have as much as 80 dB of PSRR at 10 Hz; however, the PSRR can fall to as little as 20 dB at a few tens of kilohertz.

The relationship between the error amplifier gain bandwidth and PSRR is shown in Figure 9. This example is a highly simplified case where the output capacitor and pass element parasitics are ignored.

The PSRR is equal to the reciprocal of the open-loop gain of 60 dB until the gain starts to roll off at 3 kHz. The PSRR decreases at a rate of 20 dB/decade until, at 3 MHz, the PSRR reaches 0 dB, where it stays for all higher frequencies.

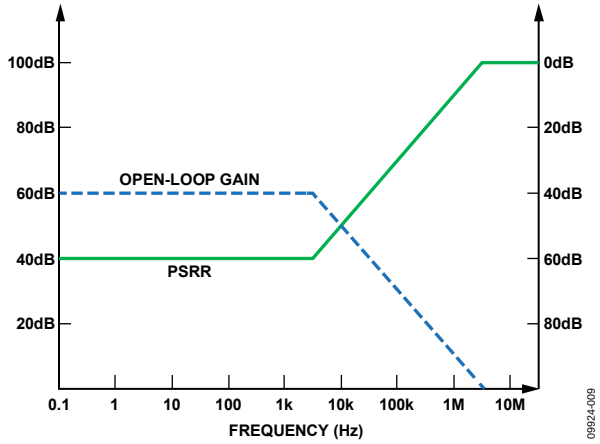

Figure 9. Simplified LDO Gain vs. PSRR

The PSRR plot in Figure 10 shows three main frequency domains that characterize the PSRR of an LDO: the reference PSRR region, the open-loop gain region, and the output capacitor region.

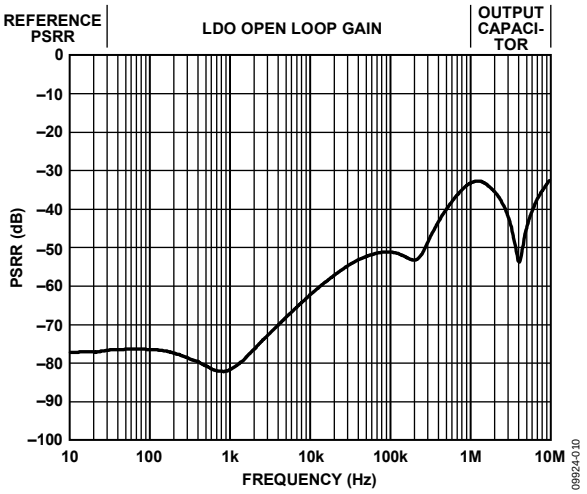

Figure 10. Typical LDO PSRR vs. Frequency

The reference PSRR region is dependent on the PSRR of the reference amplifier and the LDO open-loop gain. Ideally, the reference amplifier is fully isolated from perturbations in the power supply. In practice, the reference need only reject power supply noise up to a few tens of hertz because the error amplifier feedback ensures high PSRR at low frequencies.

Above 10 Hz or so, PSRR in the second region is dominated by the open-loop gain of the LDO. The PSRR in this region is a function of the error amplifier gain bandwidth up to the unity gain frequency. At low frequencies, the ac gain of the error amplifier is equal to the dc gain and remains constant until it reaches the 3 dB roll-off frequency. At frequencies above the 3 dB roll-off point, the ac gain of the error amplifier decreases with frequency, typically at a rate of 20 dB/decade.

Above the unity gain frequency of the error amplifier, the feedback of the control loop has no effect on the PSRR. PSRR is determined by the output capacitor and any parasitics between the input and output voltages. Output capacitor ESR and ESL, as well as board layout, strongly affect the PSRR at these frequencies. Careful attention to layout is essential to reduce the effect of any high frequency resonances.

PSRR AS A FUNCTION OF LOAD CURRENT

As shown in the PSRR as a Function of Frequency section, the PSRR of an LDO is dependent on the gain bandwidth of the error amplifier feedback loop. Anything that affects the gain of this loop affects the PSRR of the LDO. The load current can affect the PSRR in two ways.

At light load currents, typically less than 50 mA, the output impedance of the pass element is high. The LDO output appears to be an ideal current source due to the negative feedback of the control loop. Because of the pole formed by the output capacitor and the pass element, the output impedance occurs at a relatively low frequency and tends to increase the PSRR at low frequencies. The high dc gain of the output stage at low currents also tends to increase the PSRR at frequencies below the error amplifier unity-gain point.

At heavy loads currents, the LDO output looks less like an ideal current source, and the output impedance of the pass element is relatively low, which causes the gain of the output stage to decrease. The drop in gain of the output stage reduces the PSRR from dc to the unity-gain frequency of the feedback loop. Figure 11 shows how dramatically the dc gain can fall as a function of load current. Between 100 mA and 200 mA, the dc gain of the ADP151 decreases over 20 dB.

The output stage bandwidth increases because the output pole increases in frequency. At high frequencies, it seems that the PSSR should increase due to the increased bandwidth of the loop. In practice, the high frequency PSRR may not improve because of the decrease in overall loop gain. In general, PSRR at light loads is better than it is at heavy loads.

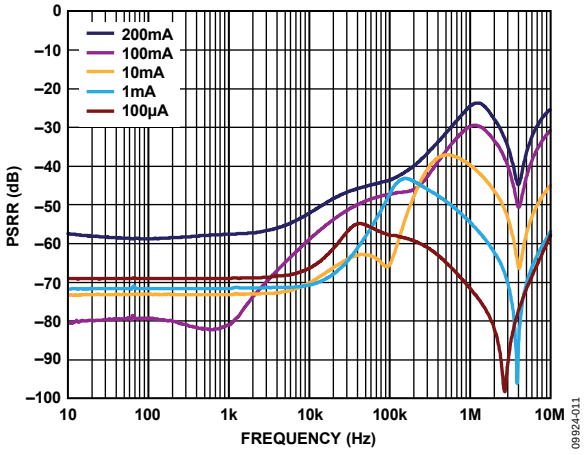

Figure 11. Typical LDO PSRR vs. Load Current (ADP151)

PSRR AS A FUNCTION OF LDO HEADROOM

The PSRR of an LDO is also a function of the input-to-output voltage differential, or headroom. For a fixed headroom voltage, PSRR decreases as the load current increases; this is especially apparent at heavy load currents and small headroom voltages. Figure 12 shows the difference in PSRR for a 2.8 V output ADP151 at 500 mV and 1 V of headroom with a load of 200 mA.

The gain of the pass element (PMOSFET for the ADP151) decreases as it leaves saturation and into the triode region of operation as the load current increases. This causes the overall loop gain of the LDO to decrease, resulting in a lowering of the PSRR. The smaller the headroom is, the more dramatic the reduction in gain. At some small headroom voltages, the control loop has no gain at all, and the PSRR falls to zero.

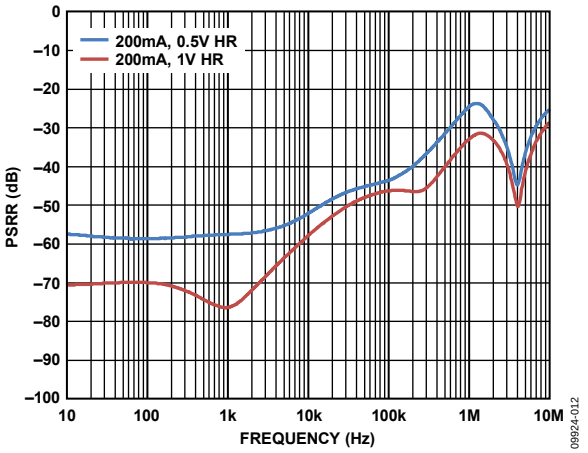

Figure 12. Typical LDO PSRR vs. Headroom (ADP151)

Another factor that reduces the gain of the loop is that the pass element has a nonzero resistance, or RDS_{ON}. The RDS_{ON} includes the MOSFET on resistance, the on-chip interconnect resistance, and the wire bonds. The RDS_{ON} is estimated by the dropout voltage of the LDO. For example, the ADP151 in the WLCSP has a worst-case dropout voltage of 200 mV at a 200 mA load. This means that the RDS_{ON} is about 1.0 Ω. Figure 13 shows a simplified schematic of the pass element and RDS_{ON}.

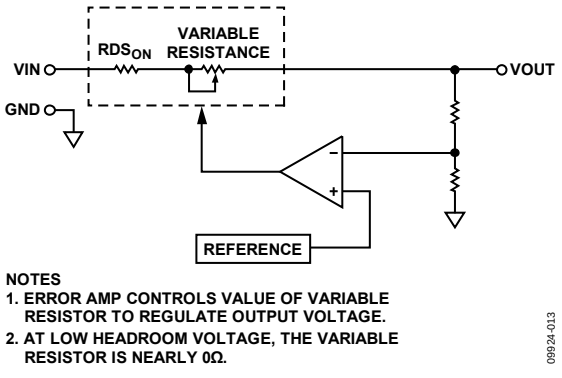

Figure 13. Simplified LDO Showing Pass Element Resistances

Any voltage drop across the RDS_{ON} due to the load current, subtracts from the headroom of the active portion of the pass element. For example, if the pass element is a 1 Ω device, a load current of 200 mA reduces the headroom by 200 mV. When operating LDOs at headroom voltages of 1 V or less, this voltage drop must be accounted for when estimating the LDO PSRR.

IMPROVING PSRR

For a given load current, the PSRR of an LDO can be improved in several ways:

- Operate the LDO with at least 1 V of headroom. Some LDOs, such as the ADP151, perform well with as little as 500 mV.
- Use an LDO with a maximum load current rating of at least 1.5× greater than the expected load.
- Add external filtering to the input or output of the LDO.
- Cascade two or more LDOs, if there is adequate headroom.

Adding External Filtering to Increase PSRR

The addition of external filtering can greatly improve the PSRR of an LDO circuit; however, it comes at the cost of additional circuit complexity and a decrease in headroom and efficiency. Depending on the application, the additional filtering can be added to the input (prefiltering) or output (postfiltering) of the LDO.

Postfiltering is often used if there is significant low frequency noise present at the output of the LDO. Postfiltering is no longer necessary with modern low noise LDOs, such as the ADP151. The disadvantage of postfiltering is that it incurs an additional load regulation error due to the resistance of the filter inductor.

Adding prefiltering is preferable when high frequency noise, such as the output voltage ripple of a switching converter, must be suppressed. It is also desirable because it does not affect load regulation.

Figure 14 shows an LDO circuit with both prefiltering and post-filtering; however, only one external filter is typically used.

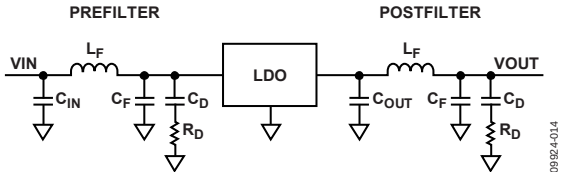

Figure 14. LDO with External Prefiltering and Postfiltering

The main filter components are L_F and C_F, which set the corner frequency of the filter. C_D and R_D damp the resonance of L_F and C_F. C_{IN} and C_{OUT} are the typical input and output capacitors used for the LDO, although C_{IN} is not necessary.

The following equations can be used to determine the values for C_F, L_F, C_D, and R_D:

$$1/(2\pi \times \sqrt{(L_F \times C_F)}) = Corner\ Frequency \quad (9)$$

$$C_D = 10 \times C_F \quad (10)$$

$$R_D = \sqrt{(L_F/C_F)} \quad (11)$$

For example, assume that 1 MHz ripple from a switching converter must be reduced by at least 30 dB. A corner frequency between 100 kHz and 200 kHz should be adequate.

From Equation 9, assuming C_F = 1 µF and L_F = 1 µH, f_C = 160 kHz. From Equation 10, C_D = 10 µF, and from Equation 11, R_D = 1 Ω.

Figure 15 shows the response of the example filter. The attenuation at 1 MHz is about 33 dB, and the maximum peaking is about 0.7 dB at 81 kHz.

The inductor L_F should have as low a dc resistance as possible to minimize the reduction in headroom, and in the case of a post-filter, load regulation error. The saturation current of the inductor must also be at least as high as the maximum expected load current of the circuit.

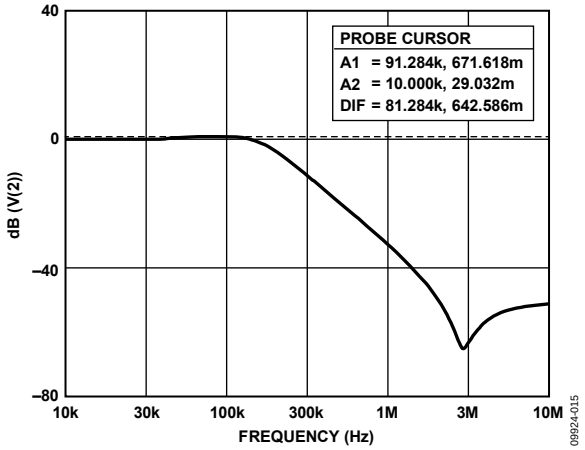

Figure 15. Response of the Example Ripple Filter

CASCADING LDOs TO INCREASE PSRR

In applications with adequate headroom, cascading LDOs, such as the ADP151, can greatly improve PSRR while preserving the low output noise characteristics of the ADP151. Figure 16 shows the schematic for two cascaded LDOs. The bypass capacitors, C_{IN}, C_{OUT}, and C_O, are equal to the value recommended in the ADP151 data sheet, in this case 1 µF.

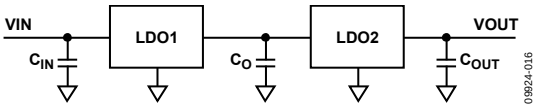

Figure 16. Cascaded LDOs

The output of LDO1 is chosen so that the headroom across LDO2 is at least 500 mV. The headroom across LDO1 should also be at least 500 mV for best results. Figure 17 compares the PSRR of a single 1.8 V ADP151 and two cascaded ADP151s. The load current and headroom are 200 mA and 1 V, respectively, in both cases. It can be clearly seen in Figure 17 that cascading two LDOs can improve PSRR by as much as 30 dB over a wide frequency range.

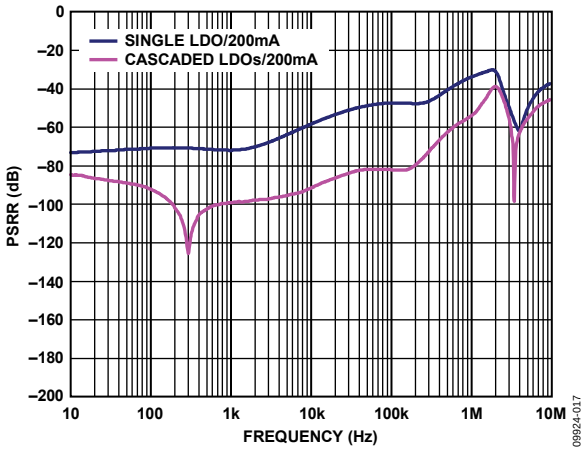

Figure 17. PSRR of a Single LDO and Cascaded LDOs

Comparing LDO PSRR Specifications

When comparing LDO PSRR specifications, ensure that the measurements are made under the same test conditions. Many older LDOs specify PSRR at only 120 Hz or 1 kHz with no mention of headroom voltage or load current. At the least, PSRR in the electrical specification table should be listed for different frequencies. Ideally, typical characteristic plots of PSRR under different load and headroom voltages should be used to make meaningful comparisons.

The output capacitor also affects the LDO PSRR at high frequency. For example, a 1 µF capacitor has 10 times the impedance of a 10 µF capacitor. The capacitor value is especially important at frequencies above the error amplifier 0 dB crossover frequency, where the attenuation of power supply noise is a function of the output capacitance. When comparing PSRR figures, the output capacitor must be the same type and value for the comparison to be valid.

TOTAL LDO NOISE

The intrinsic noise and PSRR both contribute to the total output noise of an LDO. Depending on the application, the contribution of intrinsic noise, PSRR, one or the other, or both may be important. When both PSRR and internally generated noise contribute to the overall performance of an application, a single figure for noise cannot be applied.

A typical application is a switching converter powering an RF PLL. To surpress the ripple from the switching converter, the output is regulated with an LDO. The intrinsic noise of the LDO slightly modulates the supply to the PLL and causes phase noise in the output of the PLL. Phase noise in the PLL is caused by the shift in the VCO frequency as a function of the supply voltage. This is expressed as $\Delta f/\Delta V$ and is often referred to as the pushing gain of the VCO.

The PSRR of the LDO reduces the switching converter noise up to the unity-gain frequency of the LDO. Beyond the unity-gain frequency of the LDO, the switching converter noise is attenuated by the LDO output capacitor, or by any passive filtering following the LDO. Harmonics of the switching converter frequency that are not adequately attenuated show up as spurs on either side of the PLL frequency.

SUMMARY

In general, LDO noise comprises two components: intrinsic, or internally generated noise, and extrinsic, or externally generated noise.

Thermal and 1/f noise are the main contributors to internally generated noise and are a function of the design and semiconductor technology of the LDO.

Extrinsic noise has many sources, but the most common is the noise on the input power supply to the LDO.

Because an LDO has high gain to ensure good line and load regulation, it is able to attenuate the noise and ripple from the input power supply. This is known as the PSRR of the LDO. The PSRR of the LDO decreases as a function of frequency because the LDO has a finite bandwidth. Noise beyond the bandwidth of the LDO is not attenuated and may be reduced with passive filter components.

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