AN-1091
APPLICATION NOTE

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Configuring the AD7606/AD7607 for Slow Supply Ramp Conditions

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INTRODUCTION

The AD7606/AD7606-6/AD7606-4/AD7607 are 16-/14-bit, simultaneous sampling, analog-to-digital data acquisition systems (DAS). The parts operate from a single 4.75 V to 5.25 V AV_{CC} supply and a 2.3 V to 5.25 V digital interface supply, V_{DRIVE}. This application note explains how to configure the AD7606/AD7607 to heighten application immunity when the ramp rate on the AV_{CC} and V_{DRIVE} is very slow or the time between the ramps on these supplies is long.

SLOW SUPPLY RAMP CONDITIONS

In multiboard systems where power supply circuitry is used to power multiple boards or on a board where there is heavy loading on the AV_{CC} and V_{DRIVE} supply generation circuitry, very long ramp rates may be seen at the AD7606/AD7607 AV_{CC} and V_{DRIVE} supply pins.

The AD7606/AD7607 mode of operation is controlled using pin programmable inputs. In an application, the pin programmable inputs can be hardwired to V_{DRIVE} or AGND or can be driven by general-purpose input/output (GPIO) pins. When the pin programmable inputs are hardwired to V_{DRIVE}, the logic state on these pins on power-up is determined by the voltage on V_{DRIVE}. The $\overline{STBY}$ and RANGE pins are individually used to control the standby power mode and the analog input range, respectively. However, to heighten the immunity of the AD7606/AD7607 to different supply ramp conditions, a combination of $\overline{STBY}$ and RANGE pins is used to control the full shutdown mode after supplies are established at the AD7606/AD7607.

CONFIGURING THE AD7606/AD7607 FOR SLOW SUPPLY RAMP CONDITIONS

To increase immunity to long supply ramp conditions, the AD7606/AD7607 should be placed into full shutdown mode and then switched to normal mode after the supplies are established at the AD7606/AD7607 pins.

To place the AD7606/AD7607 into full shutdown mode, the $\overline{STBY}$ and RANGE pins should be set low after the AV_{CC} and V_{DRIVE} supplies are established (see Figure 1 and Figure 2). When the $\overline{STBY}$ and RANGE pins are both low after power-up, or brought low after power-up, the AD7606/AD7607 are in full shutdown mode.

To place the AD7606/AD7607 into normal mode, for the ±10 V range, the $\overline{STBY}$ and RANGE pins are brought high (Figure 1).

For the ±5 V range, the $\overline{STBY}$ pin alone is brought high (see Figure 2). At this point, the REGCAPA, REGCAPB, and REGCAP pins power up to their correct potential as outlined in the AD7606 and AD7607 data sheets. If a $\overline{STBY}$ pulse is used to power up the AD7606/AD7607, the duration of the pulse should be 500 ns minimum.

Once fully powered up, the AD7606/AD7607 should see a RESET rising edge to configure the AD7606/AD7607 for normal operation. The time between coming out of full shutdown and the RESET high edge is specified as $t_{WAKE-UP\ SHUTDOWN}$, as outlined in the AD7606 and AD7607 data sheets.

Figure 1 shows how to control the $\overline{STBY}$ and RANGE pins for the ±10 V range. The $\overline{STBY}$ and RANGE pins return high to take the AD7606/AD7607 out of full shutdown mode and into normal mode and configure the AD7606/AD7607 for the ±10 V range. In Figure 2, the $\overline{STBY}$ pin alone is used to take the AD7606/AD7607 out of full shutdown mode. The RANGE pin can remain low to select the ±5 V range.

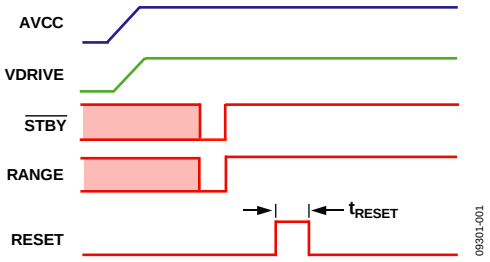

Figure 1. Placing the AD7606/AD7607 into Full Shutdown (±10 V Range)

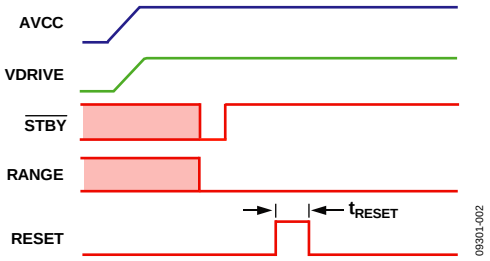

Figure 2. Placing the AD7606/AD7607 into Full Shutdown (±5 V Range)

CONCLUSION

Implementing the above scheme after the AV_{CC} and V_{DRIVE} supplies are established makes the AD7606/AD7607 immune to slow supply ramp conditions and to delays between the AV_{CC} and V_{DRIVE} supply ramps.

NOTES

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