ANALOG DEVICES

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APPLICATION NOTE

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Understanding the Input Reference Monitors of the AD9548

by Ken Gentile

INTRODUCTION

As indicated in the AD9548 data sheet, the AD9548 can support up to eight independent reference clock signals at its input. Each of the eight inputs has a dedicated reference monitor that determines whether the period of the input signal meets the requirements of the user. Figure 1 is a block diagram of the reference monitor and the necessary supporting elements. The reference monitor measures the period of the input reference signal and declares it as slow or fast, which constitutes a faulty reference. This information resides in the reference status register (each reference monitor has a dedicated status register available to the user). A reference that is neither fast nor slow is not faulty according to the reference monitor but is subject to further scrutiny by the AD9548 reference validation logic. Because they are all identical, Figure 1 shows only one of the eight reference monitors. Note, however, that all eight reference monitors share the same sample clock and the user-supplied nominal system clock period value (T_{SYS}).

Any device that measures time intervals must have a timing source. In the case of the AD9548 reference monitors, the timing source is the system clock that provides the sample clock for each of the eight reference monitors. Note that the sample clock has a period of $32T_S$ (where T_S is the period of the AD9548 system clock). Because the reference monitors must perform calculations to determine the period and accuracy of the input reference signals, a numerical representation of the system clock period is necessary. To accomplish this, the user provides a 21-bit number, T_{SYS}, which represents the nominal system clock period in units of femtoseconds (fs). For example, if the system clock frequency is 950 MHz, then T_S = 1,052,631.579 fs; therefore, T_{SYS} = 1,052,632 (after rounding to the nearest integer).

The purpose of the reference monitor is to measure the period of the input reference signal, T_{REF}. To accomplish this task, the reference monitor requires the user to provide the expected nominal period of the input reference signal, T_{NOM}, which is a 50-bit number with units of femtoseconds. For example, if the expected input reference frequency is 1.544 MHz, then T_{REF} = 647,668,393.782 fs; therefore, T_{NOM} = 647,668,394 (after rounding to the nearest integer). Note that T_{NOM} and T_{SYS} use units of femtoseconds so that both are expressible with at least 1 ppm precision relative to a 1 GHz signal.

It is important to note that T_S and T_{REF} are the real period of the system clock and input reference signal, whereas T_{SYS} and T_{NOM} are digital approximations of T_S and T_{REF}, respectively. This is a key distinction because the reference monitor relies on T_{SYS} being an accurate representation of T_S. Any deviation between T_S and T_{SYS} is a potential source of measurement error for the reference monitor. However, the error is quantifiable as described in Appendix A.

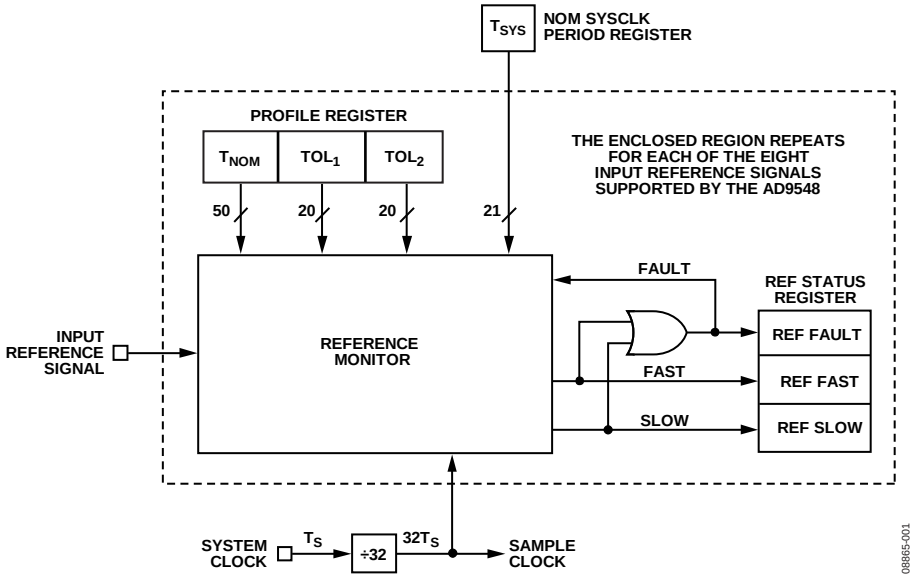

Figure 1. Reference Monitor and Supporting Elements

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THEORY OF OPERATION

The functional detail of the reference monitor appears in Figure 2. Note that the sample clock provides the timing source for the reference monitor and has a period of $32T_S$ (T_{CLK} in Figure 2). T_{CLK} has three primary functions.

- To reset the edge counter with each rising edge of T_{CLK}
- To clock the accumulator
- To clock the tolerance timer

EDGE COUNTER

The edge counter counts rising edges of the input reference signal, which occur at intervals of T_{REF}. It reports the number of edges counted as a 6-bit number, K (0 to 63). Note that if $T_{REF} > T_{CLK}$, then the counter occasionally outputs a value of K = 1 followed by a series of K = 0 values. The reason for this is that the counter captures a rising edge of T_{REF}, setting K = 1, but because T_{REF} is longer than T_{CLK}, the counter is reset by the rising edge of T_{CLK} before the occurrence of the next rising edge T_{REF}, which makes K = 0. The counter continues to output K = 0 until the next rising edge of T_{REF}, at which time, it sets K = 1 again, resulting in a continuous repetition of the sequence, K = 1 followed by 0s. On the other hand, if $T_{REF} \leq T_{CLK}$, the counter outputs a sequence of nonzero values (K ≥ 1) that depend on the number of T_{REF} edges occurring between each T_{CLK}-induced reset. Note that in the case of $T_{REF} \leq T_{CLK}$, the value of K is not necessarily constant but tends to dither around the integer closest to the value of T_{CLK}/T_{REF}.

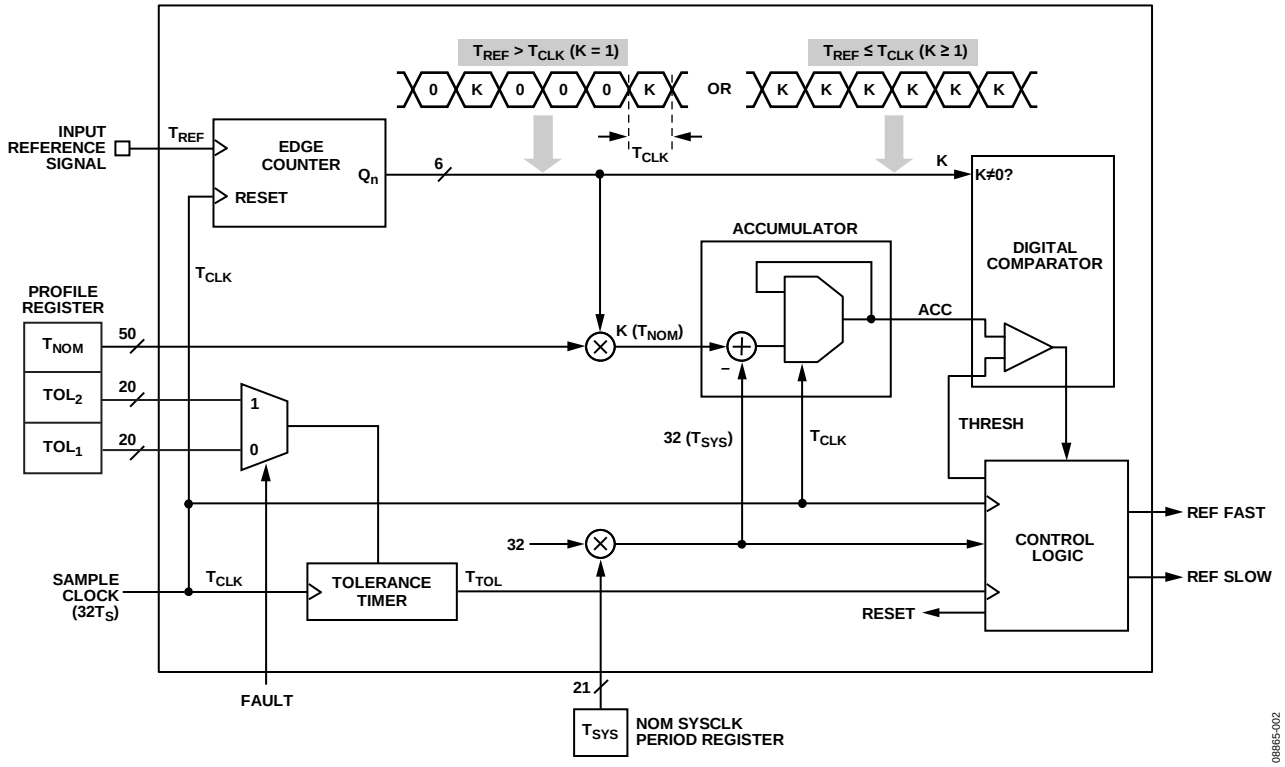

Figure 2. Reference Monitor Detailed Block Diagram

ACCUMULATOR

The accumulator output (ACC) tracks the residual timing difference between T_{CLK} and T_{REF}. It does so by accumulating the quantity, R.

$$R = K \times T_{NOM} - 32T_{SYS} \quad (1)$$

Recall that T_{NOM} and T_{SYS} are digital representations of T_{REF} and T_S, respectively. Furthermore, $32T_{SYS}$ is a digital representation of T_{CLK}, which is the sample clock for the accumulator and the reset signal for the edge counter. To get an idea of how accumulating R enables measurement of T_{REF}, consider the following case:

T_S = 1 ns (1 GHz)

T_{SYS} = 1,000,000 fs

T_{REF} = 300 ns (~3.33 MHz)

T_{NOM} = 300,000,000 fs

T_{CLK} = 32 ns

This is a case for which $T_{REF} > T_{CLK}$; therefore, the edge counter occasionally outputs a value of K = 1 followed by a series of K = 0 values (see Figure 3).

Note how the CLK waveform is offset from the REF waveform, demonstrating the asynchronous relationship between T_S and T_{REF}. Note, also, the relative timing markers (in units of nanoseconds) that appear below the REF and CLK waveforms. The initial rising edge of CLK clears the edge counter, and the subsequent rising edge of REF increments the edge counter; therefore, K = 1. The second rising edge of CLK clears the edge counter; therefore, K = 0, which continues to be the case until the next rising edge of REF (300 ns after the previous rising edge). This once again increments the edge counter and K = 1, but the next rising edge of CLK restores the edge counter to K = 0, and the sequence repeats. The accumulator sums R ($R = K \times T_{NOM} - 32T_{SYS}$) at sampling intervals of T_{CLK}, resulting in the ACC waveform shown in Figure 3.

Note that ACC tends to be close to 0 at the sampling interval just prior to each REF rising edge. Thus, the value of ACC one sample prior to the occurrence of K = 1 indicates how well T_{REF} matches T_{NOM}. A value near 0 indicates a close match. Note that for a reference signal slower than indicated by T_{NOM}, ACC drifts negative over time. The reason for this is that there are additional K = 0 values between successive rising edges of REF causing ACC to become more negative. Conversely, for a reference signal faster than indicated by T_{NOM}, ACC drifts positive over time because there are fewer K = 0 values between successive rising edges of REF.

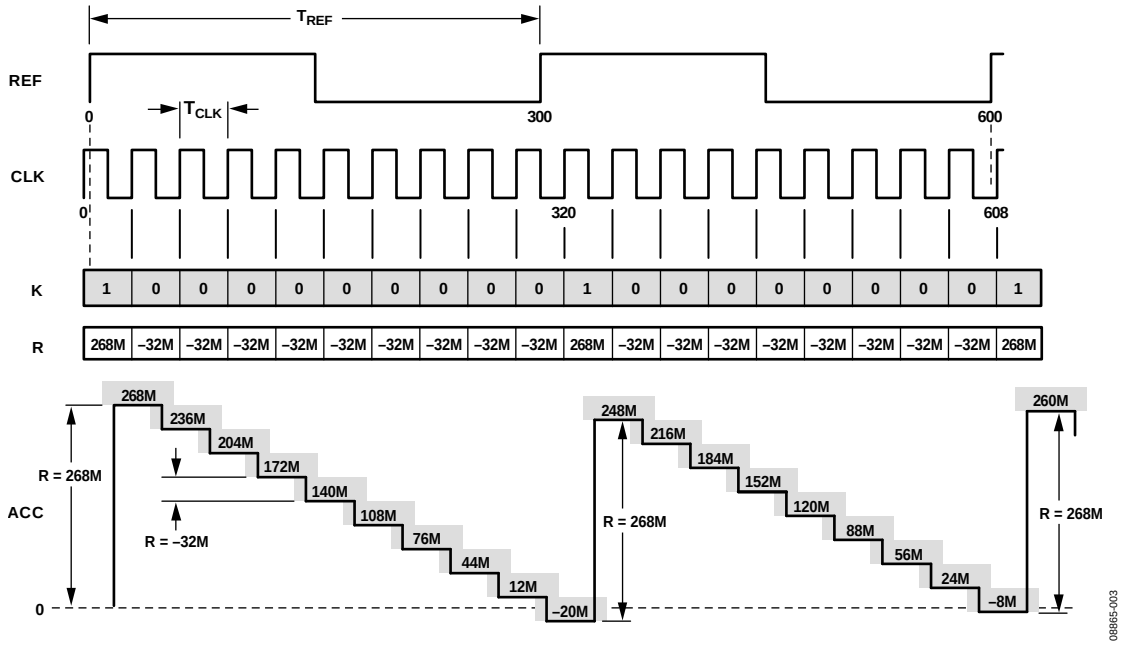

Figure 3. Accumulator Output Waveform for $T_{REF} > T_{CLK}$

The case for $T_{REF} \leq T_{CLK}$ is slightly different than the previous case, but the results are similar. For example, consider the following case:

T_S = 1 ns (1 GHz)

T_{SYS} = 1,000,000 fs

T_{REF} = 5 ns (200 MHz)

T_{NOM} = 5,000,000 fs

T_{CLK} = 32 ns

Because $T_{REF} \leq T_{CLK}$, the edge counter outputs a value of $K \geq 1$ for each T_{CLK} interval (see Figure 4). In fact, T_{CLK}/T_{REF} = 6.2; therefore, K dithers between 6 and 7. The result is that ACC tends to hold near 0, indicating a close match between T_{REF} and T_{NOM}. A reference signal slower than indicated by T_{NOM} causes the accumulator to drift negative over time. The reason for this is that K = 6 values occur more frequently for a slow reference signal than they otherwise should, which causes R to be negative more often, thereby forcing the accumulator in the negative direction. Conversely, a reference signal that is faster than indicated by T_{NOM} causes the accumulator to drift positive over time because K = 7 values occur more frequently for a fast reference signal than they otherwise should, which causes R to be positive more often, thereby forcing the accumulator in the positive direction.

The fact that the accumulator drifts negative for a slow reference signal and positive for a fast reference signal establishes a mechanism by which the reference monitor can determine if the reference signal is slow or fast. To accomplish this, a digital comparator tests whether ACC is within a threshold window (±THRESH). When ACC is greater than +THRESH, it indicates a fast REF signal. When ACC is less than −THRESH, it indicates a slow REF signal. However, the comparator only performs this test when K ≠ 0. This ensures that when $T_{REF} > T_{CLK}$ (see Figure 3), the test occurs at the rising edge of REF, which is when ACC is expected to be near 0.

Because the accumulator/comparator mechanism enables identification of a fast, slow, or acceptable reference signal, it shows some promise in being able to quantify the accuracy of a reference signal. For example, if a reference signal should be accurate to within 100 ppm, it is beneficial to have the reference monitor measure the reference signal with enough precision to make such a judgment. To do so, the reference monitor must satisfy the following criteria:

- It must have a stable and accurate timing source.
- It must observe the reference signal for a sufficiently long period.

The system clock presumably satisfies the first criterion. However, note that the reference monitor can be no more accurate than its timing source. For example, if the system clock has a 100 ppm accuracy specification, the reference monitor cannot guarantee a reference signal measurement to an accuracy less than 100 ppm. The second criterion implies the use of a timer that establishes a suitable observation period. This is where the tolerance timer comes into play.

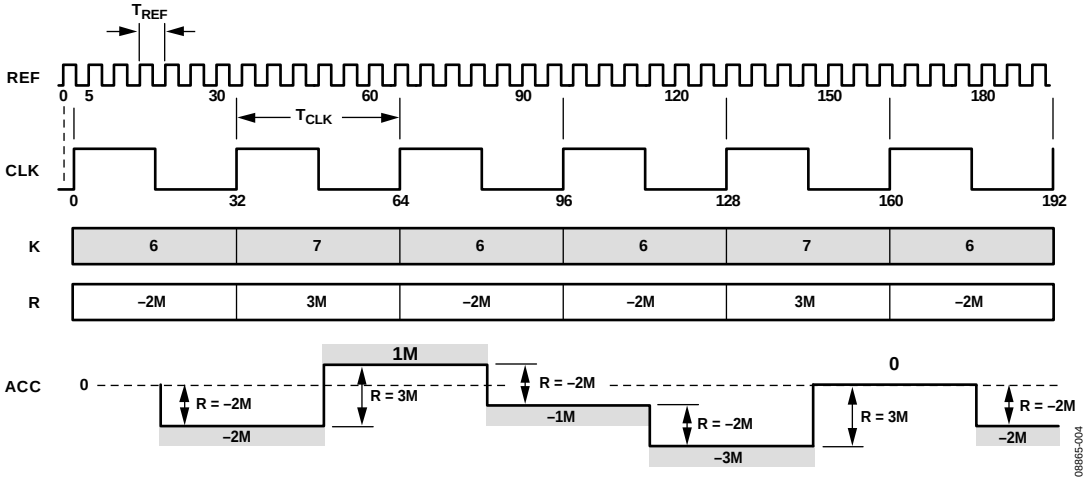

Figure 4. Accumulator Output Waveform for $T_{REF} \leq T_{CLK}$

TOLERANCE TIMER

The tolerance timer counts out a predefined number (TOL) of T_{CLK} periods that span a time interval, T_{TOL}.

$$T_{TOL} = TOL \times T_{CLK} \quad (2)$$

The AD9548 data sheet refers to two tolerance parameters associated with each input reference signal. The first is the outer tolerance, which is the maximum period deviation that a validated (that is, unfaulted) reference must exceed before being faulted. The second is the inner tolerance, which is the maximum period deviation that a faulted reference must not exceed to qualify as unfaulted (that is, suitably accurate for use). Note that separate inner and outer tolerance values enable custom configuration of each input reference with hysteresis regarding entry and exit of a fault condition. The TOL_1 register value specifies the outer tolerance and the TOL_2 register value specifies the inner tolerance (see Figure 1 and Figure 2). Both TOL_1 and TOL_2 are 20-bit values that have units of 1/tolerance. For example, if the outer tolerance specification is 50 ppm, $TOL_1 = 1/(50\text{ ppm}) = 1/(50/1{,}000{,}000) = 20{,}000$. To determine T_{TOL}, substitute the value of TOL_1 or TOL_2 for TOL in Equation 2.

DECISION THRESHOLD (THRESH)

Recall that T_{CLK} has a period of $32T_S$ and is the sampling clock for the reference monitor, which establishes the timing granularity of the reference monitor. Because TOL is the reciprocal of the desired tolerance, T_{TOL} is the minimum time interval necessary to measure T_{REF} with sufficient accuracy to meet the desired tolerance. Furthermore, the reference monitor has a digital representation for T_{CLK}, namely $32T_{SYS}$, which represents the timing granularity of the accumulator output (ACC). This implies that setting the decision threshold (THRESH) for the comparator to $32T_{SYS}$ and running the accumulator for a period of T_{TOL} satisfies the accuracy requirement for the desired tolerance.

Due to hardware constraints, however, the reference monitor requires THRESH to be at least $3 \times (32T_{SYS})$. This means that T_{REF} must deviate by at least three times the desired tolerance before the reference monitor indicates that it was too fast or too slow. This is a 300% error relative to the desired tolerance and is completely unacceptable.

The solution is to extend the observation period. To this end, the reference monitor observes the reference signal for a minimum of seven T_{TOL} periods before making a fast or slow declaration. However, each additional T_{TOL} observation interval means that ACC can accumulate another $32T_{SYS}$ of error and still meet the desired tolerance requirement. To compensate, it is necessary to increase THRESH by $32T_{SYS}$ with each additional T_{TOL} of observation time.

Thus, during the first T_{TOL} period, THRESH is set to $3 \times (32T_{SYS})$. During the next T_{TOL} period, THRESH is set to $4 \times (32T_{SYS})$, and so forth. That is,

$$THRESH = (3 + N) \times (32T_{SYS}) \quad (3)$$

where N is the number of T_{TOL} periods spanning the observation interval.

However, after N occurrences of T_{TOL}, the ideal value of THRESH is $N \times (32T_{SYS})$. This means that the actual value of THRESH is 3/N larger than the ideal value of THRESH. Therefore, the decision threshold is 3/N larger than what it should be for a given value of TOL. For N = 7 (the minimum number of T_{TOL} periods observed by the reference monitor), this represents an excess decision margin of 40%, which is much better than the 300% decision margin that results without the N = 7 minimum.

Because the reference monitor must wait long enough to capture two rising edges of T_{REF}, when T_{REF} is greater than $7 \times T_{TOL}$, the actual observation period could be significantly greater than the $7 \times T_{TOL}$ minimum. For example, consider the case for which T_{REF} = 1 sec with a desired tolerance of 10 ppm and with T_S = 1 ns. This yields TOL = 10^5 and T_{TOL} = 3.2 ms; therefore the number of T_{TOL} periods necessary to cover one T_{REF} period is T_{REF}/T_{TOL} = 312.5. This means that N = 313 and the excess decision margin is only 1% (as compared to 40% for N = 7). In summary, T_{REF} and T_{TOL} define N (N is the greater of 7 or T_{REF}/T_{TOL}), and the excess decision margin (3/N) is highest for N = 7 (~40%) but decreases as N increases. Furthermore, the excess decision margin is always positive; therefore, the reference monitor always makes its fast or slow decision with more leniency than the tolerance specified by the TOL value.

SUMMARY

Observation Interval and Automatic Adjustment of the Decision Threshold

The reference monitor uses a minimum observation interval of seven T_{TOL} periods. When $T_{REF} > 7\ T_{TOL}$, the reference monitor uses T_{REF} as the observation period. In both cases, the reference monitor increments THRESH by $32T_{SYS}$ for each T_{TOL} period after the first. The reference monitor control logic takes care of incrementing THRESH and extending the observation period as required. In addition, the control logic resets the accumulator, the tolerance timer, and the edge counter at the end of each observation period, which restarts the reference measurement process anew.

Early Detection of Slow (or Absent) Input Reference Signal

Even though the minimum observation interval is seven T_{TOL} periods, the reference monitor flags an out-of-tolerance reference signal as soon as the digital comparator detects that ACC is not within the ±THRESH limits. If $T_{REF} > T_{CLK}$, this occurs on the rising edge of the reference signal, but if $T_{REF} < T_{CLK}$, it occurs on the rising edge of T_{CLK}. In either case, the reference monitor declares the fault (fast or slow) before the expiration of the observation interval. Furthermore, because the reference monitor has access to the value of T_{NOM}, it declares a very slow (or absent) reference signal shortly after the T_{NOM} period elapses instead of waiting for the entire observation interval to expire. Note, however, that the reference monitor requires the entire observation interval before it can declare that a reference signal meets the tolerance limits.

Excess Decision Margin

The excess decision margin is given by 3/N, with N being the number of T_{TOL} periods that span the observation interval. The excess decision margin represents how much the input reference signal must exceed the desired tolerance before the reference monitor declares it as out of tolerance (that is, fast or slow). 3/N is a worst-case value; however, it does not include the error caused by a discrepancy between the real value of T_S and its digital representation, T_{SYS}.

Decision Errors Caused by a Deviation of the System Clock Frequency

The decision error caused by a discrepancy between the real value of T_S and its digital representation, T_{SYS}, can be determined from the information provided in Appendix A.

For example, here we apply Appendix A to the case of an expected reference frequency (F_{REF}) of 100 MHz (T_{NOM} = 10,000,000), an expected system clock frequency (F_S) of 1 GHz (T_{SYS} = 1,000,000), and the tolerance set for 1 ppm (TOL = 1,000,000). Next, by varying F_{REF}, the reference monitor indicates the results shown in Table 1. Note that the reference monitor indicates a faulty input reference signal when the frequency is in error by a little more than ±1 ppm, as expected.

Table 1.

Reference Monitor Result	Reference Frequency Deviation Required to Produce the Reference Monitor Result
Slow	< −1.294 ppm
Good	−1.294 ppm to +1.383 ppm
Fast	> +1.383 ppm

Next, we apply Appendix A to the same case but change F_S to +3 ppm (F_S = 1.000003 GHz). Varying F_{REF} causes the reference monitor to indicate the results shown in Table 2.

Table 2.

Reference Monitor Result	Reference Frequency Deviation Required to Produce the Reference Monitor Result
Slow	< +1.572 ppm
Good	+1.572 ppm to +4.383 ppm
Fast	> +4.383 ppm

Once again, apply Appendix A to the same case but change F_S to −3 ppm (F_S = 0.999997 GHz). Varying F_{REF} causes the reference monitor to indicate the results shown in Table 3.

Table 3.

Reference Monitor Result	Reference Frequency Deviation Required to Produce the Reference Monitor Result
Slow	< −4.294 ppm
Good	−4.294 ppm to −1.438 ppm
Fast	> −4.383 ppm

Table 2 reveals that the reference monitor declares an otherwise good input reference (±1 ppm) as slow when the system clock is 3 ppm fast. On the other hand, Table 3 reveals that the reference monitor declares an otherwise good input reference (±1 ppm) as fast when the system clock is 3 ppm less than its expected frequency. This demonstrates the importance of an accurate and stable system clock when trying to monitor a high precision input reference signal. Clearly, to monitor a 1 ppm input reference signal requires a system clock with accuracy and stability that is better than 1 ppm. As a rule of thumb, the system clock of the AD9548 should satisfy an accuracy and stability requirement that is ten times better than the input reference signal having the most stringent tolerance requirement.

APPENDIX A

MODELING THE BEHAVIOR OF THE AD9548 REFERENCE MONITOR

Modeling the reference monitor of the AD9548 requires the input parameters shown in Table 4.

Table 4.

Parameter	Definition
F_{SYS}	The expected system clock frequency
F_S	The real system clock frequency
F_{REF}	The expected input reference frequency
F_R	The real input reference frequency
ε	The tolerance requirement for F_{REF} (ε ≤ 10%)

The input parameters provide the information necessary to model the behavior of the reference monitor. The mathematical expressions for modeling the reference monitor rely on the definitions in Table 5.

Table 5.

Term	Definition
round(x)	Yields the nearest integer to x
floor(x)	Yields the nearest integer ≤ x
ceil(x)	Yields the nearest integer ≥ x
if(EXPR, x, y)	Yields x if test statement (EXPR) is true; otherwise, yields y

Following is a list of the mathematical expressions for modeling the reference monitor.

The nominal system clock period in femtoseconds expressed as an integer,

$$T_{SYS} = \text{round}(10^{15}/F_{SYS})$$

The nominal input reference period in femtoseconds expressed as an integer,

$$T_{NOM} = \text{round}(10^{15}/F_{REF})$$

The reference monitor sampling period,

$$T_{CLK} = 32/F_S$$

The reciprocal of the tolerance requirement expressed as an integer,

$$TOL = \text{floor}(1/\varepsilon)$$

The tolerance period (the duration of the tolerance timer),

$$T_{TOL} = TOL \times T_{CLK}$$

The number of input reference periods within seven tolerance periods,

$$N_{REF} = \text{ceil}(7 \times T_{TOL} \times F_R)$$

The observation period,

$$T_{OBS} = N_{REF}/F_R$$

The number of tolerance periods within the observation period,

$$N_{TOL} = \text{floor}(T_{OBS}/T_{TOL})$$

The number of reference monitor sampling periods within the observation interval,

$$N_{CLK} = \text{if}(F_R < F_{REF}, \text{ceil}(T_{OBS}/T_{CLK}), \text{floor}(T_{OBS}/T_{CLK}))$$

The value of the accumulator at the end of the observation interval,

$$ACC = \text{round}(N_{REF} \times T_{NOM} - N_{CLK} \times (32T_{SYS}))$$

The digital comparator threshold value,

$$THRESH = (3 + N_{TOL}) \times (32T_{SYS})$$

The relationship between ACC and THRESH determines whether the reference monitor declares the input reference signal (F_R) as slow or fast, as follows:

If ACC ≤ −THRESH, then the reference monitor declares F_R as slow.

If ACC ≥ THRESH, then the reference monitor declares F_R as fast.

If neither fast nor slow, then F_R is acceptable.

Use this model to determine the resulting excess decision margin for any arbitrary set of input parameters. For example, with a given F_S, adjust F_R and note when the model yields a fast result and a slow result. Then calculate the error of the input reference signal (F_R with respect to F_{REF}) corresponding to the points at which the results indicate fast or slow. The excess decision margin is the amount by which the calculated error exceeds the error defined by TOL (which is 1/TOL).

Figure 5 to Figure 9 are the results obtained by performing the procedure described in the previous paragraph with F_S = 1 GHz. The data points correspond to various settings of the expected input reference frequency parameter, F_{REF}, and tolerance setting parameter, ε, according to Table 6. Each figure shows the excess decision margin (in percent) for a particular subset of the ε values given in Table 6. Note that a particular ε value consists of two traces of the same color: a solid trace for fast indication and a dashed trace for slow indication.

Table 6.

Parameter	Values	Unit
F_{REF}	1, 3.1, 6.6, 10, 66, 100, 310, 660	Hz
	1, 3.1, 6.6, 10, 66, 100, 310, 660	kHz
	1, 3.1, 6.6, 10, 66, 100, 310, 660	MHz
ε	1, 3, 6, 10, 30, 60, 100, 300, 600, 1000, 3000, 6000, 10000, 30000, 60000, 100000	ppm

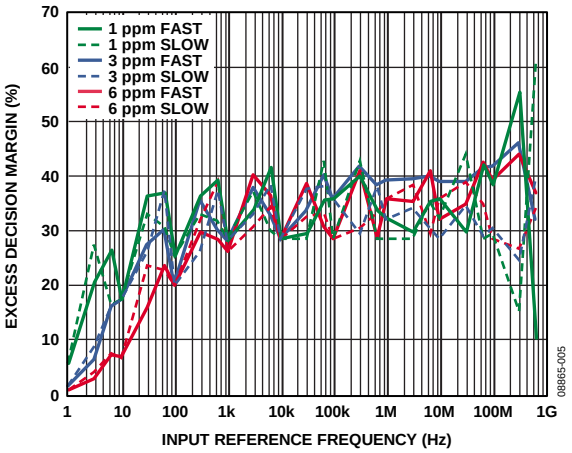

Figure 5. Excess Decision Margin for Tolerance = 1 ppm, 3 ppm, and 6 ppm

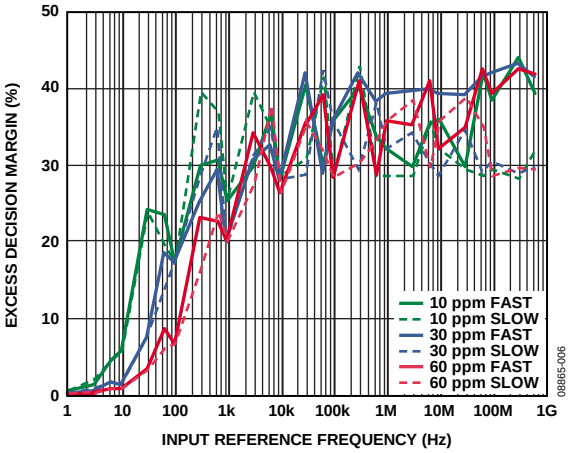

Figure 6. Excess Decision Margin for Tolerance = 10 ppm, 30 ppm, and 60 ppm

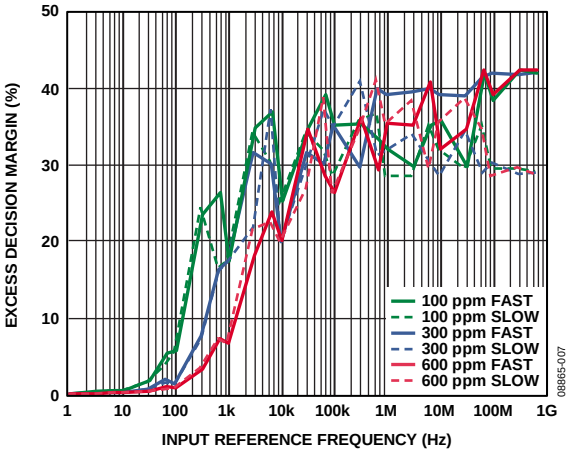

Figure 7. Excess Decision Margin for Tolerance = 100 ppm, 300 ppm, and 600 ppm

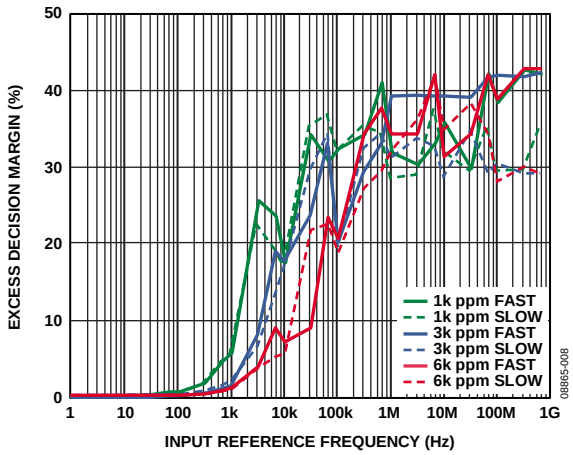

Figure 8. Excess Decision Margin for Tolerance = 1000 ppm, 3000 ppm, and 6000 ppm

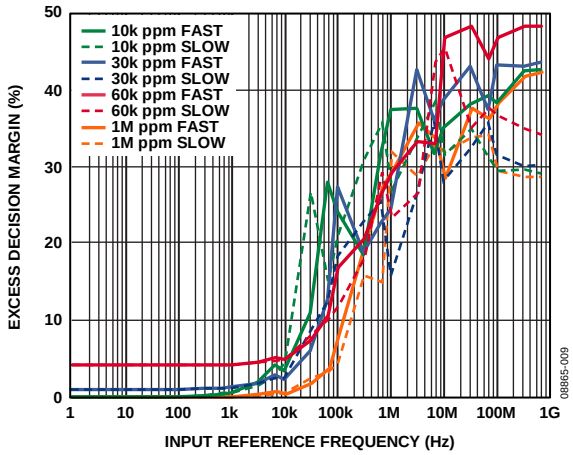

Figure 9. Excess Decision Margin for Tolerance = 10,000 ppm, 30,000 ppm, 60,000 ppm, and 100,000 ppm

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