

analog dialogue

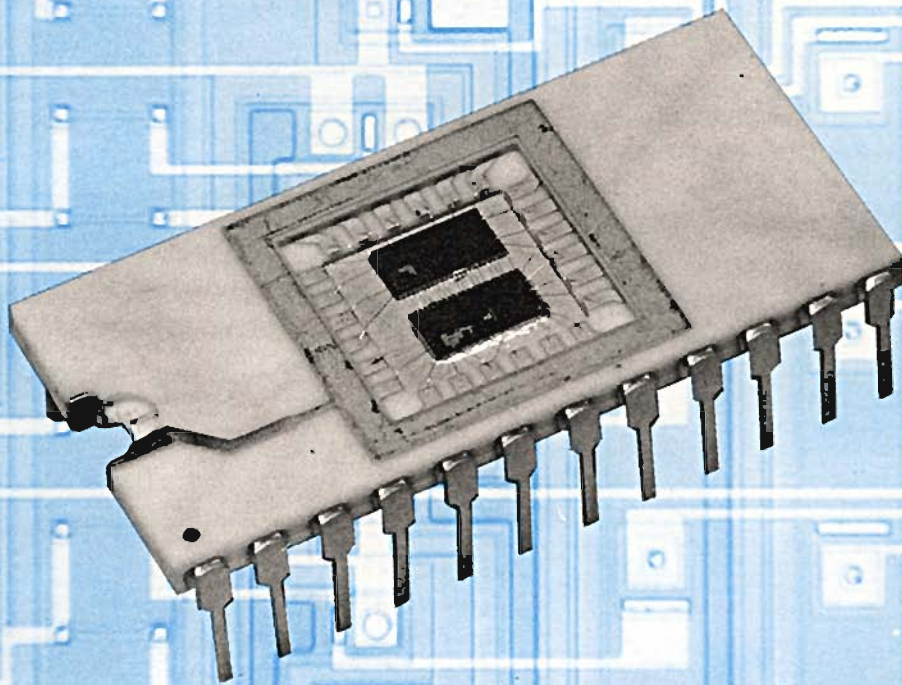
A forum for the exchange of circuit technology: Analog and Digital, Monolithic and Discrete

12-BIT IC D/A CONVERTER (P. 3)

Also in this Issue:

- CMOS Analog Switches for Many Purposes
- Constant Voltage Regulator
- New Thin-Film Resistor Networks

Full Contents
on Page 3



Editor's Notes

Some months ago, an Analog Devices advertisement bravely proclaimed the *double entendre*: "We've got designs on the analog CMOS market." The concrete meaning, explicitly stated in the ad, was the introduction of three new analog CMOS circuit designs: a quad switch, an 8-channel multiplexer, and a 4-channel differential multiplexer.

Also present was the veiled implication of an ambition and a reasoned purpose—that there was more to come. And indeed there was. The next —and perhaps the best-known— product was the AD7520 10-bit D/A converter, the first commercially-available CMOS D/A converter, the first to utilize thin-film-on-CMOS resistors, and (it appears) the first monolithic 10-bit converter to be readily available to all at reasonable prices, off the shelf.

And now comes a major thrust, the introduction of a whole family of CMOS analog switches, for a wide variety of purposes. Some are proprietary ADI designs; others are "second-source items," so that you can try ours without a "cold-turkey" withdrawal from a circuit configuration you may have grown accustomed to.

Whatever the circuit, though, you're coming to specialists in *analog* CMOS. We don't make watches; we don't make LSI memories; we don't make microprocessors. So we can concentrate on supplying circuits designed by *analog* circuit specialists to bring the benefits of CMOS to analog-circuit switching, benefits such as low quiescent-power-drain, low capacitance, high open-circuit resistance, and reasonably-constant, reasonably-low closed-circuit resistance. An additional benefit is *availability*; these circuits are our bread-and-butter, so we can't afford long delivery time or non-competitive prices.

Finally, since our sales engineers exist to deal competently and successfully in the analog circuit elements you use the switches with — ADI op amps, conversion circuits, and precision resistance networks —they bring a sympathy for and an understanding of the *analog* problems you are using the switches to solve, a rare phenomenon in the go-go, largely-digital world of CMOS.

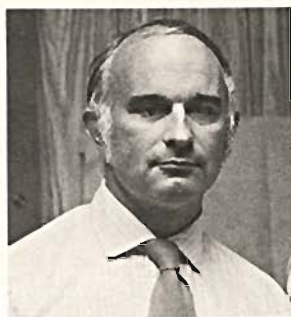
A PLEA FROM THE SUMMING POINT

This issue of *Analog Dialogue* has 24 pages, a record for a single issue. Among its discussions of technologies, new products, and applications, are two items that were either written by or originated by readers. If the increase in numbers of pages signifies a long-term trend, we consider it essential that these pages contain more contributions from outside our corporate family. We (again) invite our readers to submit brief and practical application notes dealing with new or improved ways of using analog circuit elements. Or if your need for such ideas exceeds your production of them, we'd like to know what your needs are, so that we can be sure that the material we publish continues to be relevant to them. We're trying our best to keep you informed; but it is very important that you keep us informed. That's at the heart of an *analog dialogue*.

Dan Sheingold



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12-BIT INTEGRATED CIRCUIT D/A CONVERTER

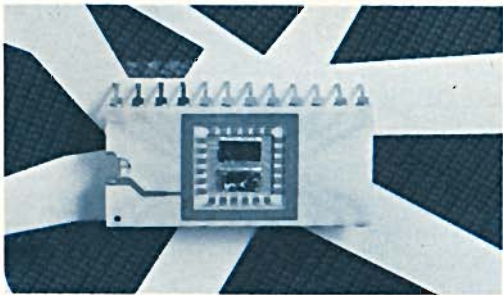
GUARANTEED MONOTONIC, BINARY OR BCD, POSITIVE TRUE, TTL OR CMOS

by Bob Craven and Stan Harris

The AD562* is a 12-bit integrated-circuit digital-to-analog converter in a hermetically-sealed 24-lead ceramic dual in-line package. This small, reliable, low-cost, high-speed device is available in both binary and BCD versions. Monotonic 12-bit resolution is guaranteed over the operating temperature range, with less than 1/2LSB (1/4LSB for AD562S) *max* total error at +25°C, and 3ppm/°C *max* gain-temperature coefficient. The circuit assembly consists of two interconnected chips: (1) a monolithic bipolar transistor chip, which contains the 12 precision current switches, and (2) a compatible Si-Cr thin-film resistor chip, with the bit-weighting and range-setting resistors. All scale factors are accurately calibrated by computer-controlled automatic laser-trimming of the resistors while the device is operating – the key to its outstanding resolution and calibration accuracy, as well as its low price (\$39 in 100's).

The AD562 (Figure 1) accepts an external analog reference voltage (0 to +10V) and supplies a binary-weighted output current proportional to the product of the 12-bit digital input-code and the value of the reference voltage, which can be either fixed or variable. When the reference is fixed, the AD562 functions as a normal DAC. When V_R is a variable unipolar (0 to +10V) voltage, the device is a 2-quadrant multiplying DAC; the digital input code can be either unipolar (binary or BCD) or bipolar (offset binary).

Nominal full-scale output current (unipolar mode) is -2mA. Internally-trimmed gain-, voltage-range-, and bipolar-offset-resistors are incorporated, to provide precise voltage outputs via an external op amp. Since all voltage scale-factors rely on resistance ratios, their temperature coefficients are determined by tracking TCR's (about 1ppm/°C) rather than absolute TCR's (about -30ppm/°C). With $V_R = +10V$, the following voltage ranges can be pin-programmed (see Figure 5): 0V to +5V, -2.5V to +2.5V, 0V to +10V, -5V to +5V, -10V to +10V. The AD562's current output, when used with the internal ranging resistors, allows the device to be used as the D/A weighting element in both voltage-output DAC's and voltage-



input ADC's, with very low voltage-gain T.C., because these resistors track the other thin-film network resistors to better than $\pm 2\text{ppm}/^\circ\text{C}$.

Logic Inputs. The logic relationship is "positive-true": voltage above threshold ("1") turns a bit *on*; voltage below threshold ("0") turns it *off*. Logic drive currents are only -100 μA *max* at "0" and +100nA *max* at "1", values compatible with both CMOS and TTL logic. Pin 2 sets the internal logic threshold for the digital inputs, bits 1-12. When it is open-circuited, with $V_{CC} = +5V$, the threshold is approximately +1.4V, and the device is TTL-compatible. For CMOS, pin 2 is externally connected to pin 1; the internal logic threshold is thereby set at $\sim V_{CC}/2$, and the device is then fully compatible with both low- and high-voltage CMOS, over the range $+4.75V \leq V_{CC} \leq +15.8V$.

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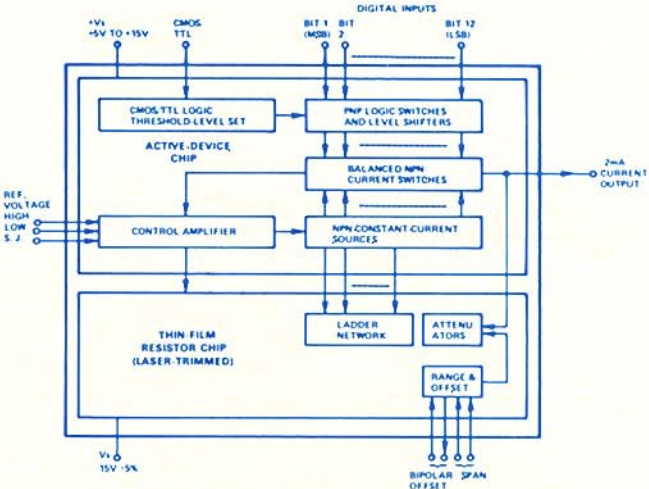


Figure 1. Functional block diagram of the AD562

*For complete information on the AD562, use the reply card. Request M1.

Coding. The various voltage ranges that can be pin-programmed are shown in Figure 5. For bipolar ranges, a fixed current is subtracted from the output current to offset it by half-scale, by the connection of the other end of the bipolar offset resistor (through an external trim pot) to V_R (Figure 2). Analog voltage zero occurs at digital code 1000 0000 0000 (2048/4096 of F.S. span) for binary models, and at 0101 0000 0000 (500/1000 F.S.) for BCD (binary-coded decimal) models.

CIRCUIT DESIGN

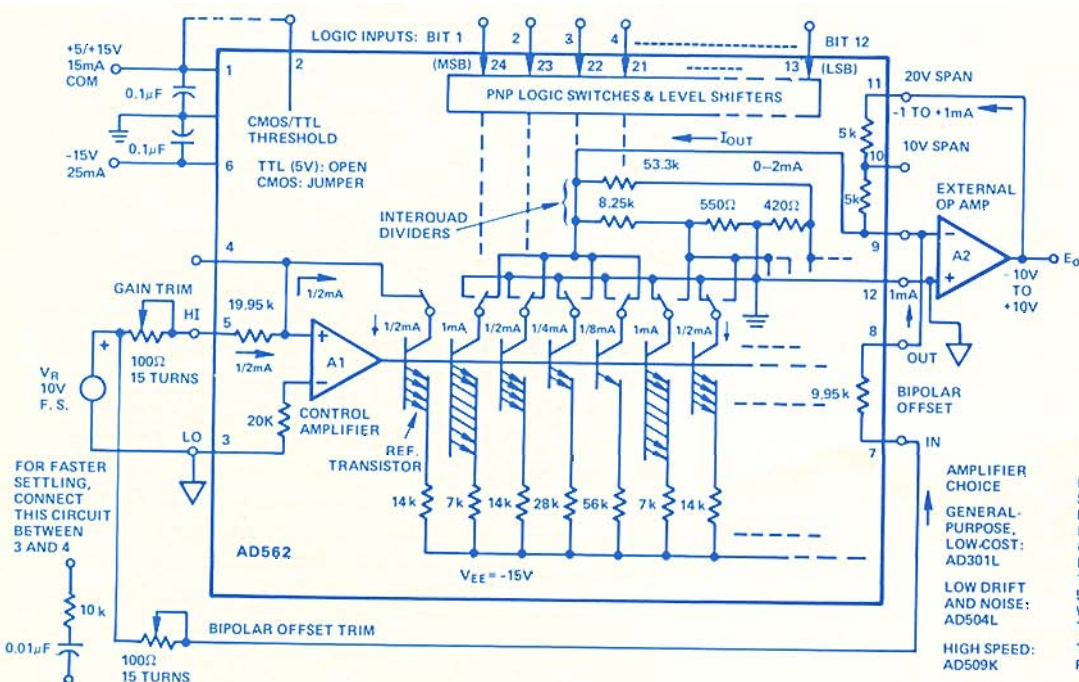
The AD562 current output is the weighted sum of the outputs of three similar groups of binary-scaled quad current-generators, controlled by V_R . The logic inputs steer these currents through non-saturating bipolar-transistor current switches to either ground or the respective quad output bus. Output currents from the 2nd and 3rd quads are attenuated (in effect) by 16:1 and 256:1 (binary; 10:1 and 100:1 for BCD), and summed with the unattenuated output of the first quad. The output current is thus the sum of 12 individually-switched currents having a binary relationship. Figure 3 shows the overall scheme; Figure 3 shows the simplified details of the control amplifier, constant-current transistors, and switching-cell interconnections.

The current-generating transistors (Q9, Q12, etc.) of each quad group have emitter areas in the ratio 8:4:2:1. The ladder-network resistances between the emitters of Q9, Q12, etc. and the -15V supply are in the ratio 1:2:4:8 (bits 1, 2, 3, 4 in the first quad). With equal voltages applied to the resistors, the emitter currents of Q9, Q12, etc., are therefore in a binary ratio. Because of their weighted emitter area, these transistors operate at equal emitter-current densities and therefore have nearly-equal V_{BE} 's and h_{FE} 's. The control amplifier (A1) drives the bases of the constant-current transistors and also a reference-transistor pair (Q2-Q1), which has h_{FE} and V_{BE} matched to those of the constant-current (Q9, Q12, etc.) and bit-switching (Q8, Q11, etc.) transistors.

V_R is applied to the externally-trimmed gain resistor R1 to set a reference current, $I_R = 10V/20k\Omega = 0.5mA$ F.S.). Amplifier A1 establishes the appropriate base voltage to force Q1 collector current equal to I_R . Variations in h_{FE} , V_{BE} , or supply voltage with time and/or temperature are sensed in the reference-transistor pair. The control amplifier then adjusts V_{BE} to hold Q1 collector current (and therefore the bit currents) constant in the presence of these variations. The use of Q1, Q2, and A1 reduces the net gain T.C. to a function of the differential h_{FE} and V_{BE} between the monolithically-matched reference- and bit-switching- pairs. This close match results in an overall transistor-contribution of $<1ppm/^{\circ}C$ to the gain T.C.

Output current (for example, Bit 1) is switched by steering Q9's collector current either to ground through Q7, or to the output through Q8. With Bit 1 *high*, Q5 is turned off, and I_O is steered through Q6; Q8 is turned on, Q7 is turned off, and Q9 collector current flows through the output. With Bit 1 *low*, Q6 is turned off, and I_O is steered through Q5; Q7 is on, Q8 is off, and the Q9 collector current flows to ground. This fully-differential switching takes place rapidly, since there is no change in steady-state voltage at the emitters of Q7-Q8, with a speed that is *nearly independent of the current level being switched*. (Switching speeds for most commercially-available DAC's vary significantly as a function of current level.) This feature is particularly useful in multiplier applications, which require fast switching at reduced (as well as full-scale) current levels, as a function of V_R .

The excellent V_{BE} match (to about 1mV) of Q2, Q9, Q12, etc., permits accurate multiplication (fast or slow) at reduced current levels (V_{BE} mismatch at these levels is the chief contributor to bit-weighting errors). V_{BE} mismatch among the output-current switch transistors, Q8, Q11, etc., which are cascode-connected, does not affect bit-weighting accuracy.



NOTES:
SINCE $I_{OUT} \geq 4 I_{REF}$, AND THEY TRACK QUITE PRECISELY WITH TEMPERATURE, EXTERNAL REFERENCE AND APPLICATION RESISTORS (THAT TRACK) CAN BE USED FOR OTHER REFERENCE VOLTAGES. FOR EXAMPLE, TO OBTAIN 10V OUTPUT USING THE 2.5V AD580, TWO EQUAL 5k Ω RESISTORS CAN BE USED AT PINS 4 AND 9, WITH APPROPRIATE FIXED TRIMS, TO REPLACE THE INTERNAL RESISTORS.
THE LOGIC INPUTS ARE PROTECTED AGAINST POWER-OFF DAMAGE.

Figure 2. Functional schematic of the AD562

Since the collector voltage of Q2, Q9, Q12, etc., does not change during bit switching, there is no differential power change as various bit combinations are switched. Moreover, the four most-significant current-setting transistors (Q9, Q12, Q15, Q18) are located on the axis of symmetry between Q7-Q8, Q10-Q11, etc., virtually freeing the device from nonlinearity and thermal-transient errors attributable to differential heating. Typical AD562 nonlinearity is, in fact, less than 30ppm F.S.

Q3 and diodes CR1 and CR2 form a bootstrapped bias source which causes the voltage V_C (very nearly equal to the collector voltages of Q9, Q12, etc.) to track the base voltage V_B . The collector-base voltage of Q9, Q12, etc., is thus maintained at approximately $3V_{BE}$, irrespective of supply- or reference-voltage variations (which are impressed across the switch transistors instead). Bootstrapping prevents h_{RE} effects from introducing errors into the bit currents and contributes to the AD562's excellent supply-voltage rejection and multiplier performance.

APPLICATIONS

Multiplication. As noted above, the AD562 can be used as a multiplying DAC. The analog input (V_R) must be unipolar (0 to +10V); the digital coding may be either unipolar (single

quadrant) or bipolar (2 quadrants). When V_R is +1V (10%F.S.), worst-case error is only about 0.05% of the (reduced) full-scale output. Settling time for a 10V-full-scale V_R step is 5 μ s to 0.01%, while the slewing rate is 1mA/ μ s (or 5V/ μ s with a suitable output amplifier providing a 0-10V range), with all bits on. Feedthrough of a full-scale (10Vp-p) sinewave, with all bits off, is 0.0125%F.S. at 2kHz, increasing at 20dB/decade at higher frequency.

12-Bit Successive-Approximations A/D Converter (Figure 4). The AD562 is shown here as the D/A weighing element in a 12-bit ADC, for conversion rates up to 40kHz. The digital output-equivalent of the analog input is formed by weighing the programmed DAC-output, one bit at a time (MSB first, LSB last), and accepting or rejecting each bit, depending upon the comparator state following each bit-trial. The analog input voltage is applied to the appropriate AD562 span resistor, and the current-output terminal (summing-point) voltage is compared against "ground." The AD562's output voltage is diode-clamped to keep the out-of-balance error voltage within the device's compliance-voltage limits. The AD562's multiplying capability permits the reference voltage to be varied for ratio-metric conversion.

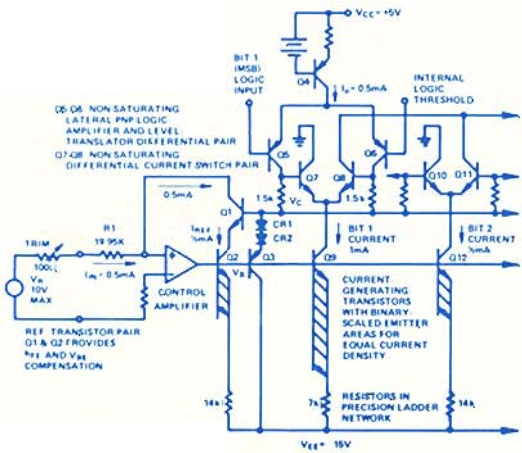


Figure 3. Control amplifier, current generators, and bit-switching cell structure

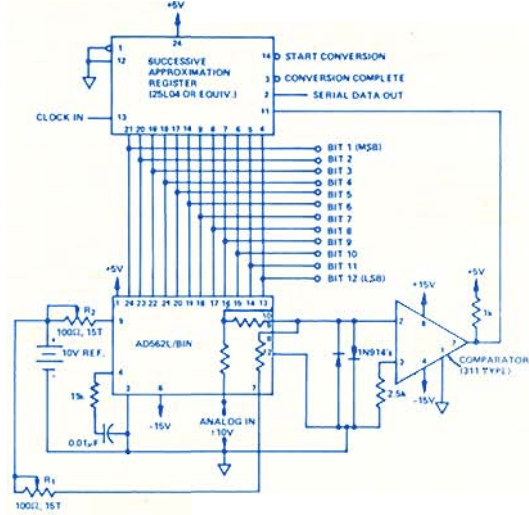


Figure 4. 12-Bit successive approximation A/D converter

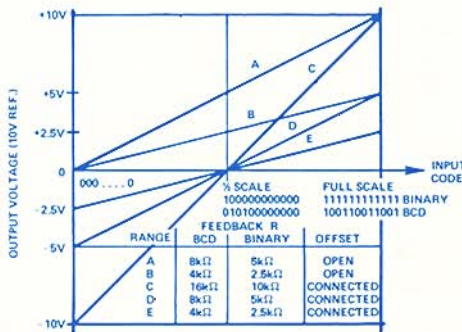


Figure 5. Voltage vs. digital input code for various connections of span and bipolar-offset resistors (10V reference).

BRIEF SPECIFICATIONS OF THE AD562

(Binary @ +25°C and 10V Reference, unless otherwise specified)

Data Inputs	TTL CMOS	(V_{CC} = +5V, pin 2 open) "1": $\geq 2V$ @ 100nA, "0": $\leq 0.8V$ @ -100 μ A (4.75V $\leq V_{CC}$ $\leq$ 15.8V, pin 2 tied to pin 1) "1": $\geq 70\%V_{CC}$ @ 100nA, "0": $\leq 30\%V_{CC}$ @ -100 μ A
Accuracy (error)		$\pm 1/2LSB$ max ($\pm 0.012\%$ F.S.)
Output Current	Unipolar Bipolar	0 to -2mA $\pm 10\%$ -1mA to +1mA $\pm 10\%$
Leakage (all bits off)		0.03% F.S. max
Output Compliance		+10V to -1.5V
Output Impedance		7.5k Ω $\pm 10\%$ in parallel with 33pF
Resolution		12 Bits
Gain Error		$\pm 1/2LSB$ max ($\pm 1/2LSB$ max, "S" grade) referred to F.S.
Settling Time to 1/2LSB		3.5 μ s max (current output), all bits "1" to "0" or "0" to "1" (1.5 μ s max with 0.01 μ F capacitor in series with 10k Ω connected between pins 3 & 4)
Major-Carry Switching Transient:		400ns to 90% complete
Power Requirement	V_{CC} : V_{EE} :	+4.75VDC to +15.8VDC @ 15mA -15VDC $\pm 5\%$ @ 20mA
Supply-Voltage Sensitivity:		1ppm F.S./% max, V_{CC} = +5.0V or +15.0V 2ppm F.S./% max, V_{EE} = -15V
Binary Options	AD562KD/BIN AD562AD/BIN AD562SD/BIN	AD562KD/BIN AD562AD/BIN AD562SD/BIN
Temperature Range, Operating		0°C to +70°C -25°C to +85°C -35°C to +125°C
Temperature Coefficients, Average		
Leakage Current		1ppm F.S./°C max
Bipolar Offset		4ppm F.S./°C max
Gain (excluding ref)		3ppm F.S./°C max
Differential nonlinearity		2ppm F.S./°C
Monotonicity		Guaranteed over operating temperature range
Reference Voltage		0 to +10V, Input Resistance: 20k Ω $\pm 10\%$

SPECIFYING AND MEASURING A LOW NOISE FET-INPUT IC OP AMP, THE AD514

by Bill Maxwell

The AD514* is a FET-input integrated-circuit operational amplifier designed to provide at low cost the benefits of moderately low drift and bias current, and a guaranteed peak-to-peak noise level at low frequencies, in the "1/f" region. The amplifier is designed for applications that call for high input impedance and low noise, where low cost is essential. Applications for which it is well-suited include ecg and ecg amplifiers, pH-electrode amplifiers, and long-term integrators. For such applications, low noise, with predictable characteristics, in the 0.1 to 10Hz band, is well-nigh essential. For the AD514L, maximum voltage noise of 5μV p-p is guaranteed by testing all units.

Since IC op amps with guaranteed low-frequency noise specifications have not until now been available in quantities and at prices that are conducive to high-volume usage, the decision to break new ground by making such an amplifier available has posed certain problems in the area of characterization, interpretation of specifications, and the design of on-line test equipment.

A BRIEF REVIEW OF NOISE

Since the statistical nature of noise is at the heart of these problems, it may be useful to review a few basic noise relationships¹, particularly as they pertain to op-amp performance. We are concerned here with the irreducible noise generated within the amplifier itself, excluding all external interference sources, such as the power supplies, associated components, and fields in the vicinity of the device, which might cause noise to be induced, coupled, or conducted into the circuit.

Like drift (itself partly a low-frequency noise phenomenon), noise originating within the amplifier may be referred to the input circuit. The three fairly-uncorrelated effects (in FET-input op amps at low frequency) are a noise voltage in series with either input and noise currents from both inputs to common. Voltage noise is amplified by the closed-loop gain (i.e., "noise gain") of the feedback-amplifier circuit; current noise develops voltage across impedances connected to the input terminals, and it may or may not be amplified, depending on the circuit configuration. In single-ended amplifier circuits, especially inverters, only one of the two current sources is usually of interest, since the other input is connected to a low impedance.

Though noise is random, and its value at any instant of time is unpredictable, most types of noise found in semiconductor circuits do have stationary properties, hence consistently-measurable amplitude distributions and frequency spectra. This means that noise in a given bandwidth can be characterized by its root mean-square (rms) value. Since noise from independent sources, and noises in different bands of the spectrum

(from the same source) are all uncorrelated, they may be combined by root sum-of-the-squares summation. For example, if the rms voltage noise in the band 10Hz to 100Hz amounts to 0.13μV, and the noise in the band 100Hz to 1kHz is 0.2μV; and if the noise generated in a signal source resistance is 0.41μV over the band 10Hz to 1kHz, the total rms input noise to the amplifier due to these sources will be

$$E_n = \sqrt{0.13^2 + 0.2^2 + 0.41^2} = 0.47\mu V \quad (1)$$

Note that the squaring causes the summation to be dominated by the largest term. Usually, we can neglect noise components less than 1/3 of the largest component (in this case, if we were to neglect the 0.13μV term, the sum would be 0.46μV).

RMS vs. "PEAK-TO-PEAK"

For many applications, especially in "one-shot" measurements at low frequency, rms noise is not very meaningful, because it represents the result of an averaging process. Rather, we might be concerned about the effects of instantaneous noise that occurs during the measurement. All values of noise are possible, but it can be shown that, for a "Gaussian" distribution (and many of the types we are concerned with can be assumed to have Gaussian amplitude distributions), the proportion of time occupied by peaks higher than a specified value decreases quite rapidly as a function of increasing peak amplitude. This can be shown graphically or in tabular form (Figure 1). For many practical purposes, the assumption that the largest peak-to-peak noise swing is 6.6x rms (0.1% probability) is quite tenable, and useful measurements can be made assuming even smaller ratios of peak-to-peak to rms.

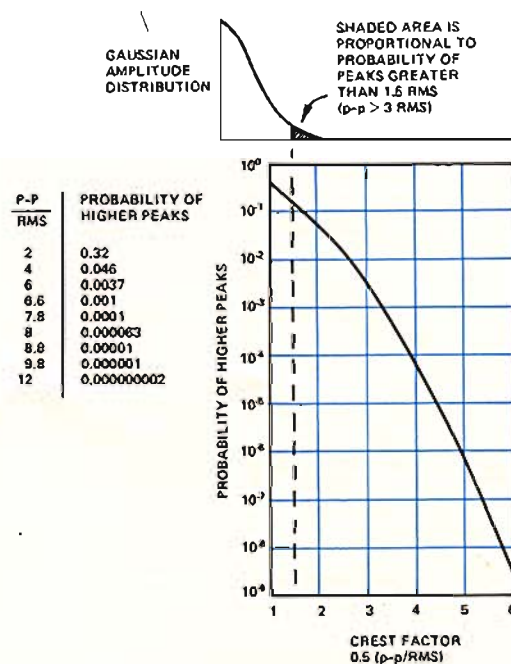


Figure 1. Crest factor of gaussian noise

*For technical data on the AD514, use the reply card. Request M2.

¹See also: *Analog Dialogue* 3-1, "Noise and Operational Amplifier Circuits." A useful book: *Low-Noise Electronic Design*, C. D. Motchenbacher and F. C. Fitchen, John Wiley & Sons, 1973; it contains a list of further references.

THE NOISE SPECTRUM

A plot of noise vs. frequency provides useful information (Figure 2), since it may be multiplied by circuit amplitude-response spectrum to obtain the output distribution of noise vs. frequency, and hence the resulting rms noise, in any band. The function that is plotted is called the *spectral density*, and it is plotted either in "power" form (e_n^2 , i_n^2), or in root-power form (e_n , i_n). If we consider the frequency range to be divided into a large number of infinitesimal frequency elements, df , then the rms noise over a given frequency band is equal to the square-root of the sum of the squares of the rms noise in each incremental band. The power spectral density is the limit of the ratio of each incremental mean-square noise contribution to the incremental band in which it occurs, in the vicinity of a frequency f . When expressed in "power" form, its dimensions are V^2/Hz or A^2/Hz ; in root form, they are $V/\sqrt{\text{Hz}}$ or $A/\sqrt{\text{Hz}}$.* To obtain mean-square noise over any bandwidth, we integrate this function over the frequency range of interest, that is

$$E_n^2 = \int_{f_L}^{f_H} e_n^2 df, \text{ or for rms, } E_n = \sqrt{\int_{f_L}^{f_H} e_n^2 df} \quad (2)$$

The value of e_n or i_n at a given value of frequency is called the "spot noise."

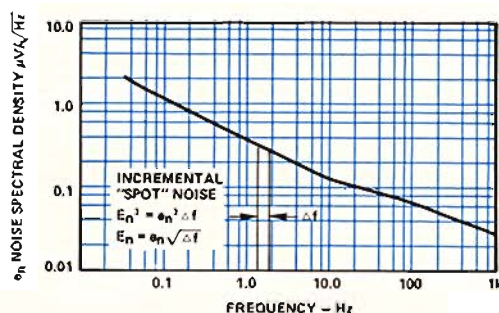


Figure 2. Voltage noise spectral density of typical AD514 operational amplifier

Despite its usefulness, the noise spectrum is difficult to acquire, even in the laboratory, especially at low frequencies, since a series of "spot" measurements generally involves small-signal amplification, narrow-band filtering, integration of the mean-square signal for a sufficient period of time (10x the lowest period for reasonable validity), and repeated measurements under carefully-controlled conditions. On-line testing under production conditions is even more difficult; it will be discussed shortly.

Though actual noise vs. frequency plots for devices do not have ideal shapes, there are certain approximate distributions that recur frequently over portions of the spectrum; they are: "white" noise (uniform frequency distribution, i.e., $e_n = \text{constant}$ or $i_n = \text{constant}$), and "1/f" noise (e_n^2 or i_n^2 inversely proportional to frequency, -6dB per octave, or e_n or i_n inversely proportional to the square-root of frequency, -3dB per octave). Over a band of frequencies, f_H to f_L , the results of integrating to obtain rms noise are:

$$\begin{aligned} \text{White noise} \\ (e_n \text{ constant}): \quad E_n &= \sqrt{\int_{f_L}^{f_H} e_n^2 df} = \sqrt{e_n^2 \int_{f_L}^{f_H} df} \\ &= e_n \sqrt{f_H - f_L} \\ &\cong e_n \sqrt{f_H} \end{aligned} \quad (3)$$

$$\begin{aligned} 1/f \text{ noise:} \quad E_n &= \sqrt{\int_{f_L}^{f_H} e_n^2(f_1) \frac{f_1}{f} df} \\ &= e_n(f_1) \sqrt{f_1} \sqrt{\int_{f_L}^{f_H} \frac{df}{f}} \\ &= e_n(f_1) \sqrt{f_1} \sqrt{\ln(f_H/f_L)} \end{aligned} \quad (4)$$

Here is an example: if the noise output of a given amplifier configuration is approximately "white" from 100Hz to 10kHz, with $e_n = 0.1\mu V/\sqrt{\text{Hz}}$, and "1/f" from 1Hz to 100Hz, with $e_n(10\text{Hz}) = 0.32\mu V/\sqrt{\text{Hz}}$, we can use root sum-of-squares summation of (3) and (4) to find the total rms noise in the band 1Hz to 10kHz:*

$$\begin{aligned} E_n^2 &= (0.1)^2(10)^4 + (0.32)^2(10)\ln(100/1) \\ &= 100 + \ln(100) = 105\mu V^2 \\ E_n &= \sqrt{105} = 10.2\mu V \text{ rms} \end{aligned}$$

First-order RC high-pass and low-pass filters are ordinarily used to limit bandwidth for measurements. Since their response is tapered to 6dB per octave, rather than "rectangular," they pass some out-of-band noise and attenuate some in-band noise, which may provide a value of measured rms noise that would differ from the results of measuring with a "perfect" filter. For white noise, a low-pass filter will have an equivalent cutoff frequency of $1/4RC$, instead of $1/2\pi RC$; the same is true for a high-pass filter at the low end, though f_L for broadband white noise is unimportant. For 1/f noise, the low-pass cutoff frequency and the high-pass cutoff frequency are both very close to $1/2\pi RC$.

"White" noise characterizes ideal resistors and junctions; for resistors, "Johnson" noise has the values, $e_n = \sqrt{4kTR} \cong 0.129\mu V/\sqrt{\text{Hz}}$ for $R = 1M\Omega$ @ $300^\circ K$, and $i_n = \sqrt{4kT/R} \cong 0.129pA/\sqrt{\text{Hz}}$, where k is Boltzmann's constant $= 1.380622 \times 10^{-23} J/^\circ K$, T is absolute temperature, and R is the resistance. For junctions, the shot noise, $i_n = \sqrt{2qI} = 5.7 \times 10^{-4} \sqrt{I}$ picoamperes/ $\sqrt{\text{Hz}}$, where I is the current flowing through the junction, in pA, and q is the charge on an electron, $1.6021917 \times 10^{-19} C$. This formula can be used to compute the limiting low-frequency current noise of a FET-input op amp, if I is the input leakage current. For example, if $I = 10pA$ (maximum specification for AD514L), $i_n = 5.7 \times 10^{-4} \sqrt{10} = 1.8 \times 10^{-3} pA/\sqrt{\text{Hz}}$, or $1.8fA/\sqrt{\text{Hz}}$.

In the frequency range below 100Hz, most amplifiers exhibit another noise component that dominates the Johnson and shot components and becomes the chief source of error at those frequencies. Dubbed "flicker noise," or "pink" noise, its power

(continued on page 19)

*You will find no consistent usage in the industry. Analog Devices generally uses the "root" form, $\mu V/\sqrt{\text{Hz}}$ or $pA/\sqrt{\text{Hz}}$. Be sure to check the scale calibration of any plots you may be dealing with.

*A powerful graphical technique can be found in *Analog Dialogue*, Volume 3, No. 1 (1969), pp. 11-12.

COMPARING THIN FILMS FOR PRECISION RESISTOR NETWORKS

ADI'S NICKEL-CHROMIUM FILM SYSTEM vs. TANTALUM NITRIDE

by Tom Parello and Dr. Carl Drumheller

For resistor networks, especially high-precision designs for use with op amps in analog data processing, thin-film monolithic construction is increasingly being preferred to matched assortments of wirewound and bulk metal-foil discrete resistors. The many reasons include the potentially high tracking accuracy of thin films, efficient use of space and weight, long-term stability, low cost per element, low noise, and high reliability, as well as the capability of employing standard IC packages and assembly techniques (including chips for hybrids).

The degree to which these advantages are realized depends on the characteristics of the film system and the process employed. In *Dialogue* 8-1, the technology used with a high degree of success and consistency at the Resistor Products Division of Analog Devices (RPD), was described in some detail. Elsewhere in this issue, a few members of a new line of standard resistance networks for use by circuit designers are introduced.*

The key to the excellent overall results obtained with these networks is the nickel-chromium (NiCr, "Nichrome") film system. While comparison of NiCr thin films with discretes can easily be performed by even an unsophisticated designer, and the literature is replete with comparisons between thin- and thick-film networks, there has been little discussion about thin-film alternatives. It is our purpose here to compare NiCr with the principal commercially-available alternative, various forms of tantalum, and particularly tantalum nitride (Ta_2N), in terms of properties of interest to the circuit designer.

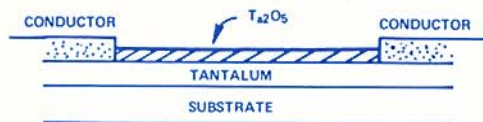


Figure 1. Tantalum pentoxide-tantalum film system

TANTALUM FILMS

Pure tantalum, while highly stable in adverse environments, and successfully employed in such devices as film capacitors, is unsuitable for high-precision resistor networks because of the low sheet resistivity and high temperature-coefficient of resistivity (TCR) of sputtered tantalum films. As Figure 1 shows, one approach to precision adjustment is to convert a portion of the tantalum to an insulating layer of tantalum pentoxide (Ta_2O_5), by a "wet-jell" anodizing process, thus increasing the sheet resistivity of the film and allowing some control over the resistance values. The process is slow and cumbersome, and large investments in special process equipment are required to build precision devices in volume.

*For information on resistance networks, use the reply card. Request M3 for standard networks for op amps and converters; request M4 for custom networks.

The method principally employed, which provides a usable range of sheet resistivity and TCR, is to sputter tantalum in the presence of nitrogen, forming a mixture of Ta, Ta_2N , and interstitial nitrogen. This complex system is better than tantalum, but at the expense of its thermodynamic stability, which limits its useful range of resistivity to about $100\Omega/\text{square}$ for applications requiring high stability. Also the difficulties of precise process control in forming so complex a film make it hard to keep film TCR's within a narrow range. Though it is possible to achieve quite low TCR's, the practical range of TCR's is about -50 to $+200\text{ppm}/^\circ\text{C}$ (Figure 2).

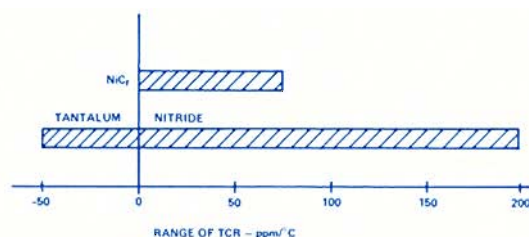


Figure 2. Comparison of temperature coefficient of resistance — tantalum nitride vs. nickel-chromium

CHROMIUM AND NICKEL-CHROMIUM

Pure chromium films encounter problems similar to the Ta films. If the Cr films are partially oxidized during deposition, problems similar to those existing with tantalum nitride films occur because of the interstitial problem. The solution, nickel-chromium (NiCr) films, eliminates the disadvantages of pure chromium and offers a wide range of parametric advantages over other systems. The NiCr films deposited by RPD are extremely stable alloys of nickel and chromium that are simpler to work with than the Ta_2N system. Since the long-term stability of NiCr films is generally over an order of magnitude better than for Ta_2N films, the design and production range of NiCr films can be quite wide. Figure 3 indicates qualitatively the limited range of film thickness available for usable sheet resistivity values. With NiCr, the available range of stable sheet resistivities (i.e., the vertical scale) is considerably greater than for Ta_2N .

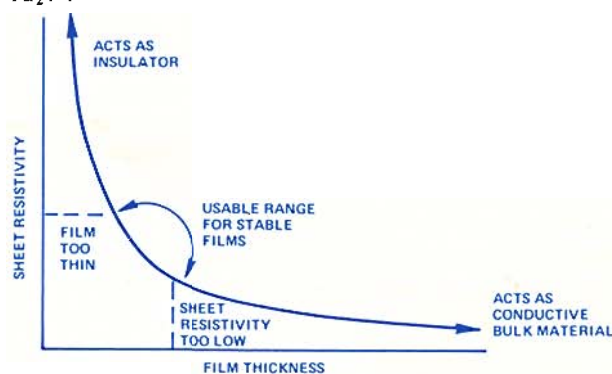


Figure 3. Qualitative relationship between sheet resistivity and film thickness

COMPARISON

In comparing the properties of the two materials more specifically, it will become apparent that, though Ta₂N is usable in many applications, NiCr is better where long-term power stability, precision, and low-noise are necessary, combined with a high degree of device-design flexibility.

SHEET RESISTIVITY RANGE – Perhaps the key specification for a resistive film system is the sheet resistivity, in Ω/square. The wider the range of controllable sheet resistivities, the greater the range of circuit applications and the better the packaging density. Figure 4 compares Ta₂N and NiCr in this respect. The “figure of merit” is a composite qualitative representation of manufacturability, stability, and ease of use. Usable NiCr sheet resistivities range from below 50 to about 500Ω/square; for Ta₂N, the range is about 25 to 125Ω/square.

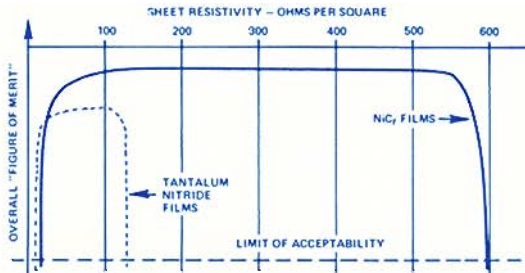


Figure 4. Comparison of overall suitability as a function of sheet resistivity – tantalum nitride vs. nickel-chromium

This flexibility of NiCr permits design of such products as the DIL-packaged AD1803 decade divider, which contains resistors ranging from 100Ω to 9MΩ, using a single reliable film deposition (see page 13). Other devices having essentially order-of-magnitude sheet-resistivity-range, but identical geometries, can be processed with no basic changes in the fabrication cycle.

ETCHING – In high-resistance applications, the higher the sheet resistivity, the wider the lines can be, with better yields and electrical tolerances, hence lower cost. Yields can drop disproportionately as linewidth decreases (and length increases), because of the increased importance of substrate and mask defects.

FILM STABILITY – For the majority of applications, the designer would like to see the properties of a network unchanged over a long period of time. Though all films drift to some extent, the striking contrast between Ta₂N and NiCr can be seen in Figure 5.

TRIM TECHNIQUES – Both film systems can be “tweaked” by diamond scribing, abrasive trimming, electrical pulse trimming, and laser trimming. Ta₂N can also be trimmed by anodizing. However automatic laser trimming is rapidly becoming the preferred method. With the NiCr system, the resistance values - - starting with a given set of masks and basically the same process - - can be adjusted, first by choice of sheet resistivity (50-500Ω/square), then by coarse trimming (several orders of magnitude possible), then by fine trimming to within tolerances approaching 0.001% or better, in production quantities.

NOISE – In addition to basic Johnson noise, resistors may have “excess” flicker and shot noise (see preceding pages). Flicker noise, due to fluctuations in resistivity (related to carrier path) can be significantly in excess of Johnson noise in Ta₂N because of the complex granular and interstitial structure. Shot noise, due to fluctuating carrier densities (generally found in semiconductors), may also be present in negative-TCR films, which are common with Ta₂N. On the other hand (Figure 6), NiCr films are among the lowest-noise resistance materials available today. Excess noise of -50dB (1/300) for a 10kΩ resistor, measured on a Quan-Tech test set, is typical. The advantages for low-level “front-end” applications is evident.

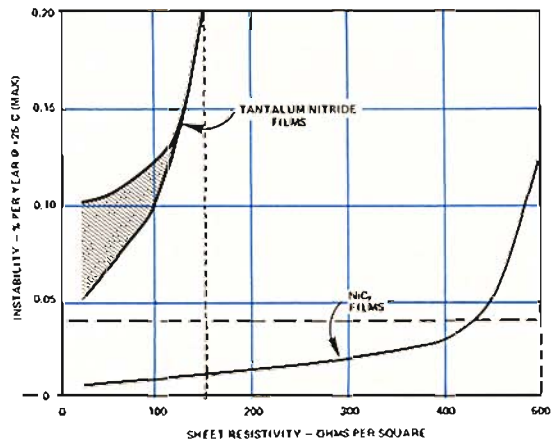


Figure 5. Comparison of drift stability (at about 10W/in² applied power-density) of tantalum nitride and NiCr resistance films. One year at +25°C ambient is considered equivalent to 250-500 hours at +125°C.

TEMPERATURE COEFFICIENT OF RESISTANCE – In solid-state components, poor noise performance is often accompanied by high TCR's (or vice versa), since similar mechanisms contribute to the measured effects. Ta₂N films generally exhibit widely-varying TCR's (Figure 2). High accuracy over wide temperature ranges is difficult to achieve when the film system can contribute errors of up to 0.02%/°C.

ENVIRONMENTAL CONSIDERATIONS – Under adverse conditions, Ta₂N does offer some advantages, since it is somewhat moisture- and abrasion-resistant, due to the thicker oxide layers that are formed when it is anodically trimmed. However, such conditions are no problem for NiCr with appropriate production methods and packaging techniques (e.g., in hermetically-sealed IC packages). Thin-film microcircuits with NiCr resistors are among the highest-reliability, Class 1 components in our most-stringent military systems. ▶▶▶

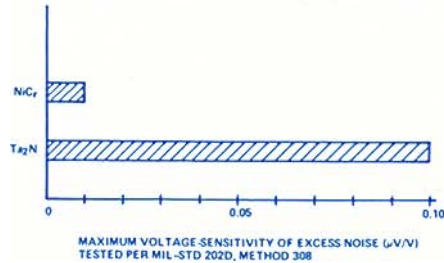


Figure 6. Comparison of excess-noise sensitivity of tantalum nitride and nickel-chromium

TWO FET-INPUT OP AMPS AND A POWER SUPPLY

1 μ V/ $^{\circ}$ C FET-OP AMP

$E_n < 1.5\mu$ Vp-p (0.01-1Hz)

The Model 52* is a high-resolution operational amplifier designed for handling signals characterized by low voltage or current with little added noise, or higher voltages and currents with improved accuracy. Contributing to its low uncertainty are these guaranteed specs

- Low noise, 1.5 μ Vp-p max, 0.01-1Hz
- High CMR, 100dB min, ± 10 V CMV
- High gain, 120dB min
- Low input current, 3pA max
- Low offset voltage, 500 μ V max

plus low drift, 1 μ V/ $^{\circ}$ C max (Model 52K). Its offset can be adjusted to zero by a 3-point adjustment that doesn't affect the temperature coefficient.

The FET input allows the Model 52 to handle low-level signals from high-impedance sources with low drift and noise contributions by the amplifier's voltage and current errors, with up to 5M Ω of source impedance. In many applications, the thermal noise of the source resistance will itself be the major contributor to voltage noise.

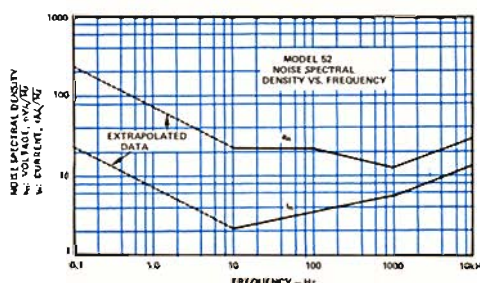
Applications for which these characteristics are especially beneficial include current measurement, charge amplification, buffer amplifiers, high-performance low-frequency filters, instrumentation pre-amplifiers, long-term integration, and high-precision analog computation.

The figure shows noise spectral density plots of both voltage and current noise. For further information on the meaning and use of spectral density plots, see pages 6 and 7, this issue, or *Analog Dialogue*, Vol. 3, No. 1.

Frequency response is 500kHz (small-signal, unity-gain bandwidth) and 4kHz min full-power bandwidth. Slewing rate is 0.25V/ μ s min, with 150 μ s settling time to 0.01%.

Model 52's two versions, J/K are nearly identical, distinguished only by the drift spec (3/1 μ V/ $^{\circ}$ C max). Available from stock, in 1-1/8 x 1-1/8 x 0.4" (28.4 x 28.4 x 10.2mm) modules, their prices are \$42/\$49.

*For data on the model 52, request M5.



HOW ARE YOU FIXED FOR POWER SUPPLIES?

MODEL 921: ± 240 mA @ ± 12 V

Just about every application for the products described in these pages requires a power supply. Yet the glamour of some of our other devices makes it easy to forget that Analog Devices also provides a line of power supplies with ratings from 5 to 24V and 25mA to 1A, intended to energize our op amps, converters, logic circuits, as well as other devices, efficiently, reliably, and at low cost.

An example of a power supply designed for systems involving numbers of IC op amps is the new 921,* which makes available 240mA at both + and -12V, with 0.02% max regulation (line and load), 0.5mV ripple and noise, and 0.015%/ $^{\circ}$ C sensitivity, combined with current-limited short-circuit protection. Specified for 105-125VAC @ 50-400Hz, and operation at temperatures from 0 to +70 $^{\circ}$ C, Model 921 measures 3 1/2" x 2 1/2" x 1 1/4" (89 x 63.5 x 32mm) and weighs only 18 oz. (1/2 kg). Price is \$69 (1-9).



*For information on ADI power supplies, including the 921, request M6.

FAST FET 250ns TO 0.05%

Model 51, a variant of Model 50*, recently introduced in these pages, is a fast, FET-input operational amplifier with 100mA @ ± 10 V output capability. Full output power is available at frequencies as high as 6MHz, with a minimum slewing rate of 400V/ μ s (inverting) and settling time of 250ns max to 0.05% of full-scale output. Small-signal gain-bandwidth is 80MHz, and a load of 100pF can be driven stably (inverting) without extra compensation or isolation.

Reliable operation is insured by protection against output short-circuits to ground. Its semiconductors are all hermetically-sealed metal-can types. It will operate at temperatures from -55 $^{\circ}$ C to +100 $^{\circ}$ C, and the 51B maintains the 20 μ V/ $^{\circ}$ C drift specification from -25 $^{\circ}$ C to +85 $^{\circ}$ C. Bias current at +25 $^{\circ}$ C is less than 2nA, and difference current is less than 100pA.

APPLICATIONS

Fast settling time makes the Model 51 ideal for high-speed buffer applications and as an output amplifier for D/A converters. The fast slewing rate is useful in video pulse amplification, CRT deflection applications, and wideband current boosting.

Of special value is the 51's ability to attain its maximum slewing rate with only slightly more than 1V of input. This permits it to provide fast pulse response and settling time, even in amplifier-with-gain configurations. For example, when compared with the Model 46, an amplifier that develops a slewing rate of 1000V/ μ s, but only at full input, the Model 51 is twice as fast, in a gain-of-4 inverting configuration, with a risetime (10%-90%) of 18ns, compared with 38ns for Model 46.

Model 51 is available from stock in two versions, A/B, which differ only in drift specifications, 50/20 μ V/ $^{\circ}$ C max, and in price, \$99/\$119 (1-9).



*For complete information on models 50 & 51, request M7.

DUAL SLOPE CONVERTER AND A DPM

VERSATILE A/D

WITH RATIOMETRIC CAPABILITY

CAN READ OUT IN ARBITRARY PHYSICAL UNITS

3½ DIGIT DPM USES 5 VDC OR AC-LINE POWER

The ADC1105* is a high-resolution dual-slope analog-to-digital converter designed for use with external counters and registers. With it, the designer can build conversion systems that utilize any desired counting scheme, with resolutions up to and including 4 BCD digits (or 14 binary bits), plus 100% overrange, plus sign. This versatility is especially useful in instrumentation applications for which it is desired to have outputs scaled directly in terms of engineering or physical units (e.g., pounds and ounces, as exemplified below).

Performance specifications include $2\mu\text{V}/^\circ\text{C}$ zero stability, $5\text{ppm}/^\circ\text{C}$ gain sensitivity (ADC1105K), and $15\text{ppm}/\%\Delta V_s$ power-supply sensitivity. The ADC1105 is available in two versions (J/K), distinguished by relative accuracy (error $<0.1\%/0.02\%$ of reading ± 1 count), gain stability ($10/5\text{ppm}/^\circ\text{C}$), reference stability ($20/5\text{ppm}/^\circ\text{C}$), and price (\$209/\$159, 1-9).

Physically, it is an encapsulated module $4.01'' \times 2.01'' \times 0.61''$ ($102.4 \times 51.1 \times 15.5\text{mm}$) max, also available with a mounting card, \$40 additional (1-9).

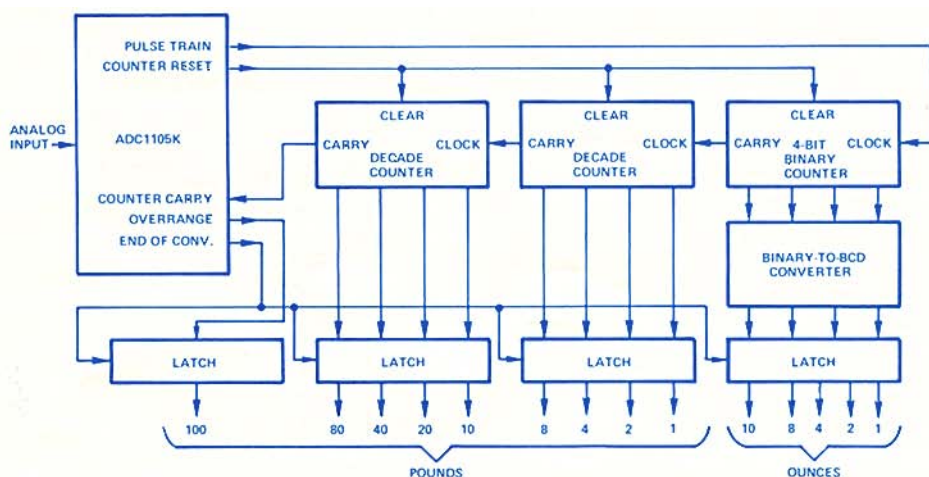
The ADC1105 is compatible with DTL, TTL, and even some forms of RTL. It can be configured to perform conversions on

command or automatically, at a rate controlled by simple external circuitry. Input ranges of $\pm 10\text{V}$ or $\pm 1\text{V}$ are available, with 100% overrange capability. The output of its dual-slope conversion circuit is a train of pulses, proportional in number to the analog input voltage. All of the signals needed to control the external counters and registers properly are provided.

TYPICAL APPLICATION

The simplified illustration shows a basic configuration that can be used for readout in engineering units. In this case, the output from the load cell in a weighing system is converted to a latched BCD output reading for display in pounds and ounces (199 lbs. 15oz max), a readout problem that is peculiar to some non-metric countries, such as the U.S.

The 0 to 15 count, which corresponds to the number of ounces, is implemented with a 4-bit binary counter and a binary-to-BCD converter. The $2\frac{1}{2}$ digits corresponding to the number of pounds are generated by two decade counters and the overrange output. The number of automatic conversions per second (from 0.2 to 260) is controllable by an external connection.



*For complete information on the ADC1105, request M8.



The AD2006* was introduced in *Dialogue* (7-2) as a "versatile" ac-line-operated digital panel meter. As a further enhancement of its versatility, it is now offered with a choice of either line power or +5VDC.

The primary benefit of this new option (AD2006/D) is the availability of a 5V-powered DPM with the large, bright, Beckman gas-discharge display. The circuit techniques required for excitation of the display also make available the $\pm 15\text{V}$ outputs for accessory circuitry (such as op amps) that are characteristic of the line-powered versions.

The AD2006D also provides the user with a third choice of readouts available on a 3½-digit 5V-powered DPM. It joins the AD2010,† with its all-solid-state LED (light-emitting diode) readout, and the AD2003,† with its incandescent Numitron display, which can be filtered for color-coded readouts. All three models have similar case designs, and they fit in the same front-panel cutout, but they do differ in depth behind the panel. Price of AD2006/D is \$179 (1-9).

EDGE-CONNECTOR OPTION

Another newly-available DPM option is the edge-connector-compatible version, with card-edge fingers (AD2006/C and AD2003C), available at no extra cost, and compatible with all other versions. Designed for convenience in readout-only applications, it replaces the 3M multipin connector, which is more suitable for the ribbon or flat woven-cable generally used in data-acquisition systems.



*For complete information on the AD2006, including the new options, request M9.

†For information on these Models, request M10.

TWO NEW ANALOG INTEGRATED CIRCUITS

FAST FET OP AMP

The AD528* is a FET-input integrated-circuit operational amplifier that combines the advantages of high slewing rate (50V/ μ s/min) and wide bandwidth with the high input impedance and low bias current that are inherent in FET-input designs. Despite its high speed, it is stable without external compensation; in fact, its phase margin is 60° at the unity-gain frequency, 10MHz, uncompensated.

However, specialized jobs call for versatile open-loop characteristics. For this reason, a compensation terminal has been provided to permit (for example) feedforward compensation, for nearly double the slewing rate and bandwidth. Or, if fast settling to within 0.1% is desired, a single compensation-capacitor may be used to optimize settling time.

High-speed performance is complemented by the open-loop dc gain of 50,000, offset voltage less than 1mV, drift less than 25 μ V/°C, and bias current less than 15pA, fully warmed up at +25°C (AD528K). It is, of course, a differential amplifier, with common-mode rejection of 80dB minimum at low frequencies. Typical applications of this versatile amplifier include sample-and-hold and peak-follower circuits, charge amplifiers, analog pulse amplifiers, and d/a and a/d conversion, as well as buffer amplification and filtering.

The basic AD528 is available from stock in three models, all having similar dynamic performance, but differing in dc characteristics and/or temperature range: the AD528J and AD528K, for operation at 0 to +70°C, and the AD528S, for operation from -55°C to +125°C. Minimum gains of J/K/S are 25,000/50,000/50,000; initial offset voltages 3/1/1mV max; voltage drift 50/25/25 μ V/°C max; warmed-up 25°C bias current at worst input 30/15/15pA max; CMR 70/80/80dB minimum. All types are housed in the TO-99 can. Prices (in 100's) are \$12 (J), \$16 (K), \$28 (S).



*For complete information on the AD528, use the reply card. Request M11.

LOW COST VOLTAGE REFERENCE FOR ANALOG CIRCUITS

The AD580* is a 3-terminal monolithic integrated circuit that accepts "upstream" voltages from 4.5V to 30V, and provides a steady low-impedance output of 2.5V ($\pm 2\%$ to $\pm 3\%$) at currents up to (and beyond) 10mA. Temperature coefficient is less than 40ppm/°C, long-term stability is 25 μ V/month (AD580K), and dc output resistance is 1 Ω . Cost, in the hermetically-scaled TO-52 can, is a low \$2 (AD580J, 100's).

APPLICATIONS

Perhaps a majority of analog circuit designs have a terminal variously designated as V_R , V_{REF} , E_{REF} , +10V, etc., at which a constant input voltage is destined to appear. It might serve the function of a constant bias; an additive constant in an equation; a scale-factor setting for a multiplier or divider; or as a reference voltage for a d/a or an a/d converter, a digital panel meter, or some other subsystem.

How is the reference voltage developed? Classically, it can be done in several ways:

- Derived from a power-supply voltage. This requires a stable source of system dc power (which might be expensive if loads are heavy), or an auxiliary supply for reference purposes (also costly).

- Developed across a zener diode or an IC zener-diode substitute. While it is possible to obtain stable reference diodes at reasonable cost, their internal resistance makes it essential that the load be either isolated by a buffer amplifier or essentially constant. In addition, a high quiescent current is necessary if a range of load currents are to be handled. The few available IC zener-diode substitutes answer some of the objections to zener diodes, but they are expensive and have accuracy and temperature-tracking problems because their internal resistors are of the high-TEMPCO diffused type.

The AD580 is a new (and to a great extent, irresistible) option: it can be used (without any external elements) to step down any arbitrary supply voltage to a

constant 2.5V output level. Its 1½mA quiescent current drain minimizes its loading of the supply. Its 4.5V minimum supply voltage spec allows it to work even from a logic supply (for DPM reference). It may be used singly, to supply up to 10mA (more through the use of a booster op amp); or several units might be used in a system, with appropriate calibration. Performance is excellent, partly because of the use of low-TC thin-film resistors deposited on the chip. The "K" version has a 40ppm/°C temperature sensitivity, and there is the definite promise of units having greatly-improved performance as this product-concept matures.

HOW IT WORKS¹

The AD580 is a "band-gap" reference system consisting basically of a transistor-pair with an emitter-area ratio of 8:1, a feedback amplifier, and a set of resistors having predetermined ratios (see simplified schematic). The amplifier acts to maintain its net differential input voltage at zero, and the emitter currents at equality, by manipulating the base voltage via the divider R_5 - R_6 . Since V_{BE} and ΔV_{BE} are both linear with temperature, as shown by the equations, voltage V_Z can be maintained at the "extrapolated band-gap voltage," V_G , independently of temperature.



SIMPLIFIED EQUATIONS

$$V_{BE} = V_G - 0.002T = 1.205 - 0.002T \text{ (VOLTS)}$$

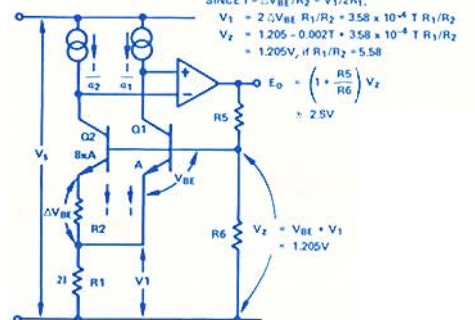
$$\Delta V_{BE} = 8.62 \times 10^{-5} T \ln \frac{A_2}{A_1} = 1.79 \times 10^{-4} T \text{ (VOLTS)}$$

$$\text{SINCE } I = \Delta V_{BE} / R_2 = V_1 / 2R_1$$

$$V_1 = 2 \Delta V_{BE} R_1 / R_2 = 3.58 \times 10^{-4} T R_1 / R_2$$

$$V_Z = 1.205 - 0.002T + 3.58 \times 10^{-4} T R_1 / R_2$$

$$= 1.205V, \text{ if } R_1 / R_2 = 5.58$$



*For information on the AD580, request M12.

¹A paper detailing the design of the AD580 is expected to appear in the December, 1974 issue of the *IEEE Journal of Solid-State Circuits*.

STANDARD THIN FILM RESISTOR NETWORKS FOR HIGH ACCURACY DESIGNS WITH OP AMPS AND SWITCHES

It is a truism that even modest operational amplifiers have behavior so closely approaching the ideal that gain accuracy of op amp circuits is largely limited by the associated circuit elements. Since gains are usually controlled by resistance ratios, a portion of the circuit-design effort involves the choice of resistors. Recently, thin-film resistor networks in standard IC packages (or in chip form) have become available at low cost in arrays that will suit a substantial variety of analog circuits.

The circuits shown here* are representative examples chosen from among the numerous high-precision nichrome thin-film resistor networks manufactured by the Resistor Products Division of Analog Devices, which already has a history of solid achievement in the manufacture of the more-complicated networks for converters,† custom circuitry,§ “precircuits”, hybrids, as well as the all-important substrates themselves,‡ including a large number of units purchased to MIL-STD-883.

WHY THIN-FILM NETWORKS?

In addition to excellent resistance-matching (to better than 0.01%), temperature tracking (to better than 2ppm/°C), and uniform behavior, which are usually more important than absolute resistance value alone, the small size of monolithic (single-substrate) devices tends to maintain all resistors at the same ambient temperature, despite external gradients.

Thin-film networks are convenient: the entire network can be specified, purchased, and used as a single component (like an IC), simplifying the process of buying, testing, keeping-track-of, and assembling matched elements. Their initial moderate cost, plus the savings in purchasing, inventory, assembly, and test, make these thin-film networks highly competitive with

do-it-yourself resistor assemblies, even in some lower-performance applications.

AD1830: 7 EQUAL INDEPENDENT RESISTORS in 14-pin DIP or Flatpak. Choice of 13 standard values from 50Ω to 500kΩ, absolute accuracies within ±1% to ±0.01%. Prices start at \$3.00 (100's).

AD1805: DUAL DIVIDER—4 EQUAL INDEPENDENT RESISTORS ratio-matched in pairs in TO-99 can. Choice of 7 standard values from 2kΩ to 200kΩ, ±1% to ±0.01% ratio match, ±1% absolute for reference. Prices start at \$1.90 (100's).

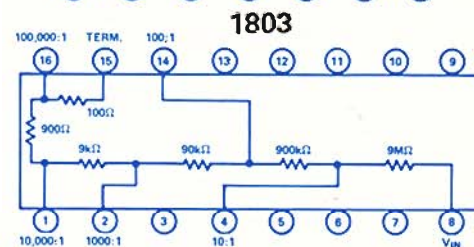
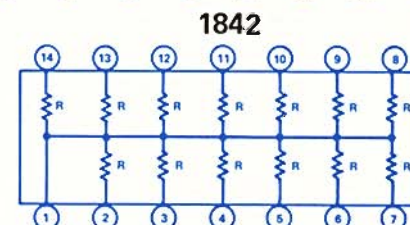
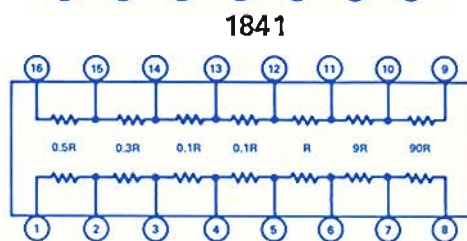
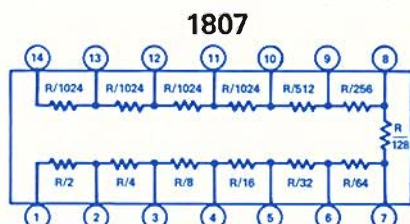
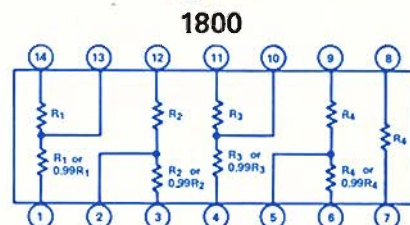
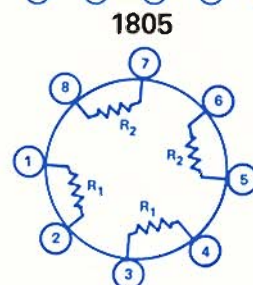
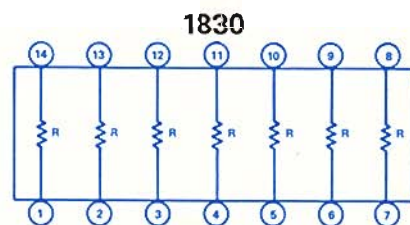
AD1800: QUAD DIVIDER—4 RATIO-MATCHED RESISTOR PAIRS with choice of equal values or 0.99 ratio (to permit external trimming to compensate for switch or source resistance) in 14-pin DIP. Choice of 7 standard values from 2kΩ to 200kΩ, ratio match ±0.01% to ±1%, absolute ±1%. Prices start at \$3 (100's).

AD1807: BINARY RATIO NETWORK—Arbitrary gains or attenuations programmable by external shunts in 10-bit (1/1024) steps. Choice of 7 standard resistance levels from 10kΩ to 1MΩ. Prices start at \$5.20 (100's).

AD1841: MATCHED DUAL NETWORK—2 IDENTICAL SETS OF 7 RESISTORS WITH 900:1 MAX RATIO in 16-pin DIP. Choice of 4 standard resistance levels for reference, from 1kΩ to 10kΩ. Prices from \$4.40 (100's).

AD1842: SUMMING NETWORK WITH 13 IDENTICAL RESISTORS in 14-pin DIP or Flatpak. Choice of 12 standard resistance levels, from 50Ω to 250kΩ. Prices from \$4.30 (100's).

AD1803: DECADE DIVIDER NETWORK WITH 10⁵ MAXIMUM RATIO (1MΩ to 100Ω) in 16-pin 0.9 x 0.5 x 0.15" (23 x 13 x 4mm) dual in-line package. Ratio accuracies from ±0.01% to ±1%, tracking TCR 5ppm/°C max. Prices start at \$5.75 (100's).



*For complete information on these circuits, request M3.

†For information on converter networks, request M3.

§For information on custom circuits, request M4.

‡For information on substrates and precircuits, request M4.

NEW ANALOG CMOS SWITCH ARRAYS: 5 INDEPENDENT SWITCH CONFIGURATIONS, 3 MULTIPLEXERS

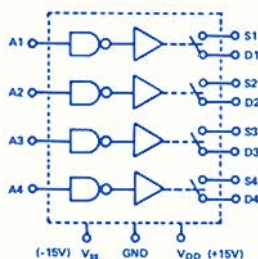
In *Dialogue 7-2*, three CMOS (complementary symmetry metal-oxide semiconductor) switch configurations were introduced: the AD7510* quad switch (4 independent switches), the AD7501* 8-channel multiplexer, and the AD7502* 4-channel differential multiplexer. Their acceptance was quite encouraging, but there were the inevitable requests for different configurations, for modifications of existing types, and for a superior second source of types already on the market.

In response to these express needs, and in consonance with our goal of market leadership, we have introduced 8 new CMOS switch configurations.*

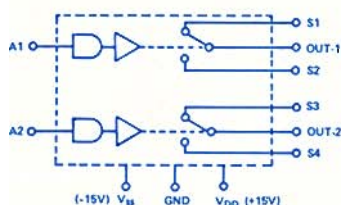
CMOS ANALOG SWITCHES

CMOS is well-suited to analog switching. One reason is the high impedance of CMOS, both in the open condition, and between the drive circuit and the switched circuits. At low frequencies, especially, the isolation is excellent. In addition, the switched path is essentially a (low) resistance, free of offset voltages. Finally, CMOS switches draw negligible power in the quiescent state and little more during switching; their load on the switching signal is also negligible.

7511



7512



AD7511 QUAD SWITCH

The AD7511 is identical to the AD7510, but its inverted logic allows external gates to be avoided. In 16-pin ceramic or plastic DIP. Prices (1-49) are as low as \$8.

AD7512 DUAL S.P.D.T. SWITCH

A SPDT variation of the AD7510, the AD7512 needs no external busing. It is TTL/DTL/CMOS-compatible, with 30μW dissipation and <100Ω R_{ON}. Available in 16-pin ceramic or plastic DIP. Prices (1-49) start at \$8.

AD7513 DUAL SWITCH (DG200)

Available in a 10-lead TO-100 can or 14-pin plastic DIP, the AD7513 is pin-for-pin compatible with the DG200, but has less power dissipation, no latchup for switch currents >5mA, no damage up to 50mA continuous, 150mA surge. \$4.80 (1-49)

AD7516 QUAD SWITCH (CD4016A)

Available in 14-pin ceramic or plastic DIP, the AD7516 is pin-compatible with the CD4016A, but has lower R_{ON} (<400Ω vs. 850Ω) at zero volts. \$2.43 (1-49)

AD7519 QUAD CURRENT SWITCH (20ns!)

The AD7519 steers current from 4 independent sources into one or the other bus line at ground or op-amp virtual ground. Operates from a single supply, drawing 8μW at 7.5 to 10V. Plastic DIP, \$5 (1-9).

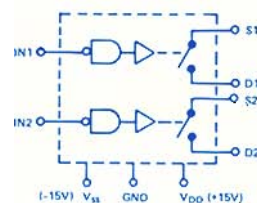
AD7503 8-CHANNEL MULTIPLEXER (HI1818)

The AD7503, available in ceramic or plastic 16-pin DIP's, is a replacement for the HI1818, with 1/10 the standby current (<0.1mA). It operates on ±15V supplies (vs. ±12V). Prices start at \$18 (1-49).

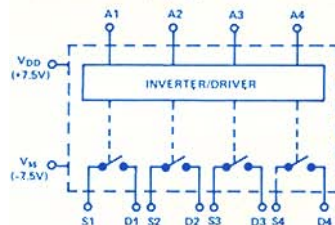
AD7506/7507 16-SWITCH MULTIPLEXERS

The AD7506 is a 16-channel multiplexer; the AD7507 is a differential 8-channel multiplexer. Pin-compatible with DG506/507, they have lower standby supply current and are latchup-free for switch currents >1mA. Package is 28-pin ceramic or plastic DIP; prices start at \$26 (1-49).

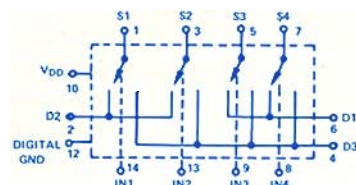
7513



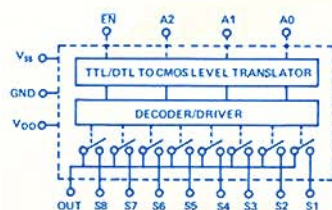
7516



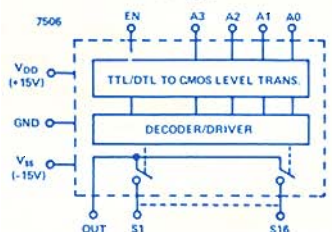
7519



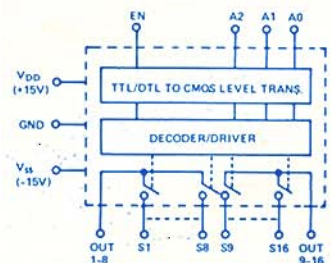
7503



7506



7507



*For complete catalog information on switches, request M13. For data on specific types, list them on the reply card.



DAC SETTLES FAST: 0.2% IN 30ns, 0.05% IN 60ns



The DAC1106* is a fast, adjustment-free D/A converter, with a 10ppm/°C gain-temperature coefficient, designed for operation with positive-true TTL logic. It is a small, low-cost replacement for the pioneering MDA-F fast DAC. The DAC1106 is available as a 2" x 2" x 0.4" (51 x 51 x 10mm) module with either 8- or 10-bit resolution, at a price of \$119 (1-9) for 8 bits, \$139 for 10 bits.

It provides an output current of 0 to 5mA full-scale as a binary unipolar DAC, and -2.5mA to +2.5mA in offset-binary bipolar operation. Voltage compliance is 1.2V, which allows it to be used without the additional delay of an output op amp in critical applications, yet with reasonable voltage output. Internal impedance is 600Ω. Typical output settling time to 0.2%/0.1%/0.05% is 25/40/50ns, with a guaranteed maximum of 30/50/60ns.

APPLICATIONS

High-speed d/a converters are useful in the design of fast a/d converters, especially successive-approximations and counter-comparator types (which include tracking types and "infinite" sample-holds). They may also be used for conversion of data at "video" rates to analog form, and for generation of 0.1%-resolution sweeps and other analog functions, using counters (and read-only memories—ROM's—for function generation), at rates of the order of 20kHz or better. In such applications, time skew of the logic inputs should be held to less than 5ns, since it has a major effect on the output "glitch."



*For complete information on DAC1106, request M14.

THREE NEW D/A CONVERTERS

DAC1009, MULTIPURPOSE: TTL/DTL/CMOS POSITIVE-TRUE LOGIC, V OR I OUTPUT, 12 BITS

The DAC1009† is a 12-bit multipurpose D/A converter packaged in a 2" x 2" x 0.4" (51 x 51 x 10mm) module. It can be programmed for (self-contained) fixed reference or 2-quadrant multiplication, and for current or voltage output. It will interface with TTL/DTL or CMOS logic systems, responding to positive-true logic signals.

As a voltage-output device, the DAC1009's self-contained output op amp provides a settling time of 4μs to 0.01% (full-scale digital step), with a choice among 5 output ranges. The current output, which settles to 0.01% in 700ns, can be used with an external inverting op amp; the device's precision scaling resistors can be used for the same choice of output ranges, with optimum temperature tracking of the scale-factor-determining elements.

Though it has a precision internal-reference source, the DAC1009 will also accept an external analog reference. In this form of operation, the (unipolar) reference voltage will be multiplied by the unipolar or bipolar (offset binary) digitally-set gain for 1- or 2-quadrant operation. As a multiplying DAC, the small-signal bandwidth is 950kHz and the full-power bandwidth is 125kHz. With appropriate circuitry, feedthrough is less than 1LSB at 50kHz.

The DAC1009 is compatible with TTL and DTL logic, and will respond to CMOS levels as high as +15V. At the low end, the CMOS driving gates should be capable of sinking 1mA at <0.8V for logic "0".

Price of DAC1009 is \$84(1-9), \$54(100+).



DAC1118 INCLUDES 12-BIT INPUT REGISTER, PROGRAMMABLE OUTPUT, 5μs SETTLING, LOW COST

The DAC1118‡ includes an input storage register, a versatile output amplifier with 5 programmable output-voltage ranges, and the performance advantages of a 20ppm/°C gain-temperature coefficient and 5μs settling to 0.01%, in a 2" x 4" x 0.4" (51 x 102 x 10mm) package, priced at \$80 (in 100's), \$112 (1-9).

It is DTL/TTL compatible, and can be ordered for binary, BCD, or two's-complement (bipolar) coding. The binary version can be connected for offset-binary bipolar coding.

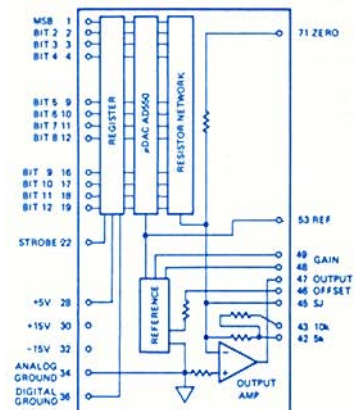
Digital data appearing at the converter's 12 input terminals will be strobed into the register whenever a positive-going transition is applied to the *Strobe* input.

With the *Strobe* steady (either "1" or "0"), the input data may be changed without affecting either the contents of the register or the output of the converter. Positive-true input logic provides positive full-scale output; that is, the analog response of the converter is not inverted.



†For complete information on the DAC1009, request M15.

‡For complete data on the DAC1118, request M16.



HANDLING VARIABLE DATA RATES WITH SERDEX FAST-TO-SLOW, SLOW-TO-FAST, STEADY-TO-BURST, BURST-TO-STEADY

by David G. Larsen and Dr. Peter Rony

The use of on-line data acquisition and control in the research laboratory has experienced dramatic changes since the introduction of the general-purpose small computer in the early 1960's. The cost was, of course, prohibitive for the first few years, for processing, memory, and -- to a lesser extent -- for analog/digital data-acquisition equipment. Then, as the cost tumbled at the rate of about 40% per year for a constant price/performance ratio, the use of a minicomputer became acceptable to more and more laboratories.

There were still rather serious limitations on the use of a minicomputer for the average research laboratory. The basic minicomputer was, and still is, only a small part of the system's cost. In addition to the central processing unit (CPU), interface hardware, and data-acquisition circuitry, software was also required. These additional requirements were so expensive, if purchased as a turnkey system, that in many instances a decision was made to build a "homemade" interface system. For most laboratories, this almost always proved to be disastrous: the amount of effort needed to write software at an assembler level and build interface hardware was, and will continue to be, underestimated by factors of five to ten times. Some of the very large corporate research labs were able to absorb the time, cost, and range of talent (from analog circuit design to digital software) and have very viable automation systems. However, most groups who built "homemade" systems discovered that their final operating system required an overall investment that had been substantially underestimated.

Recently¹, the SERDEXTM SERial Data EXchange modules have become available.* It is clear that the use of asynchronous serial ASCII-coded data, along with optically-isolated standard 20mA current loops, the two most important characteristics of SERDEX, will permit substantial savings of time and money associated with computer interfacing. With the SERDEX modules, only digital signals are transmitted; only a single twisted pair of wire is required for each remote location; both data and control commands can be either transmitted or received on each channel; no hardware interface to teletypewriters or to teletypewriter ports is required; all programming may be done in a high-level language, such as BASIC; high noise-immunity exists; and -- finally -- serial data can be

transmitted at the rate of 20,000 bits per second, which corresponds to 1800 ASCII characters per second.

The advantages of using asynchronous serial ASCII-coded data are almost overwhelming. In fact, the only disadvantage that such a technique has, when compared to parallel data-transmission systems, is speed. With serial ASCII-coded data, we will occasionally encounter situations where a loss of data, owing to a mismatch in the speed at which data can be handled, occurs, somewhere between the point at which such data is acquired and the point at which it enters the minicomputer.

An obvious source of rate-limiting is the teletypewriter itself, which can only handle data at the rate of 10 ASCII characters/second. (However, most minicomputers have available as options telecommunications ports that will operate at up to 20kbit/s.) A second rate-limiting step can occur when high-level languages are employed; such languages can require appreciable time to perform several digital multiplications and divisions, and this time will naturally limit the rate at which data can be accepted by the minicomputer.

For the resolution of dilemmas such as these, the user may find *First-In First-Out serial memories (FIFO's)* to be convenient buffers between digital devices whose data-handling speeds are mismatched. The principle of operation of the FIFO is straightforward:

- Digital data bits are independently clocked into the FIFO memory via the input clock. The data entry proceeds as long as the memory remains not completely full.
- The data bits, upon entering the FIFO, immediately ripple through the memory and stack up at the output terminals.
- The data bits are subsequently clocked out of the FIFO at a clock rate that is usually (and can be substantially) different from the input clock rate.
- A strict sequential order is maintained between the entering and leaving data bits: the first data bits to enter the FIFO are the first ones to leave.

The term, "first-in first-out memory" is certainly an apt description of this interesting LSI chip.

One of the popular FIFO's is the Fairchild Semiconductor 3341 64-word by 4-bit FIFO, which can operate at 1MHz shift-in shift-out data rates. According to the manufacturer:² "An ideal use of the 3341 FIFO's is with two systems or subsystems of differing data or unsynchronized data rates that must talk to each other. Data can be entered or removed in steady streams, bursts, or irregular patterns, or a combination of these." In our example, which involves the transmission of

²Fairchild Semiconductor: OPTIMOS manual, September, 1972, pp. 74-79.

THE AUTHORS are with the Scientific Telecommunications and Computer Interfacing Laboratories, Virginia Polytechnic Institute and State University, Blacksburg, Virginia. Mr. Larsen is in the Department of Chemistry, and Dr. Rony is in the Department of Chemical Engineering.

¹"SERDEX--The Near-Ideal System Interface," *Analog Dialogue* 7-2, 1973.

*For complete information on SERDEX, use the reply card. Request M17.

digital information from a digital instrument, via a SERDEX transmitter module, to either a teletypewriter, teletypewriter port, or telecommunication serial minicomputer port, we can envision the following situations:

A. Irregular data can be collected from a remote location and stored in a FIFO for transmission by a SERDEX transmitter module when it is convenient.

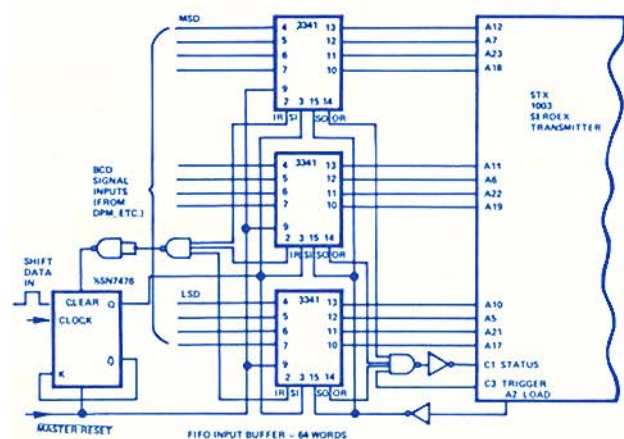
B. High-speed data can be collected in bursts from a remote location and stored in a FIFO for transmission by a SERDEX transmitter module at considerably slower data rates.

C. A slow flow of steady data can be collected from a remote location and stored in a FIFO which, with the aid of a SERDEX transmitter module (STX1003), re-transmits the data in bursts to the minicomputer, thus promoting more-efficient use of the CPU.

D. Data for printout on a teletypewriter can be loaded into a FIFO, freeing the SERDEX transmitter module and allowing the teletypewriter to proceed at its own slower pace.

To illustrate item C above, let us consider a laboratory that has a number of slow data-generating systems that require on-line data logging (but perhaps minimal immediate control response). It would be very desirable to use FIFO's between the sources of data (including converters or multiplexers) and the parallel *n*-digit BCD (binary-coded decimal) input to the SERDEX transmitter module; these *n* FIFO's would store parallel BCD data and thus reduce the number of times the SERDEX transmitter would need to be serviced by the minicomputer.

For example, let us assume that a liquid chromatograph output is such that one data-point per second is an adequate sampling rate. If the A/D converter output were 4 digits BCD (0.01% resolution), then, by multiplexing, 16 data points could be stored in a single 3341 FIFO without losing any data. It would then take a CPU asynchronous port, operating at 20,000 bits/second, a total of 35.2ms to read the 16 ASCII characters transmitted by the SERDEX transmitter module, operating at a similar 20,000b/s data rate. This corresponds to one 35.2ms transmission in a 16s period, which is a much more efficient way of handling data than to cause a CPU to service the transmitter module once a second. Using external memories at the parallel BCD data source, as suggested in this example, allows us much more flexibility in timing constraints when we write software, to service both a number of on-line instruments that are slow, and also those instruments that generate data at a very fast rate, but intermittently.



The figure shows a FIFO memory -- which can accept three BCD data bits and store 64 words -- used with the SERDEX transmitter. Of course, a FIFO can be added for each additional BCD character that is desired. The system works in the following manner (a more-concrete functional description appears in the Appendix):

- To input data into the memory: A clock pulse (*shift data in*) must be provided when the desired ("ready") BCD data is present at the FIFO inputs. The data may be entered at word rates from dc to 1MHz. At any time the FIFO is full, additional data points will simply be lost, until data has been shifted out to make room for new data.

- To transmit data, the STX1003 is used in the normal way: When an ASCII "?" is received, trigger C3 will initiate transmission by being *nand*-ed with the FIFO data-ready flags, and trigger the STX transmitter at C1. If there is no data in the FIFO, no transmission will occur when the ASCII "?" is received.

APPENDIX

First Data In, First Data Out (FIFO) Memory

The Fairchild 3341 is built with MOS technology and mounted in a 16-pin dual in-line integrated circuit package, and it is fully TTL-compatible. The name truly defines the system operation in terms of data flow. The 3341 is a 4-bit, 64-word FIFO: the first word entered will bubble to the output and be the first data removed as a 4-bit parallel word. Both input and output are asynchronous and independent in operation. The maximum data transfer rate of 4-bit words is 1MHz; however the input and the output can operate at the same or at different rates simultaneously.

DATA INPUT: When the Input Ready Flag (pin 2, "IR") is *high*, data on the 4 Input lines (pins 4, 5, 6, 7) may be strobed in by externally applying a *low-to-high* transition at the Shift Input (pin 3, "SI"). The "IR" input goes *low* after the *low-to-high* at "SI," and when "SI" is returned to *low*, the data will flow from the first input position towards the output, stopping in the last empty word location in the memory. All previously-entered data that has not been shifted out will be ahead of the last 4-bit word entered into the memory.

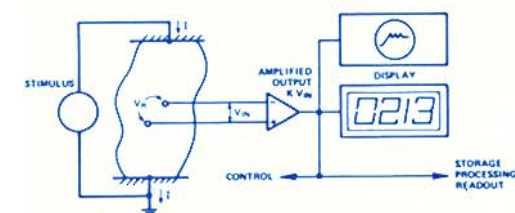
DATA OUTPUT: When the FIFO has data ready at its Output pins (10, 11, 12, and 13), the Output Ready Flag (pin 14, "OR"), will go *high*. New data can be shifted into the output by going from *low* to *high* on the Shift Output (pin 15, "SO"). "OR" will then go *low*, and when "SO" returns to a *low* state, new data will be shifted into the output, provided that there is data in the FIFO.

OTHER CONSIDERATIONS: If it is necessary to know exactly how much data the FIFO memory contains at any one instant, an external register can be built, using *up-down* counters, to perform this task. The 3341 can be used to build FIFO memories which accommodate large parallel words, in increments of 4 bits; it can also be easily expanded to hold more than 64 words, in increments of 64 words. See the manufacturer's application notes for these and other possibilities.

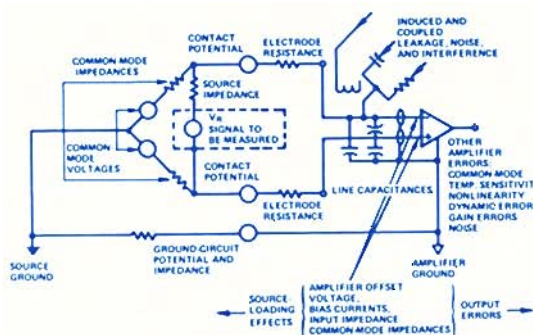
VOLTAGE MEASUREMENTS IN BIOMEDICAL RESEARCH HOW FET-INPUT IC OP AMPS CAN HELP—A BRIEF SUMMARY

by Rich Frantz

The problem is easily stated but wicked to solve: One must measure a (small) voltage occurring between two points in an entity under test safely and with reasonable accuracy and fidelity (Figure 1a). Why it is difficult can be seen in 1b. The sources of trouble are threefold: the entity itself (including the measurement electrodes), the amplifier that acquires and processes the measurement, and their interconnection (and interaction).



a) Typical bioelectric measurement



b) Sources of noise and errors

Figure 1. Ideal measurement and the arrayed opposition

The entity. First of all, the voltage to be measured may be inaccessible to direct measurement; or the act of measuring it may introduce significant errors (such as contact potentials), or it may even change or destroy the entity if too large an energy flow (either in or out) occurs. The first two of these considerations are in the province of the design of the experiment itself; the third can usually be ameliorated by proper electronic design and choice of circuitry. In addition, there will be a number of traditional electrical characteristics of the circuit that affect measurement accuracy, compounded by the differential nature of the measurement (since there aren't too many entities in Nature that are so obliging as to have a terminal at ground potential). These include: source impedance, common-mode impedances, and common-mode voltages and currents (such as line-frequency and radio-frequency pickup).

The Amplifier. Faithful readers of these pages and others, such as the *Analog-Digital Conversion Handbook*¹ (see page 23), have been well-exposed to the foibles of nonideal amplifiers and the comparative merits of isolation amplifiers, differential-instrumentation amplifiers, and op amps in subtractor configurations. Relevant sources of error include the amplifier's offset

voltage and bias currents (and their variations with time, temperature, and supply voltage), amplifier voltage- and current-noise, input impedance (the raw amplifier and/or the associated circuitry), common-mode voltage error and impedances, bandwidth limitations (both differential and common-mode). Equally important considerations in these days of shrinking budgets are device costs; fortunately, integrated-circuit productivity tends to be counter-inflationary, and a respectable-performance differential amplifier can be constructed from low-cost IC FET-input op amps, such as the AD503K or the AD514L.*

Interconnection. The problems that arise here include induced noise and interference, ground loops, common-mode and scale-factor errors due to loading, offset errors due to the flow of bias currents through source resistances, attenuation of high-frequency signals due to capacitive loading, and ac common-mode errors due to asymmetrical capacitive loading. In addition to the errors caused by contact potentials and their variation, such offset voltages may be considerably larger than the signals that "ride" on them and require continuous long-term nulling or ac coupling to avoid overranging the amplifier. Dangers to the entity under test may be posed by: differences in ground potential, dissipation due to bias current flow through the source resistance, capacitive coupling from the power line, and potentials or currents imposed by component or system failures, or potential differences in the "power-off" mode.

CHOOSING AN APPROACH

Space limitations prohibit completely satisfactory treatment. However, having raised the questions that would lead the designer to consider salient elements of the problem, we can now suggest a few elements of solution that are known to be effective.

Isolation. For extreme "hard cases" where the entity under test involves living tissue, which must be protected in a "fail-safe" manner, and where some performance compromise is possible in terms of noise and bandwidth, an isolation amplifier (model 273, or some newer designs)†, may be considered.

Instrumentation Amplifiers. Depending on the characteristics of the source and the required performance, instrumentation amplifiers are available for use, essentially as "subtractors-with-gain."‡ As a rule, they are designed to minimize cost, voltage drift, and/or common-mode error. It is hard to find an amplifier that combines all of these features and the high input impedance and low bias current of FET-input amplifiers.

Instrumentation-Amplifier Configurations. Where the high input-impedance and low bias-current of FET's are essential to minimize loading of the source, a proven configuration that can utilize low-cost FET-input op amps is shown in Figure 2.

*For information on these amplifiers, request M2 and M5.

†For information on the 273 and other isolation amplifiers, request M18.

‡For information on the AD520, 602, 603, and 605 instrumentation amplifiers, request M19.

¹ Still in print and available at \$3.95 from Analog Devices, Inc., P.O. Box 796, Norwood, Mass. 02062, U.S.A.

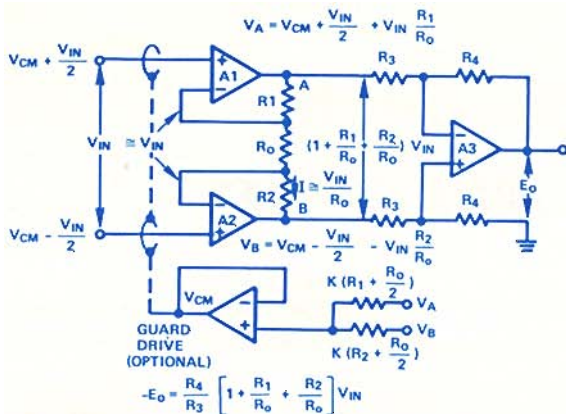


Figure 2. Differential-amplifier configuration

How it works: Since the voltages appearing at the positive inputs of A1 and A2 must be duplicated at the negative inputs, the current through R_O is determined by the difference voltage, V_{IN} , which is magnified by the sum of the resistance ratios, to appear as the difference voltage $V_A - V_B$. Since the common-mode level is the same as the input common-mode level, current to flow through R_O ; therefore the output common-mode level is the same as the input common-mode level. This relative reduction of the common-mode level eases the task of stage A3 (shown as a simple subtractor-with-gain) to

(continued from page 7)

A LOW-NOISE FET-INPUT IC OP AMP

is usually proportional to $1/f$, though, more generally, it often fits a $1/f^2$ relationship. It is thought to be due to imperfect surface conditions on transistors and integrated circuits, in carbon composition resistors, etc. In bipolar transistors, a correlation has been established between excessively-large amounts of $1/f$ noise and unreliability. In some transistors, "popcorn" noise exists; it is an erratic jitter between two values of h_{fe} , causing additional base-current noise, consisting of a shift at random intervals between two values of base current. It is unacceptable in a low-noise amplifier.

SPECIFYING AND MEASURING THE AD514

As with modular low-noise amplifiers, such as the model 52 (see page 10), noise in the $1/f$ region is usually measured in terms of its peak-to-peak value, for a number of reasons: first, peak-to-peak noise is the important variety in many low-frequency applications, second, it permits inspection of a large number of individual noise values in a short period of time, whereas an rms measurement provides a single average number, with little qualitative or quantitative regard for what the actual waveform might be like. Finally, it permits a rough estimate of the general order of magnitude of the rms voltage. Unlike sample testing in the laboratory, the quantities of low-cost IC's that must be tested on-line in a relatively-short time preclude the possibility of using chart recorders for unhurried examination of noise waveforms over lengthy periods in a quiet environment (if the environment is not quiet, the peak that causes an amplifier to "fail" may be an artifact caused by interference). Since most other tests on IC operational amplifiers are performed in milliseconds, it may be evident that, in order to keep the cost at a minimum, the time allowed for noise testing has to be kept to a matter of seconds.

bring the differential output of the first stage "down to earth," i.e., to system ground. The common-mode rejection of the second stage is theoretically infinite, but it is affected by the resistance-ratio match and the amplifier characteristics. However, the common-mode error in the A3 stage is reduced (relative to the input) by the gain of the first stage.

First-stage common-mode errors can be minimized (a) by choosing amplifiers with low error contributions and/or (b) by matching their errors in polarity (and magnitude), and mounting them isothermally, so that the errors become common-mode signals, rather than difference signals. Figure 2 includes a guard-drive circuit that can minimize pickup and capacitive loading on the source. FET-input op amps can minimize amplifier loading on the source and voltage drops in the source impedance due to amplifier bias current. Circuit-board leakage, especially to the supply leads ($15V/10^{11}\Omega = 150pA$!) should be reduced by the use of guarding and Teflon standoffs. Since bias current of FET input transistors doubles with each $10^\circ C$ increase of temperature, the amplifiers should be kept cool by the use of heat sinks (such as Wakefield 205 or 209), and decreased supply-voltage. ▶▶▶

Rich Frantz is a Product Marketing Engineer at Analog Devices Semiconductor.

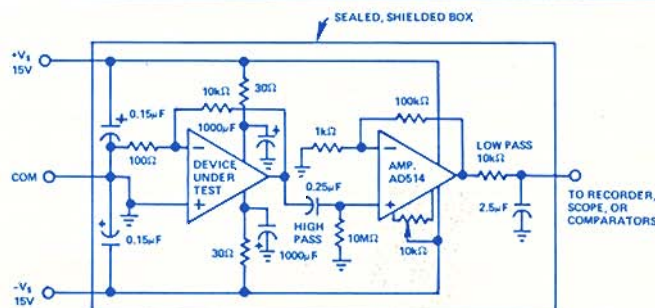


Figure 3. Test circuit for AD514

The amplifier under test is inserted into the circuit of Figure 3, in a closed, shielded box, protected (as well as possible) from both electrical noise and random air currents (they can introduce drift error, which is indistinguishable from low-frequency noise), and allowed to warm up for 30 seconds. The output of the circuit is then observed electrically, using biased comparators and logic. If, in two-out-of-three 10-second intervals, the specified maximum value of peak-to-peak noise has not been exceeded, the device is deemed to have passed the noise test.

An oscilloscope may also be used for observation, but one should use high intensity, careful attention, and an increased number of observations. If the test occurs in an electrically-noisy environment, great care should be taken to avoid picking up interference noise, since there may be no practical way of knowing whether a single excessive spike is an artifact or a true random event.

The test circuit consists of two stages of amplification, one of which is inherently provided by the device under test. The post-amplifier also has a high-pass and a low-pass filter, which together determine the test bandwidth (100:1, or 2 decades in the $1/f$ region). For frequencies as low as 0.5Hz, this procedure will have sampled more than 10 cycles, and for frequencies down to 0.1Hz, 2 or more cycles. ▶▶▶

KEYS TO LONGER LIFE FOR CMOS

HERE'S HOW CMOS CAN BE PROTECTED AGAINST ABUSES

by Jerry Whitmore

The two principal dangers to analog CMOS (Complementary-symmetry Metal-Oxide Semiconductors) are static electricity and overvoltage (signal voltages exceeding the supply). Both can be effectively dealt with by the aware user.

STATIC ELECTRICITY

The danger from electrostatic voltage buildup is that of "punch-through" of the thin oxide (or nitride) layer that insulates the gate from the substrate, due to accumulation of static charge ($V = q/C = 1\text{ kV/nC/pF}$). This danger is minimal in working circuits, because the gate is protected by zener diodes on the chip, which permit depletion of the charge at safe levels. However, during socket insertion, it is possible for a large static charge to exist between the CMOS device and the socket. If the first pin plugged into the socket happens not to be common to the zener-diode protection circuit, the charge on the gate will discharge through the oxide layer, destroying the device. These four steps will help the device survive the system assembly stage.

1. Keep unused CMOS devices in the black conductive foam in which they were shipped to prevent charge buildup between pins.
2. Ground the operator, who is inserting the devices, to the system power ground with a plastic ground strap.
3. Before pulling the CMOS device from the protective foam, ground the foam to power common to deplete accumulated charge.
4. After the circuit has been inserted into a circuit board, keep the board grounded or shielded when carrying it around.

THE SCR "LATCH"

When working with analog CMOS circuits, the safest practice is to make sure that no analog or digital voltage applied to the device exceeds the supply voltage, and that the supply voltage itself is within ratings. Nevertheless, occasions do arise where

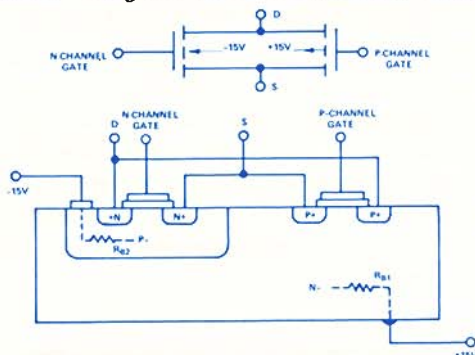


Figure 1. Cross-section of CMOS switching element

Jerry Whitmore is an Applications Engineer at Analog Devices, Santa Clara, Ca. 95050. This article was stimulated by several helpful discussions with Walter Jung, of Cockeysville, Md. We expect to publish an article by him on a variety of protective circuits, to appear in an early issue.

it is necessary to tolerate overvoltage. Protection is possible in most cases, if the mechanism of failure is understood.

Figure 1 shows the circuit and cross-section of a typical CMOS output switching element. From the connections and associations of the various elements and regions, we can draw an equivalent diode circuit (Figure 2). If the analog input voltage

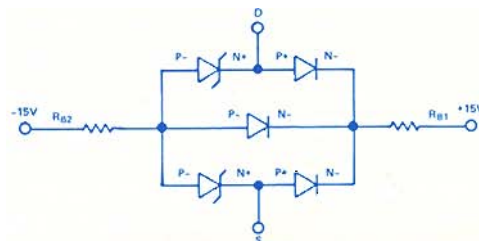
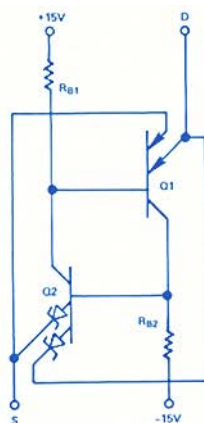


Figure 2. Diode equivalent circuit of CMOS switching element at either the S or the D terminals exceeds the power-supply voltages, the parasitic transistors formed by the various diode junctions are placed in the forward bias mode. These parasitic NPN and PNP transistors appear to form the SCR ("silicon controlled-rectifier") circuit shown in Figure 3. Overvoltage



IF, FOR EXAMPLE, A POSITIVE OVERVOLTAGE IS APPLIED TO THE DRAIN TERMINAL, THE BASE OF Q1 WILL CONDUCT WHEN ITS EMITTER VOLTAGE EXCEEDS V_{DD} BY ONE BASE-EMITTER DROP. THE COLLECTOR CURRENT WILL INCREASE TO A LEVEL LIMITED ONLY BY THE V_{SS} AND V_D CURRENT LIMITATIONS. SINCE THE METAL INTERCONNECT TO THE SUPPLY TERMINAL IS NORMALLY DESIGNED TO HANDLE SMALL CURRENTS, THE CURRENT DENSITIES INVOLVED CAN CAUSE DEVICE FAILURE.

Figure 3. Parasitic transistor action in CMOS switch can cause excessive current and metallization failure. Normally, the outputs of op amps are used as the voltage sources feeding the S or D terminals, so the currents cannot exceed the op amps' dc output current limitations. Nevertheless, it is still possible for transient induced currents to destroy the CMOS device; protection is therefore desirable.

Figure 4 illustrates a means of preventing turn-on of the parasitic transistors by means of diodes (say 1N459's) in series with the supply leads. If the S or D terminal is at a higher-than-supply voltage, CR1 and/or CR2 are reverse-biased and base drive is unavailable to turn the transistors on. A separate pair of diodes should be used for each CMOS device to be protected. Though powerful, the method is not infallible. If one terminal of the switch is tied to a negative potential (e.g., a charged capacitor), and the other terminal is raised above V_{DD} ,

(continued on next page)

USING DPM'S IN OUR OWN TEST EQUIPMENT FOR FAST, EASY, ACCURATE TESTING OF ELECTRONIC PRODUCTS

by Jim Hayes

Since entering the Digital Panel Meter market, we have discovered (to no one's surprise) that DPM's are useful in production test equipment for our other electronic products. The advantages are like those for any other application: the DPM allows the user to make accurate, unambiguous readings of electrical quantities without the errors associated with conventional analog meters. The digital readout and fast response relieve even the unskilled operator of the necessity for interpolating between analog scale divisions and waiting for the pointer to settle. Using the digital output, the operator can even be relieved of the task of writing down the readings. The low bias current and high input impedance of the DPM further simplify its application, since buffering is seldom necessary.

Using the digital data outputs, the meter can be interfaced with comparators to provide an accurate go/no-go indication, to data processors for storage and evaluation of test results, and to printers for hard-copy test data for quality-assurance records. As an A/D converter, the DPM is, of course, the key link in automated test systems with optional on-line operator control.

In addition to the above advantages, test-equipment operators find test sets with DPM readouts to be easier and less tiring to use, allowing faster and more-accurate testing of all relevant product parameters in full operation. Here are a few examples:

TESTING OP AMPS. Many specified op-amp parameters are tested on a 100%-sample basis, often over specified temperature ranges. To check compliance with tempco specs, test fixtures are loaded with devices to be tested, placed in "ovens," and cycled over the full temperature range. A DPM rapidly reads

out the voltage offset and bias-current error of every device in sequence, so that all devices can be fully tested at every temperature checkpoint in a short time.

TESTING D/A AND A/D CONVERTERS. To check d/a converter outputs for accuracy and linearity, the analog output is measured with a DPM and compared with the digital input. The operator can use the direct reading of the output to make test adjustments or go/no-go decisions rapidly. DPM's can also be used to measure magnitude and polarity of errors directly. An example of A/D converter testing is shown in the photograph: The ADC1100, a 0.05%-resolution converter, has its BCD output displayed digitally, and compared with the analog input, as measured with a 0.005% AD2004* DPM. By matching the two displays, the operator can test ADC1100's to specified accuracy in minimal time.

TESTING DPM's. Since DPM's use several circuit boards for different functions, the test fixture for each board is an "incomplete DPM," consisting of the other boards and appropriate connectors. The board is placed in the test fixture, and the DPM is checked as a whole. DPM's are used for troubleshooting in these fixtures by checking for proper voltages at specified test points. On ac-powered DPM's the power-supply board's output of $\pm 15V$, $+5V$ and (for gas-discharge displays) 200V, can be tested with a single DPM (with attenuators and switch controlled decimal points) by an untrained operator in seconds.

THE TEST DEPARTMENTS' FAVORITE DPM. Which DPM is the most-used in our test equipment? Our test-equipment engineers prefer the AD2004* (+5V-powered, 4½-digits). Besides the reasons discussed above, the high resolution, accuracy, and stability of the AD2004 make it ideal for test equipment, allowing precise measurements of test parameters, with long intervals between calibrations. But plenty of our other DPM's are also used (for the simpler tests).

(continued from preceding page)

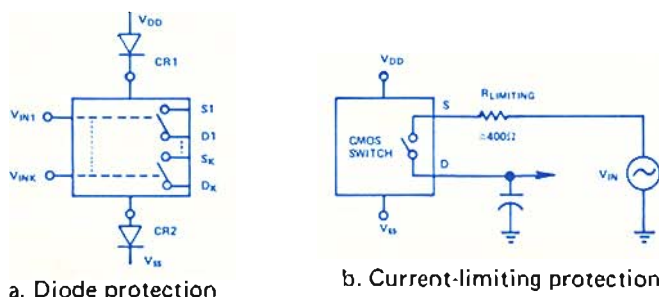


Figure 4. Circuit protection schemes

the avalanche diode at one emitter of Q2 is sufficient to supply enough base drive to turn Q2 on, despite the protective diodes. For such a situation, a current-limited supply, or resistance in series with the capacitor is necessary.

If transient overvoltages are expected at the S or D terminals, 300–400 Ω in series with the terminal to be fed by the voltage source is suggested (Figure 4b).



THE AUTHOR: Jim Hayes is Marketing Manager, Digital Panel Meters. *For information on the AD2004, request M20.

Application Briefs

WAYS OF USING THE AD7520

SOME DESIGN IDEAS FOR A 10 BIT M

by Jerry Whitmore

The AD7520*, introduced in the last issue of *Dialogue*, is a monolithic 10-bit thin-film-on-CMOS digital-to-current converter, available in a 16-pin dual in-line package at low cost. Its equivalent circuit is, in effect, a digitally-controlled attenuator (Figure 1). Its ability to accept a wide range of positive or negative reference voltage, with linear response and wide bandwidth, makes it useful as a 4-quadrant multiplying d/a converter, as well as in more-conventional conversion applications. In the earlier article, we showed configurations for using it as a unipolar and as a bipolar d/a converter, the latter for both sign-magnitude and offset-binary/2's-complement coding.

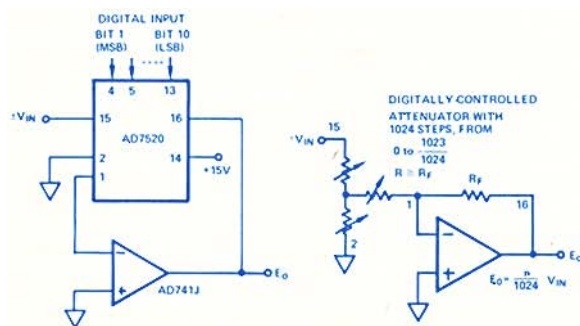


Figure 1. Connection of the AD7520 for unipolar binary input, and an equivalent circuit

Here, we shall mention a few more of its potential applications, with the thought that we may stimulate the reader to dig deeper into the many uses of DAC's, especially those having the promise of economy associated with monolithic integrated-circuit devices, and of power-conservation associated with CMOS devices. Beyond the circuits illustrated here, the interested reader should also consult Chapter I-4, "Analog Functions with Digital Components," in the *Analog-Digital Conversion Handbook* (see footnote 2 on the opposite page).

PROGRAMMABLE POWER SUPPLY

Since a d/a converter, with an op amp, can supply voltage in accordance with a digital code, and the op-amp output can be boosted in voltage or current capability to any reasonable degree by external circuitry, a programmable power supply should be a realistic possibility. One such circuit is shown in Figure 2.

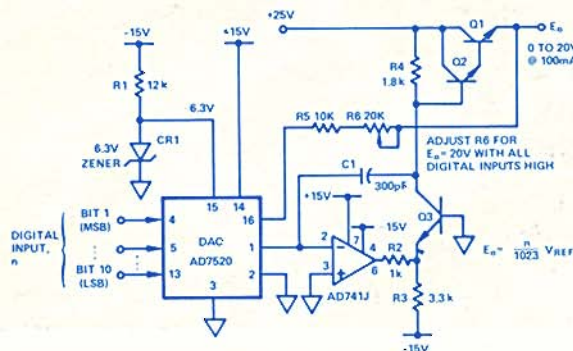


Figure 2. A digitally-programmable power-supply

Other circuitry could be used to provide a bipolar output range, so that one set of digital inputs could command a large positive-and-negative range of voltage and/or current. The supply shown in Figure 2 is designed for programmable voltage, but programmed-current supplies are equally possible, using conventional op-amp current-output circuitry.

If the reference voltage is variable, the converter and its boosted output circuit becomes a power amplifier with programmable gain, with frequency response from dc to well-beyond the audio range. The digital input can be furnished from any digital source, such as a computer or digital communications link (e.g., SERDEX). It can also be furnished manually, using switches to route control voltage to the appropriate digital code inputs. Note that the CMOS switching provides the benefits both of large logic-signal capability (hence high noise-immunity), and very low power drain on the source of the logic signals.

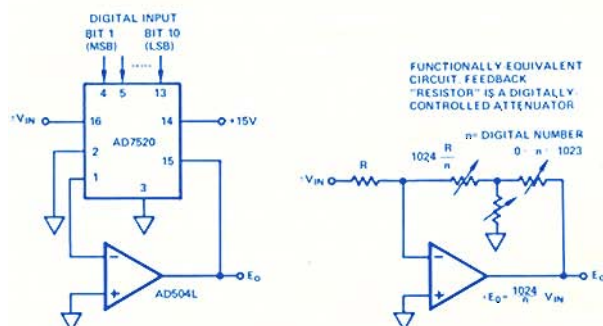


Figure 3. An analog-digital divider

ANALOG DIVIDER

Since one form of analog division circuit is a multiplier in a feedback loop, one might consider the divider circuit shown in Figure 3. In this circuit, the feedback current from the converter's "reference" input to the summing point of the op amp is proportional to (i.e., multiplied by) the digital number; but it must also be equal to the current developed through the input resistor. Therefore the op-amp output is constrained to depend on the ratio of the input signal to the gain value of the digital number. Note that the AD7520 in such an application is inherently a 2-quadrant divider, since the input signal (and the inverted output) can be either positive or negative. Connected as shown, the gain magnitude varies from a minimum of $1024/1023$ to (theoretically) $1024/0$, the open-loop gain of the op amp; the largest controlled gain is $1024/1$. At the higher gains, accuracy is lost because the feedback attenuation for small numbers may only be accurate to within $\frac{1}{2}$ LSB; for example, at a gain of 1024, if the LSB has an error of 10%, the gain will be in error by that amount. Naturally, accuracy rapidly improves with increasing denominator magnitude, and the error be less than 0.05% at full-scale denominator, after adjustment.

* For technical data on the AD7520, request M21.

LAST ISSUE OF ANALOG DIALOGUE Vol. 8 (1974), No. 1

If you haven't seen the last issue of *Dialogue*, you can get a copy by requesting M22. Here's what you've missed:

10-Bit Monolithic CMOS D/A Converter That Can Be Used for 4-Quadrant Multiplication (AD7520)

High-Precision Thin-Film Resistance Network: A Useful and Important Technology

High-Speed Op Amps Revisited - 1; What Does "High-Speed" Mean to the User?

Low-Cost RMS-Measuring Circuit (see page 24, this issue)

Low-Noise Non-Inverting Chopper Op Amp (261)

Two Improved Function Modules:

434 Wide-Range Multiplier-Divider

433B Multifunction Circuit: $Z(Y/X)^m$

Application Briefs:

Temperature-Measuring Circuit Borrows Power and Reference from DPM

Reducing Multiplier Linearity Errors: Crossfeed Reduces 2nd-Harmonic Distortion and Feedthrough

Using CMOS Switches for . . .

Low-Cost Sample-Hold

Digitally-Controlled Timer

Lock-In Amplifier Uses Single I.C.

Current Controller Uses Adjustable Exponent

Announcement of the new *Nonlinear Circuits Handbook*

Editor's Notes: On the Significance of the AD7520 monolithic CMOS DAC; An invitation to read our Annual Report

Advertisement: The AD528 fast FET-input op amp



NEW LITERATURE FROM ANALOG DEVICES (FREE)

Guide to Analog CMOS Switches and Multiplexers: A 44-page compilation of information on ADI's monolithic CMOS switch products, including technical data, package- and bonding-diagrams, Application Notes, terminology, protection schemes, and dynamic performance notes. Request M13.

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1. How to link A/D converters with teletypewriters and minicomputers.
2. How to link a TTY or minicomputer to a remote DAC for system applications.
3. Using a TTY or minicomputer to control relays or solenoids, up to 10,000 feet away, using SERDEX.



HANDBOOK ERRATA

I. NONLINEAR CIRCUITS HANDBOOK

It would be surprising to find "zero defects" in a newly-published book. However, the number that have turned up in the 536-page *Nonlinear Circuits Handbook*¹ to date have been encouragingly small. Readers are urged to mark the corrections in their own copies immediately, while it is fresh in their minds. Even more strongly, readers are begged to send us word on any other discrepancies they may find in the course of perusing the book, so that we may get the word out.

1. Chapter 3-7, Page 391, Table 1, "Characteristics of Some Common Waveforms:" The second line of expressions in the group "Offset Pulse," relating to zero-average pulses, has a number of errors.

A. Under RMS, $\sqrt{A}$, instead of A

B. Under RMS/MAD, $(1+A)/2\sqrt{A}$, instead of $(1+A)/2$

C. Under Crest Factor, $1/\sqrt{A}$, instead of $1/A$

2. Page 51, line 11, there is one "op" too many.

3. Page 317, Figure 36, the waveform next to the oscillator, at the bottom of the Figure, being a 10Hz waveform, should have a period of 0.1s, not 1 second.

II. ANALOG-DIGITAL CONVERSION HANDBOOK²

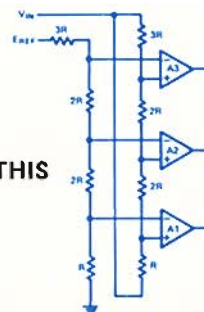
Few, if any, additional errors have been reported since the last tabulation in *Dialogue* 7-1. However, a minor technical blunder occurred in Figure 29, p. 11-53, for which your Editor must accept full blame.

The Figure in question is a rudimentary diagram of a 3-bit parallel A-D converter. Unwisely, a bias-current compensation scheme is shown (at high speeds, the attenuator network has low values of resistance, hence compensation may not be necessary, especially at the 3-bit level; also, if bias currents shift, compensation will be less than perfect; considering the sparse level of detail, the bias-current-compensation circuit is excessive "frosting on the cake;" finally it's wrong!).

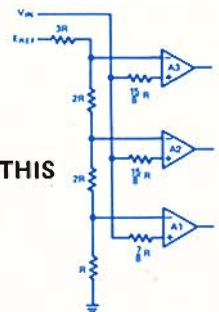
The mistake teaches a worthwhile lesson: When several op amps are driven from a resistive ladder, proper bias-current compensation calls for a similar ladder at the input—that is driven-in-common, as shown below for a simplified version. The compensation must account for the superposition of all the bias currents to result in equal offset voltages at both terminals of all amplifiers.



USE THIS



NOT THIS



¹Published 1974, by Analog Devices, Inc., 536pp, \$5.95.

²Published 1972, by Analog Devices, Inc., 402pp, \$3.95. Both books are available for \$7.95, when ordered together for shipment to one destination.

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