

# analog dialogue

A forum for the exchange of circuit technology: Analog and Digital, Monolithic and Discrete

SLIM, LOW-COST 3½ DPM (P.3)  
Four New I.C. Op Amps  
Fast 12-Bit A/D Converter  
Complete Contents on Page 3



# Editor's Notes

## RESISTANCE NETWORKS

Converter linearity depends on resistors and switches. Monolithic linear-integrated-circuit technology is capable of producing excellent switches at low cost. For example, our AD550-551 series allow us to build such products as the high-accuracy ADC16-Q and the low-cost ADC-12QZ\*A/D converters, and to sell them at prices that are attractive to both us and our customers.



The limiting factor on further product improvement and cost reduction has been the cost and difficulty of obtaining resistor networks of adequate accuracy and stability. At the present state of the Art, suitable electrical characteristics, low cost, and ready availability seem to be mutually exclusive.

As a first step toward breaking this logjam, we have established a new Resistor Products Division, which is devoted to the development and manufacture of thin-film resistor networks and substrates. Located in Rochester, N.Y., it is managed by Mr. Abram Terpening, formerly General Manager of Megadyne Industries, Inc. In addition, Dr. Carl Drumheller, founder and former president of Megadyne, is now a technical consultant to Analog Devices.

Equipped with some of the most modern equipment and advanced technology in the industry, and armed with an exquisite knowledge of customer requirements (gained partly through our own experience as a major customer for precision resistor networks), we expect that before long we can provide our readers with announcements of important new resistance products, and insights into their behavior, specifications, and successful application. But even sooner, we can expect to see the beginnings of improved converter designs, specifications, prices, and delivery.



## SYNCHRO-DIGITAL CONVERSION (AT LAST!)

For some *Dialogue* readers, there has long been a gaping "hole" in our conversion product line: Synchro-to-Digital converters. Beginning on page 7 of this issue, the void begins to be filled, with the introduction of 10- and 14-bit converters, a "tandem" converter, and a 14-bit digital angle indicator.

Other readers, unfamiliar with this somewhat specialized area of conversion endeavor, may feel aware of a "hole" in their understanding. Just what is a synchro-to-digital converter? What does it do? Where is it used? Could I use it if I understood it better? What do the specs mean?

We shall seek to answer these questions in some detail in forthcoming issues of *Dialogue*. In brief, though, a synchro transmits a measurement of a physical angle in terms of ac voltages on three wires. A S/D converter determines the angle and converts it to a digital code, *modulo* 360°. It has been most-often used as a position feedback in navigation, radar, and other control systems having military implications. However, there appear to be many peacetime applications in industrial and process control.



\*For information on the AD550-551 switches, and the ADC-16Q and ADC-12QZ converters, use the reply card. Request J24.

## A FALLACY DEBUNKED or, When is 2 x 8 ≠ 16?

More often than we should, we encounter this appalling situation:

A potential customer for a 12-bit D/A converter observes that 8-bit DAC's are quite a bit cheaper. He therefore proposes (or entertains a proposal) to sum the outputs of two 8-bit DAC's, attenuating one of them by  $2^8$  (=256). This will give him 16 bits, of which he can throw away the 4 least-significant, and he'll still be way ahead! Or will he?

The answer: He'd be even better off to throw away the whole second DAC, because there's "no way" that this technique will give him better than 8-bit effective resolution using anybody's off-the-shelf low-cost 8-bit DAC.

The reason: A 12-bit DAC will furnish 4096 distinguishable output levels in numerical order, separated by intervals of  $1/4096$  of full scale. If any level is in error by more than  $2^{-13}$ , or  $\pm 1/8192$  of full scale, it will appear within the  $\pm 1/2$ LSB quantum assigned to one of its neighbors and become indistinguishable from its neighbor(s). Since the number of effective inputs is limited by the guaranteeable maximum error, an 8-bit DAC is allowed a maximum error of  $2^{-9}$ , or  $1/512$  of full scale. Thus, in the proposed usage, the more-significant 8-bit DAC alone can have an error 16x larger than one can tolerate in 12-bit operation.

No DAC manufacturer should condone such folly! ▶▶▶

## A READER NOTES . . . STANDARDS

I see you adhere to ANSI [American National Standards Institute] Y32.2 symbols and Y10.19 abbreviations. Congratulations!

Why not tell your readers?

E. U. Thomas

Grumman Aerospace

*We're glad to see that at least one reader appreciates our struggle (not always successful) to maintain consistency in the symbols and abbreviations used in ANALOG DIALOGUE.*

*While such consistency may be gratifying to some readers in the United States, unnoticed by others, but useful to all, we have a special reason for making the effort. Half of our readers are outside the United States, in countries having differing languages, graphic standards, and conventions. We believe it essential to minimize the difficulties of communicating to our friends abroad. While it would be prohibitively costly to publish completely different editions of DIALOGUE custom-tailored to each individual group, the effort to at least meet the prescribed American standards lowers one barrier to ready understanding.*

Dan Sheingold ▶▶▶

# analog dialogue

Route 1 Industrial Park, P. O. Box 280, Norwood, Mass. 02062

Published by Analog Devices, Inc., and available at no charge to engineers and scientists who use or think about I.C. or discrete analog, conversion, data handling and display circuits. Correspondence is welcome and should be addressed to Editor, *Analog Dialogue*, P.O. Box 280, Norwood, Massachusetts, U.S.A. 02062. Analog Devices, Inc., has representatives and sales offices throughout the world. For information regarding our products and their applications, you are invited to use the enclosed Business Reply card, write to the above address, or phone 617-329-4700, TWX 710-394-6577, Telex 710-394-6577, or cable ANALOG NORWOOD MASS.

# DESIGNING A SLIM, LOW-COST 3½ DPM FOR RUGGED RELIABLE INTERFACING AND READOUT

by Ivar Wold

The AD2010\* is a low-cost 3½-digit panel meter with a bright, sharp, non-blinking LED (light-emitting diode) display.

A general-purpose meter, its latched data outputs and no-nonsense digital interface are specifically engineered for use in data acquisition; in addition, the suppression of leading zero's (e.g., +8.5, not +08.5) makes visual readout a pleasant experience.

Its small area, shallow depth, light weight, and tool-free mounting make it easy to apply and install in instruments, panel-mounted instrumentation, and systems.

Since it operates from a low-voltage DC power source (5V, 2.5-3W) its excitation wiring can be both electrically safe and free from associated line-frequency noise. In addition, its excellent normal-mode rejection at line frequency (40dB, adjustable to 60dB in Model 2010R) makes it essentially immune to the effects of extraneous noise pickup.

Automatic zero correction eliminates the need for drift adjustment, except for routine scale-factor calibration at six-month intervals.

## WHY A NEW 3½-DIGIT PANEL METER?

At a time when seemingly every issue of the major engineering periodicals (and *Analog Dialogue*†) contains news of more and "better" DPM's, one might feel that there is really very little new to be said about the subject, that there are plenty of good DPM's available, and it is unlikely that the world needs yet another 3½ DPM. Right?

*Wrong!*

We conducted an intensive study of the expressed needs of DPM users and surveyed our own not-inconsiderable DPM production and field experience. We studied existing designs, new designs, and the state of the Art and ready availability of *proven* components. Our conclusions: the world is ready for a new generation of panel meters. And surprise: The objectives are similar to those for the earlier generation, only more so: reliability and ruggedness (above all), high accuracy and low drift, ease of use and of reading, low cost and small size. All of these objectives appear to have been met in the AD2010.

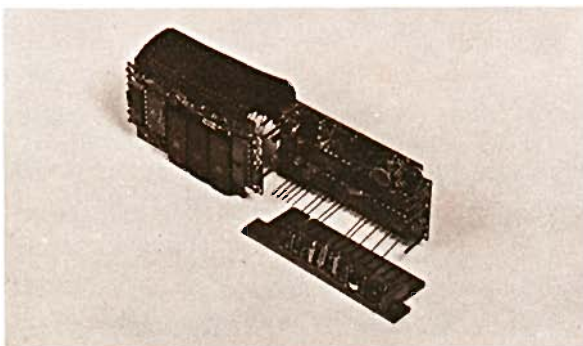
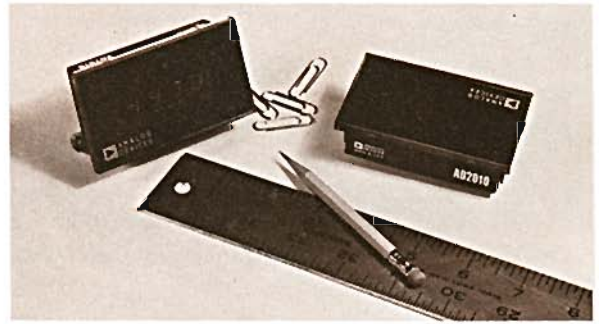


Figure 1. AD2010 Assembly

\*For information on Model AD2010, use the reply card; request J1. Price in 100's: \$79.

†Volume 5, No. 5; Volume 6, Nos. 2 and 3.



## DESIGN CONSIDERATIONS

The most noticeable feature of the AD2010, apart from its small size, is the 0.27" H LED display, which is certainly among the most rugged, and potentially the most reliable, of today's DPM displays. Since ruggedness and reliability go hand-in-hand with low parts count, a display of the TIL306 type was chosen. Besides the 7-segment LED, each element includes an MSI (medium-scale integrated-circuit) chip comprising a BCD counter, a latch with external outputs, and a decoder-driver.

A further contribution toward reliability can be achieved by operating at the lowest feasible power levels and avoiding high voltage. Since the LED display is inherently low-voltage, a single 5-volt DC supply (a DPM concept pioneered by Analog Devices and now in wide use) became a natural choice. Any necessary negative voltages could of course be generated internally.

*continued on page 4*

## IN THIS ISSUE

Editor's Notes . . . . .	2
<i>Designing a Slim, Low-Cost DPM</i> . . . . .	3
New Synchro-Digital Conversion Products:	
14-Bit Synchro/Digital Converter . . . . .	7
10-Bit Synchro/Digital Converter . . . . .	7
Two-Speed S/D Converter for	
High Resolution . . . . .	7
5-Digit Synchro Angle Display Meter . . . . .	7
Fast, High-Resolution A/D Converter (12	
Bits in 3.5µs) . . . . .	8
Low-Cost A/D with 3½-Digit BCD Output . . . . .	9
Four New I.C. Op Amps	
Fast Op Amp (500ns max Settling	
Time to 0.1%) . . . . .	10
AD504M: Lowest Noise and Drift . . . . .	10
Economical Low-Drift FET-Input Op Amp . . . . .	10
Fast, General-Purpose, Wide-Temperature-	
Range Op Amp . . . . .	10
I.C. Insight: <i>Not By Drift Alone</i> . . . . .	
(Chapter 2: The "741") . . . . .	11
<i>AD520, A True Instrumentation Amplifier</i>	
(Not an Op Amp) . . . . .	12
<i>True RMS Measurement at Low Cost</i> . . . . .	13
<i>Automatic Gain Control Circuit</i> . . . . .	13
<i>Vector Difference Circuit</i> . . . . .	14
<i>Low-Noise, Low-Drift FET-Input</i>	
Amplifier Design . . . . .	14
Worth Reading . . . . .	15
"Four New Linear Integrated Circuits. . ."	
-Advt. . . . .	16

An important factor affecting both accuracy and ease-of-use is the ability of a meter to reject noise, particularly at line frequency and its harmonics. The proven dual-slope technique,\* with an integration period equal to one (or more) line periods, was a natural choice.

A matter of concern in low-cost "single-ended" meter designs is the degree of isolation between the instrument's power-supply return and the input-signal common terminal. Without extreme care, supply current can flow in the analog input path and produce voltage drops in a shared lead, resulting in large measurement errors. While not fully differential (to keep cost down), the AD2010 eliminates ground loop-problems by means of a "limited differential" input circuit that allows the analog input return to follow the "low" side of the signal, at common-mode levels of at least full-scale input, with better than 60dB common-mode rejection.

### CIRCUIT CONFIGURATION

Having decided on a dual-slope approach, we carefully studied the many LSI circuits now available, ranging from complete dual-slope systems on single chips to more modest IC's having only counters and miscellaneous logic.

It soon became clear that the apparent advantages of "DPM-on-a-chip" circuits were more than offset by the relatively large number of external components required to interface these MOS IC's to a LED display. Additional components would be required to provide parallel TTL-compatible binary-coded decimal (BCD) outputs from the meter for data-acquisition applications.

When these and other factors were considered, it was decided that a carefully-conceived circuit incorporating the economies inherent in the display-plus-logic of the TIL306 (or equivalent

\*In a dual-slope converter, the input is integrated over a time period established by a full count. Then a constant (reference) is integrated over a period determined by the result of the first integration. Since  $I_1 T_1 = I_{ref} T_2$ , the count defining  $T_2$  is proportional to the input  $I_1$ . The count is then decoded and displayed. For more information on dual-slope conversion, see data sheet ADC-1 (request J2); *Analog Dialogue*, Vol. 5, No. 5, pp 3-4; or the *Analog-Digital Conversion Handbook* (Analog Devices, \$3.95), pp 11-48-50.

device), plus standard, proven analog and digital components, would lead to a more reliable and cost-effective, and less risky design.

The result is a converter that has automatic drift correction (to ensure zero stability), complete freedom from polarity ambiguity, and well-defined and reliable digital interfacing. A novel polarity-balance circuit insures symmetry of positive and negative readings without requiring the conventional (factory- or field-adjustable) symmetry-adjustment potentiometer.

### CIRCUIT OPERATION

The analog circuitry in the AD2010 has three normal states:

1. Quiescent, or drift-correcting
2. Integrating the signal
3. Integrating the reference

The reader will find it helpful to refer to the simplified schematic diagram and the timing diagrams of Figure 2 in following the explanation of the circuit's operation.

1. *Drift correction.* In this state, analog switches S1, S2, and S3 are conducting, while switches S4, S5, and S6 are open. Capacitor C1 charges up to the reference voltage via S1 and S2. The output of the voltage follower A1 will be  $V_{REF}$  plus the offset of A1.

Since S3 is closed, a closed-loop is formed around A2 and A3. This high-gain loop, stabilized with the aid of components not shown in the simplified schematic, will adjust the voltage across C2 until it reaches a steady state, which in turn will occur only at the time that no net current flows through the integrating capacitor C3. In the steady state, the voltage on C2 will be  $V_{REF}$  plus the offsets of A1 and A2. Since the gain of the comparator amplifier is high (about 50,000V/V), the offset of A3 is not significant.

2. *Integrating the signal.* About 8.3ms after a conversion has been initiated, the following things happen. Switches S1, S2, and S3 open, retaining the charges stored on capacitors C1 ( $V_{REF}$ ) and C2 ( $V_{REF} + \text{Offsets}$ ). Switch S4 closes, applying to A2 the input voltage  $V_{IN}$  in series with the reference voltage stored on C1. Since C2 still carries the stored value of the reference-voltage-plus-the-offsets, amplifier A2 integrates only the newly-added voltage.  $V_{IN}$ . The integration continues until

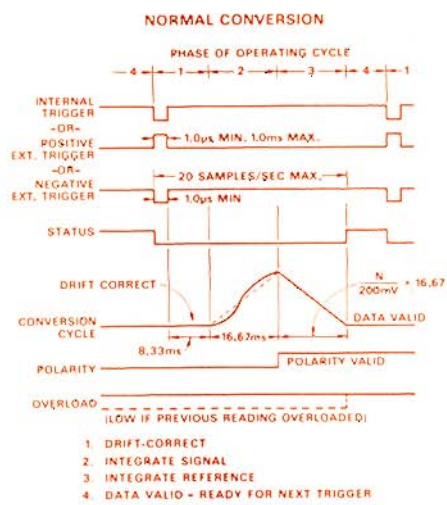
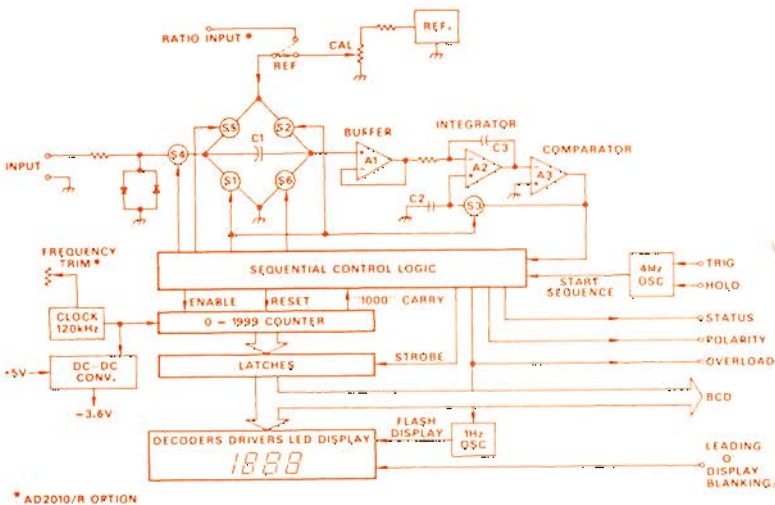


Figure 2. Simplified Schematic and Timing Diagrams of the AD2010

## AD2010: BRIEF SPECIFICATIONS (Typical @ +25°C and 5V supply unless noted otherwise)

### DISPLAY

- Four LED's 0.27"H (+1999 > N > -1999)
- Overload indication: three flashing zero's
- Decimal points: selectable at input connector, "1" on, "0" off
- Leading-zero display blanking (35, not 035), initiated externally

### ANALOG INPUT

- Full-scale range: 0 to  $\pm 199.9\text{mV}$
- Automatic zeroing
- Automatic polarity
- DC input characteristics:  $Z_{IN}$  100M $\Omega$ ,  $I_B$  3nA
- Absolute maximum voltage: 20V sustained, 50V momentary

### ACCURACY

- Maximum error: 0.05% of reading  $\pm 1$  digit
- Resolution: 0.1mV
- Temperature range (operating) 0 to +60°C
- Temperature coefficient:  $\pm 50\text{ppm}/^\circ\text{C}$

### NORMAL-MODE REJECTION

- 40dB minimum @ 60Hz (50Hz, AD2010/E)
- Adjustable to > 60dB @ 60Hz, AD2010/R (50Hz, AD2010/E/R)

### SPEED

- Internally triggered: 4 conversions/second
- Externally triggered: 0 (Hold) to 24 conversions/second (0 to 20 conversions/second for AD2010/E, AD2010/E/R)
- Maximum rate (triggered by Status): 24/s to 40/s, depending on signal magnitude (20/s to 33/s, /E versions)
- Time to complete full-scale conversion: 42ms max (/E versions 50ms)
- Overload adds  $\leq 20\text{ms}$ , depending on magnitude

### DIGITAL INPUTS (DTL/TTL Compatible "0" < 0.8V, "1" > 2.0V)

- External HOLD: "1" normal conversion, "0" hold
- External TRIGGER: Negative edge during hold

### DIGITAL OUTPUTS ("0" < 0.4V, "1" > 2.4V, 6TTL-load fanout)

- 3 Parallel BCD digits (8-4-2-1, positive true), latched
- "Overrange": Logic "1" indicates > 1000 counts, latched
- Overload: Logic "0" indicates  $|V_{IN}| > 199.9\text{mV}$ , "1" indicates data valid, latched
- Polarity: "1" indicates positive polarity, latched
- Status: "0" indicates conversion in process, "1" indicates conversion complete, latched

### POWER

- +5VDC ( $\pm 5\%$ ), 600mA

### WARMUP

- Essentially none required for specified accuracy

### ADJUSTMENTS

- Full-scale calibration adjustment, 6-month intervals
- Normal-mode rejection at mains frequency (AD2010/R and E/R only)

### PHYSICAL

- Panel cutout: 3.175"W x 1.790"H (8.065cm x 4.547cm)
- Depth (less connector and other protuberances): 3/4" (1.91cm)
- Weight: 4 oz. (113g)

### PRICE

- AD2010, AD2010/E \$120 (1-9), \$79 (100+)
- AD2010/R, AD2010/E/R \$135 (1-9), \$84 (100+)

Specifications subject to change without notice.

2000 clock pulses have been counted by the TIL306 counters and the control logic. At this point, the polarity of the average value of the analog input, as determined by the integrated sample of the input voltage, will establish the state of the comparator. That state is sampled and held by a D-type flip-flop (located within the "control logic" block).

Depending on the polarity, either S5 or S6 will close to initiate the next step in the sequence. At this instant, since the counter has gone through its full count, it is at zero.

3. *Integrating the reference.* If the input was determined to be positive, S6 closes and connects the input of A1 to zero volts. Since this input was at  $V_{REF}$  during the drift-correction interval, as recorded by the charge stored on C2, a net input of  $-V_{REF}$  (a negative voltage) is applied to the integrator. Since it has been established that  $V_{IN}$  was positive, the output of the integrator will ramp linearly in time "back" toward its quiescent level.

If the input was found to be negative, S5 closes, causing  $V_{REF}$  to be applied in series with the stored value of  $V_{REF}$  on C1. The net input to the integrator being  $+V_{REF}$  (opposite to the negative input), the output will again ramp "back" toward the quiescent level.

The display counter, which has been running during interval (3), is stopped when the output state of A3 changes polarity from the state that had been latched into the flip-flop. The number contained in the counter represents the analog input\* and is now strobed into the TIL306 latches, for continuous display until updated, and for data output at the rear connector.

The conversion having been completed, S1, S2, and S3 close, while S4, S5, and S6 open, and the circuit reverts to its quiescent mode.

## SAMPLE-RATE CONTROL

The AD2010 can be triggered by its internal 4Hz sampling oscillator, by externally-applied trigger signals, or (for highest speed) by self-triggering action that is a function of the time to complete a conversion.

With no connections to either the HOLD or the TRIGGER control inputs, the AD2010 will convert at a rate of 4 samples per second, an update rate that has been found to be quite agreeable to human operators reading the DPM.

To hold a reading, a logic "0" (DTL/TTL low) is applied to the HOLD input, stopping the low-frequency sampling oscillator. If a conversion is in progress, it will be completed and displayed; otherwise, the results of the last conversion will remain on display.

To trigger a reading externally, the converter must be quiescent and in hold. It can then be triggered by a low-going pulse applied to the TRIGGER input. The leading edge will clear the status (i.e., "ready") signal, and the trailing edge will initiate the conversion.

As we have noted earlier, the actual beginning of conversion (i.e., integration of the signal) is delayed by 8.33ms following the trailing edge of the conversion command. This is a useful feature; for example, the same signal that triggers the AD2010

continued on page 6

$$*N/2000 = \overline{V_{IN}} / V_{REF}$$

## THE AUTHOR

Ivar Wold, a native of Norway, comes to us by way of England, where he received a B.Sc. in Aero and Astronautics from the University of Southampton, with "first-class honors." Following graduate work, where his latent interest in electronics came to the fore, he joined Solartron, where he became the leader of a team developing complex digital measuring instruments (e.g., transfer-function and network analysers). Returning to Norway, he designed, built, and installed a real-time 16-terminal computer system at a bank. Since then, he has joined Analog Devices, starting as a technical consultant to Marketing. He is now Manager of Advanced Product Development.



continued from page 5

can also be used to advance a multiplexer (figure 3). The 8.33ms delay will allow the input to settle quite adequately before conversion commences. Also, zero drifts in the converter will be automatically corrected.

The HOLD input can also be used for triggering. If the converter has been in hold, returning the HOLD input to the high ("1") state will initiate a conversion. If the HOLD input is returned to low within approximately 200ms, the conversion will be single-shot; otherwise, the low-frequency oscillator will initiate another reading, and continue at 4Hz until the HOLD input returns to low.

## CONVERSION AT MAXIMUM SPEED

If the STATUS output signal is connected to the HOLD input, the completion of a conversion will immediately initiate a new conversion cycle, starting with the 8.33ms initial delay. Since the time for one conversion cycle is (for units adjusted for 60Hz line frequency rejection)  $8.33\text{ms} + 16.67\text{ms} + 16.67(\overline{V_{IN}/V_{REF}})$ , the maximum conversion rate can vary from 24 to 40 readings per second, depending on the input signal.

Since the initial 8.33ms delay is present during each conversion cycle, the STATUS output can be used to initiate the multiplexing of a number of channels into the AD2010 at its maximum theoretical conversion rate, with ample time for settling and for internal zero-drift correction (Figure 3).

## PACKAGING THE AD2010

The AD2010 is constructed on 3 fiberglass-laminate printed-circuit boards. All boards are double-sided, with plated-through holes. Following assembly and board-level tests, two of the boards are permanently mated, and the third is connected to this assembly by a plug-and-socket arrangement (it will then be physically secured after insertion in the case). A woven 23-conductor flexible cable brings BCD and control signals to the gold-plated fingers that are integral with one of the boards.

The complete assembly is compact and rugged, with no components exposed to mechanical damage.

The board assembly is mounted in an 11/16"-deep aluminum extrusion (the standard Analog Devices case, in cross-section), and the instrument is completed by the addition of moulded-

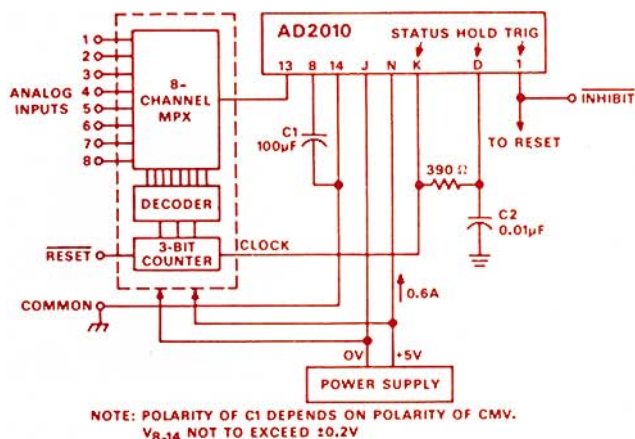


Figure 3. AD2010 Connected for Maximum-Rate Conversion and Continuously-Cycling Multiplexing. INHIBIT Holds a Specific Reading and Can be Used to Reset Multiplexer.

plastic front and rear plates. Integral with the front plate are mounting "ears", which enable the AD2010 to be snap-fitted into a front panel without the aid of tools. A snap-on plastic bezel with a red filter-insert completes the package.

The AD2010 can be calibrated from the front by the use of a small screwdriver after the bezel has been removed.

## RATIOMETRIC MEASUREMENT OPTION

In the AD2010, the stable 200mV reference is permanently wired to the converter input. An optional version, the AD2010R, provides an input terminal to which may be applied either the internally-generated reference voltage or a steady (short-term) 0.1-0.3V reference from elsewhere in a system.

This option is useful for measuring voltages that can be accurately known only in relation to a reference (which is itself not necessarily accurately-known). An example of this might be a strain-gage load cell. Its output has a highly-accurate and repeatable relationship (at a given loading) to an external excitation supply that may vary with time and temperature, besides having an arbitrary initial tolerance.

In such a case, a proportional voltage  $V_{REF}$ , derived from the excitation supply, would be applied to the reference input of the AD2010R. The desired normalized ratio,  $\overline{V_{IN}/V_{REF}}$  is equal to the ratio of the displayed number (of counts) to 2000, despite slow variations of the excitation voltage.

## OPTIMIZED NORMAL-MODE REJECTION

An additional feature of the AD2010R is the availability (at the front panel) of an adjustment of clock frequency that allows the normal-mode rejection of the power-line frequency (and its harmonics) to be increased to better than 60dB (i.e., 2 counts). Integrating converters, in theory, totally reject signals having periods of which the integrating period is an integral multiple. In practice, where this property is used to reject power-line frequencies, variations in both clock frequency and power-line frequency, aggravated by the steepness of the null characteristic, conservatively allow only 40dB NMR if preset, as in the AD2010. However, an improvement of 10x (i.e., 20dB) by on-the-spot trimming is feasible with the AD2010R.

Users desiring optimum normal-mode rejection of 50Hz mains frequency should request units bearing the suffix "E", which signifies that the integrating period is nominally 20ms.

Since the clock runs more slowly, all other periods are increased in the same proportion. For example, the drift-correction period becomes 10ms, and the maximum conversion rate ranges from 20 to 33 readings per second.

## ODDS AND ENDS

The display can be connected to suppress "leading" zero's (e.g., 12, instead of 012), an especially useful feature if the decimal point is omitted.

Decimal points can be inserted between any two digits by applying a logic "1" at the appropriate terminal.

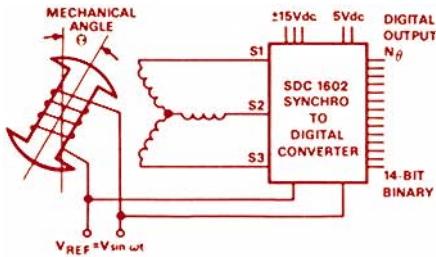
When overloaded, the display flashes 0's.

The AD2010 will sustain 20V continuous overload, 50V momentary overload without damage.



## NEW SYNCHRO/DIGITAL CONVERSION PRODUCTS

### 14-BIT SDC 1602 1' 19" RESOLUTION

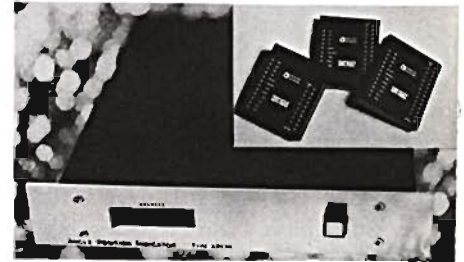


### 10-BIT SDC 1604 21 ARC-MINUTE RESOLUTION

Series SDC 1604\* is available for applications that do not require the exacting 14-bit resolution of the 1602. However, its 10-bit resolution (1024:1) and 30' accuracy are more than adequate for many applications in control and navigation, such as wind-direction measurement, control-surface positioning, and maintaining high resolution over limited angular ranges.

Except for resolution, it is physically and electrically identical to the 1602, but priced for economy at \$480 (1-9).

### 5-DIGIT SYNCHRO ANGLE DISPLAY METER



The API 1617† is an angular-position indicator that provides a LED readout (and a BCD or binary output) of angles from 0° to 359.98° (continuous rotation), with 0.02° resolution and <0.05° error, at tracking speeds up to 1440°/second.

The accuracy specification is maintained over a temperature range of 0 to +50°C, signal-amplitude variations of ±10%, total harmonic distortion up to 10%, line-voltage variation of ±10%, and frequencies from 45Hz to 450Hz.

The BCD output is available with fractional degrees expressed in either minutes or decimal fractions. Inputs are transformer-isolated (500VDC breakdown), available in a choice of ranges. Price is \$1,645 (1-9).

Series SDC 1602\* synchro/digital converters have 14-bit resolution ( $2^{14}=16,384:1$ ), ±1 arc-minute error, 1440°/second tracking rate, and small size (less than 6¾ cubic inches or 110 cm<sup>3</sup>). Rated accuracy is maintained over the full operating-temperature range, ±10% variation of signal and reference voltages, ±10% variation of reference frequency, ±10% total harmonic distortion, and ±5% power-supply variation. The 400Hz signal and reference inputs are transformer-coupled, with 500V breakdown rating.

The continuously-tracking digital output is TTL/DTL compatible (4 TTL loads), there are no external adjustments, and the unit is entirely self-contained, requiring only ±15VDC and +5VDC power supplies. Warmup to rated accuracy is 5 minutes. Despite all these impressive performance features, the unit is fully competitive in size and price (\$680, 1-9).

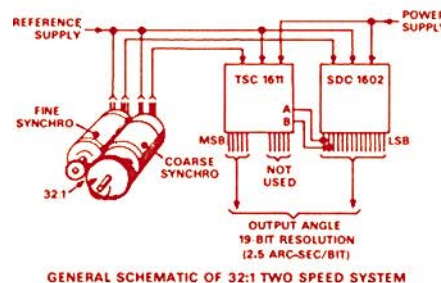
A number of variations of the basic design are available, depending on the input voltage, nominal reference frequency, temperature range, and form of input. The synchro versions accept the three-wire line (and 2-wire reference) configuration shown above. A resolver version, that accepts 2-phase 2-wire inputs, is also available. Various options, embodying the most-commonly-used voltage levels, are available.

\*For information on the SDC 1602, 1604, and 1611, use the reply card. Request J3.

### TWO-SPEED TSC 1611 FOR HIGH RESOLUTION

The SDC 1602 and the 1604 can be used in tandem with two synchros that are geared together, either electrically or mechanically, to obtain increased resolution. In general, a two-speed processor and synchronizing module (TSL (R), where R is the gear ratio) is used. However, if the gear ratio is binary (e.g., 32:1), a version of the SDC 1604, the TSC 1611\*, provides the necessary logic for obtaining combined resolutions up to 19 bits. Price is \$635 (1-9).

The two-speed scheme is analogous to the way a clock face can be used for 43,200:1 visual resolution (the second hand provides 60:1, the minute hand 60:1, and the hour hand 12:1), even though the eye can only resolve (say) 1 part in 60. It is not at all like the "forbidden" scheme described on page 2.



### IDEAL BIT WEIGHTS

Bit No. (n)	Degrees 360° × 2 <sup>-n</sup>	Fractional <sup>1</sup> in Minutes	Fractional <sup>1</sup> in Seconds
1 MSB	180.°	0.	0."
2	90.	0.	0.
3	45.	0.	0.
4	22.5	30.	0.
5	11.25	15.	0.
6	5.625	37.5	30.
7	2.8125	48.75	45.
8	1.40625	24.375	22.5
9	0.703125	42.1875	11.2
10 LSB:SDC 1604	.351562	21.0938	5.6
11	.175781	10.5469	32.8
12	.087891	5.2734	16.4
13	.043945	2.6367	38.2
14 LSB:SDC 1602	.021973	1.3184	19.1
15	.010986	0.6592	39.6
16	.005493	.3296	19.8
17	.002747	.1648	9.9
18	.001373	.0824	4.9
19 LSB:SDC 1602 & TSC 1611	.000687	.0412	2.5

<sup>1</sup> Two-Speed Connection (32:1)

†For information on the API 1617, use the reply card. Request J3.

## FAST HIGH-RESOLUTION A/D CONVERTERS

### ADC1103: 12 BITS IN 3.5 $\mu$ s

The ADC1103 series\* consists of three high-speed A/D converters, encapsulated in compact 2" x 4" modules:

- The ADC1103-003 performs a complete 12-bit conversion in 3.5 $\mu$ s maximum, a new high-water mark in speed x resolution among Analog Devices converters. The table facilitates a comparison with our most-popular 12-bit types.
- The ADC1103-002 performs a 10-bit conversion within 1.2 $\mu$ s. It is a compact modular low-cost replacement for the venerable ADC-10F.
- The ADC1103-001 converts to 8-bit resolution within 1 $\mu$ s. It is a low-cost successor to the ADC-8F for most applications.

### APPLICATIONS

These successive-approximation converters were designed for applications requiring high throughput rates. Typical examples range from obtaining a maximum number of samples in a single channel to converting a number of multiplexed channels at a respectable throughput rate per-channel.

When the ADC1103-003 is used with the SHA-2A sample/hold, the total conversion time for 12 bits is less than 4.5 $\mu$ s, which permits a quite-comfortable 200kHz throughput rate.

The figure shows the use of an ADC1103 with a SHA-2A sample/hold and an

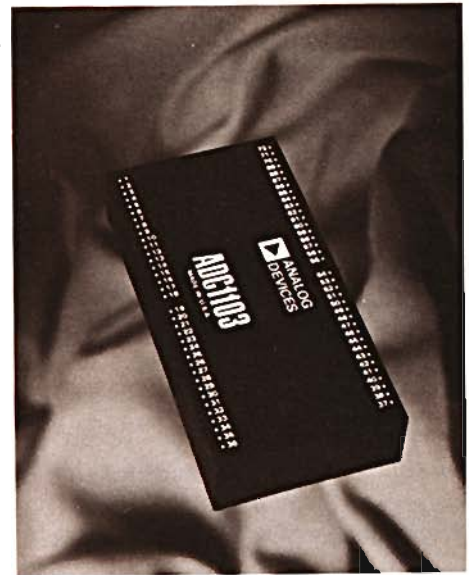
MPX-8A multiplexer in an 8-channel sequentially-multiplexed configuration. When a conversion is initiated, the *status* line indicates that the converter is "busy," switches the SHA-2A to *hold*, and indexes the multiplexer to the next position. At the end of conversion, the *status* output indicates that data is valid, and switches the SHA-2A to *sample*, in preparation for the next conversion command.

### ADC1103 CHARACTERISTICS

The ADC1103 has differential nonlinearity less than  $\pm\frac{1}{2}$ LSB at +25°C, with a temperature coefficient small enough to ensure that there will be no missed codes over the temperature range 0 to +50°C.

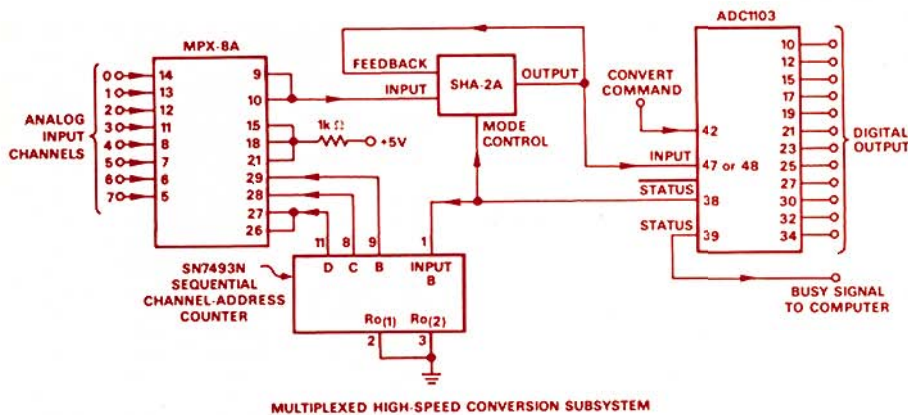
The analog input voltage range can be programmed by the user via a choice of jumpers; three ranges are available:  $\pm 5$ V,  $\pm 10$ V (offset binary or 2's complement), and 0 to +10V.

All logic inputs and outputs are of course TTL-compatible, and the data outputs are positive-true binary. Power requirements are  $\pm 15$ VDC @ +85/-80mA and +5VDC at about 500mA. Overall case dimensions are 2" x 4" x 0.75"H (5.08cm x 10.16cm x 1.01cm). Prices are: ADC1103-001, \$430; -002, \$440; -003, \$450 (1-9), with substantial discounts in quantity.

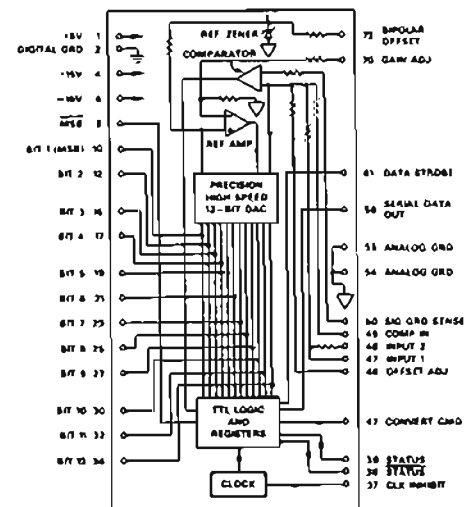


### COMPARATIVE SPECIFICATIONS

	ADC 1103-003	ADC 12QU	ADC 12QM	ADC 12QZ
Resolution (bits)	12	12	12	12
Conversion time ( $\mu$ s, maximum)	3.5	15	25	40
Nonlinearity (% maximum, +25°C)	$\pm 0.0125$	$\pm 0.0125$	$\pm 0.0125$	$\pm 0.0125$
Temp. coefficients				
Diff. nonlinearity (ppm F.S./°C, max)	$\pm 5$	$\pm 5$	$\pm 5$	$\pm 10$
Scale factor (ppm/°C, max)	$\pm 10$	$\pm 5$	$\pm 5$	$\pm 30$
Zero ( $\mu$ V/°C, max)	$\pm 50$	$\pm 50$	$\pm 50$	$\pm 100$
Power-supply rejection (%/V, typ)	$\pm 0.003$	$\pm 0.002$	$\pm 0.002$	$\pm 0.002$
Price (1-9)	\$450	\$315	\$305	\$129



Multiplexed High-Speed Conversion Subsystem



Block Diagram of the ADC1103

\*For complete information on ADC1103, use the reply card. Request J4.





## FOUR NEW IC OPERATIONAL AMPLIFIERS

### AD509: FAST OP AMP 2 $\mu$ s MAX TO 0.01%



The AD509J, AD509K, and AD509S\* are monolithic op amps specifically designed for applications calling for fast settling time to low error levels.

The AD509K and S are 100% tested to guarantee settling time of 500ns *max* to 0.1% and 2 $\mu$ s *max* to 0.01%. Typical response includes 120V/ $\mu$ s slew rate, full-power bandwidth of 1MHz and small-signal GBW 20MHz.

As befits a fast op amp, minimum full-power output is  $\pm 10$ mA at  $\pm 10$ V ( $\pm 15$ V supplies). The AD509 is stable for all values of closed-loop gain  $> 3$ , and it can be stabilized for any value of closed-loop gain (resistive loading and feedback) with a single external capacitor to ground.

Maximum offset current (AD509 K&S) is 25nA at +25°C, 50nA over the full temperature range. Open-loop gain is 10k *min*, CMR is 80dB *min*, and average offset drift is typically 20 $\mu$ V/°C.

### APPLICATIONS

The AD509 is ideal for use in data-acquisition, data-distribution, and sampled-data systems, where fast response and high output capability are required. Unlike feedforward types, such as AD301A and the AD505, it may be operated in non-inverting or differential (as well as inverting) configurations, without compromising performance.

All three types are supplied in TO-99 hermetically-sealed packages. The AD509J and AD509K are specified for operation from 0 to +70°C; AD509S is specified for operation from -55°C to +125°C. Prices (100's) are AD509J: \$8.50; K: \$12.50; S: \$19. **▶▶▶**

\*For complete information on the AD509 series, use the reply card. Request J6.

### AD504M: LOWEST NOISE AND DRIFT

Nearly two years of successful production of the AD504 series (a monolithic thin-film-on-silicon op amp, first announced in these pages in Vol. 5, No. 3), plus recent processing improvements, have resulted in the lowest-drift, lowest-noise IC operational amplifier available (to our knowledge) on the market: the AD504M.†

Specifications (*max*) include: 0.5 $\mu$ V/°C nulled drift, 0.6 $\mu$ V(p-p) noise (0.1-10Hz), 13nV/ $\sqrt{\text{Hz}}$  at 10Hz, 10nV/ $\sqrt{\text{Hz}}$  at 100Hz, and 9nV/ $\sqrt{\text{Hz}}$  at 1kHz. These specifications are confirmed by 100% testing.

In addition, the AD504M retains all the other excellent characteristics of the Analog Devices AD504 family, including fully-protected input, single-capacitor compensation,  $f_T$  of 300kHz, and 1.2V/ $\mu$ s slew rate (gain-of-10).

The AD504M is ideal for high-precision applications calling for error budgets in the parts-per-million category, such as stable references, precision instrumentation and analog computing. Naturally, it is ideally suited for numerous low-level applications, such as in precision measurement, telemetry, and data acquisition. Price in 100's is \$22. **▶▶▶**

†For complete information on AD504M and other members of the AD504 family, request J7.

§For complete information on AD507S and other members of the AD507 family, request JB.

### AD506L: ECONOMICAL LOW-DRIFT FET-INPUT

The AD506L‡ is a FET-input counterpart of the AD504M (mentioned in an adjacent column). It combines the low bias-current of FET-input op amps with a degree of offset stability commonly found only in bipolar devices. Closely-matched and carefully-controlled input characteristics, enhanced by internal laser trimming, include  $\pm 1$ mV maximum offset voltage and 5pA bias current. These specifications are realized with the unit fully warmed up (i.e., the way you normally use it). Offset drift is 10 $\mu$ V/°C maximum. Each AD506L is burned-in for at least 48 hours to ensure offset-voltage stability.

Open-loop gain is 75,000 minimum, CMR is 80dB minimum, and compensation is internal. These devices will tolerate output short-circuits to ground, and they are free from "latchup."

The AD506L is especially designed for applications involving the measurement of either low-level currents or small voltages from high-impedance sources, as well as other applications in which bias currents can be a primary source of error, but drift must be low as well. Price is \$16 in 100's. **▶▶▶**

‡For complete information on the AD506L and other members of the AD506 family, request JB.

## AN AD507 FOR -55°C TO +125°C

The AD507S§ is a wide-temperature-range version of the low-cost general-purpose AD507, announced in these pages in Vol. 6, No. 1. It combines a gain-bandwidth of 100MHz and slew rate of 25V/ $\mu$ s with maximum offset and bias currents below 15nA, and maximum offset voltage below 4mV. Voltage drift is

$< 20\mu\text{V}/^\circ\text{C}$  over the temperature range. No compensation is needed for closed-loop gains  $> 10$ .

Designed for fast, general-purpose applications, it can be used as a comparator, integrator, or wideband amplifier, and for sample-holds. Price in 100's is \$15. **▶▶▶**

## NOT BY DRIFT ALONE . . .

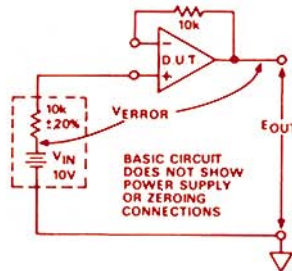
### Chapter 2. The 741 Op Amp Family by Stan Harris

In Vol. 6, No. 2 (p. 12), we developed the thesis that for practical high-precision applications, the drift spec of an operational amplifier was but one of the specifications affecting accuracy, and not always the most important one at that.

We offered an example involving a simple unity-gain follower unloading a 10V precision signal source with an internal resistance of  $50k\Omega \pm 10\%$ . An error budget compared the worst-case errors of a number of commercially-available comparably-priced "low-drift" op amps. It was gratifying (but hardly surprising) to find that the AD508H\*, with its balanced optimized design, won handily over such competitors as the LM208AH, the SSS725EJ, and the BB3500E. What *was* a bit surprising, however, was to find that the AD741KH, costing less by an order of magnitude, was *not* the worst of the lot.

Thus encouraged, we decided to take a closer look at the 741\* family. Besides the common, garden variety (AD)741 and (AD)741C, at their rock-bottom prices, Analog Devices also makes the higher-performance AD741J, AD741K, AD741L, and AD741S, for which only modest premiums are exacted.

We used for the comparison a unity-gain follower circuit, driven by a source having internal resistance of  $10k\Omega \pm 20\%$ , and using a nominal  $10k\Omega$  bias-current compensating resistance in series with the negative input terminal. The results of the error-budget comparison are shown in the table. For performance over the commercial temperature range, the AD741K has better than 5X less error than 741C at  $2\frac{1}{2}X$  the cost. Over the full "MIL" range, the AD741S has  $3\frac{1}{2}X$  less error than 741 at less than twice the cost.



#### WHAT IS A 741? (AN ANALOG DIATRIBE)

Users of 741's take them for granted: 741, 741C, TO-99, can, minidip, use them anywhere, get them anywhere, same specs, at the cheapest price. After all, a 741 is a 741 is a 741 . . . Right?

Not quite.

The  $\mu A741$ , as the historically-minded may recall, was Fairchild's answer to the National LM101A. Both were successful 2nd-generation op amps, but the 741 became the more popular (except for wideband applications) because of its internal compensation. Soon the number of suppliers of 741's mushroomed: five, ten, fifteen? twenty? It became the product with which a new supplier broke-in his linear process capability.

Curious thing about these suppliers: some make a pretty good 741; some make a pretty bad 741; some don't make a 741 at all. This isn't just a qualitative feel; there's hard engineering data to back it up. We can distinctly recall an evaluation of yet-another-741 by one of our engineers: "It's a good op amp . . . and if I were still designing systems, I might even use it . . . but it sure isn't a 741!" Call it I.C. design license; there are enough processing and design variations in existence to strongly suggest a policy of *caveat emptor* on the next "standard" 741 you meet. Here are a few manifestations of variety:

- **Noise** (to wit, *popcorn noise*, the erratic jump of bias current between two levels at random intervals). This kind of noise is process-oriented, and the fraction of units that exhibit it varies from lot to lot, but, in general, the manufacturers — both large and small — that supply low-noise 741's tend to do so consistently; and the guys that don't — again, both large and small — also tend to be consistent (sometimes with amplitudes as high as  $150\mu V/100k\Omega = 1.5nA$ ).
- **AC Performance** Some 741's are said to be faster than the "ordinary" standard 741. One wonders whether this is by intent or by accident, since all it takes is a thicker oxide layer (i.e., less C) in the compensating capacitor. The fewer the pF's, the faster the device, but . . . the price you pay is possible instability (a) in tight feedback loops, or (b) if your circuit application has parasitic capacitive loads that a "slow" standard 741 takes in its stride. Such devices, in our book, are *not* 741's.
- **Offset and drift** The practice observed by all 741 manufacturers, of specifying a standard 741 (or 741C) for competitive purposes, deprives users of the highly-desirable  $\Delta V_{OS}/\Delta T$  voltage-drift spec. However deplorable, it is an economic necessity: if you don't have a spec, you don't have to reject a  $60\mu V/^{\circ}C$  device for not meeting a  $25\mu V/^{\circ}C$  spec. The dilemma for the good guys is: if you have a process that can usually be depended on to produce mostly  $10\mu V/^{\circ}C$  units, how do you give your customers the benefit of the better spec, still remain price-competitive, and maintain some protection against "off" days?

ERROR BUDGET ANALYSIS

PARAMETER		0 to +70°C				-55°C to +125°C	
		AD741C	AD741J	AD741K	AD741L	AD741	AD741S
Gain (G, V/V)	SPEC	15,000	25,000 <sup>1</sup>	25,000	25,000	25,000	25,000 <sup>1</sup>
Gain error (10 <sup>3</sup> $\mu V/G$ )	ERROR	650	400	400	400	400	400
$I_b$ (nA)	SPEC	800	400	120	100	1,500	250
$I_b \times R$ mismatch ( $\mu V$ )	ERROR	1,800	800	240	200	3,000	600
$I_{OS}$ (nA)	SPEC	300	100	16	10	600	75
$I_{OS} \times 10k\Omega$ error ( $\mu V$ )	ERROR	3,000	1,000	160	100	6,000	250
$\Delta V_{OS}/\Delta T$ ( $\mu V/^{\circ}C$ )	SPEC <sup>2</sup>	25	20	15	5	25	15
$\Delta V_{OS}$ over temp. ( $\mu V$ )	ERROR	1,125	900	875	225	2,500	1,500
CMR = 20logCMRR (dB)	SPEC	70	80	90	90	70	80
CME = 10V/CMRR	ERROR	3,160	1,000	318	318	3,160	1,000
PSRR ( $\mu V/V$ )	SPEC	150	100	15	15	150	100
ERROR = 3 $\times$ PSRR ( $\mu V$ ) <sup>3</sup>	ERROR	450	300	45	45	450	300
Total (Algebraic)	ERROR ( $\mu V$ )	10,000	4,400	1,800	1,300	14,500	3,950
Total (RMS)	ERROR ( $\mu V$ )	4,800	1,900	890	600	7,100	1,950
PRICE (100's) U.S.		\$1.00	\$1.25	\$2.25	\$6.00	\$7.00	\$3.20

<sup>1</sup> For  $\pm 10V$  output into 1k $\Omega$  load.

<sup>2</sup> Not specified as a ratio, typical 741 and 741C.

<sup>3</sup> Assuming +5% power-supply change,  $2 \times 15 \times 0.05 \times 3 \times PSRR$ .

\*For information on AD508, and the AD741 family, request J10.

*continued on page 12*

20 $\mu\text{V}/^\circ\text{C}$  specification (and other improved specs) AD741J, price them just a few cents higher, and still compete for the penny-pinching "don't-care" market with an AD741C (which is often a much better device than its name would indicate, but then again . . .). The beauty of this approach is that, as a bonus, we also get 15 $\mu\text{V}/^\circ\text{C}$  AD741K's and 5 $\mu\text{V}/^\circ\text{C}$  AD741L's, with other specs tightened, as the table shows. We also get much better feedback about our process from the large number of units that get extra testing. And finally, we get to publish some of the most-informative data sheets in the business.

A note to the user: with op amps that use simple differential-pair bipolar-transistor inputs, the lowest drift is experienced at the lowest offset. As the offset voltage is nulled out, the reduction of drift is commonly given as 3.3 $\mu\text{V}/^\circ\text{C}/\text{mV}_{\text{OS}}$ . However, the 741 has a somewhat more-involved input circuit, and zeroing the amplifier may actually worsen the drift (then again, it may improve it, but we have to take Murphy's Law into account). Thus if low (e.g., zero) offset and low drift are needed, and the budget calls for a 741, the AD741K (2mV max) or the AD741L (0.5mV max) may be the answer for the commercial temperature range, and the AD741S (2mV max) for the "MIL" range.

- The dismal effects of economics The price-vs.-time curve for the 741 has been an apparent blessing to users; for producers, it has been a mixed curse, rewarding the efficient or the agile, penalizing the inefficient or the straightforward. Since profit (equal to price minus cost) is a key objective of producers, maintaining the equation's polarity positive requires that cost decrease as price decreases.

Sometimes, to keep cost coming down, a highly-motivated production manager might find it necessary to omit certain manufacturing cost items, such as 100% testing, or relax the test-limit guard bands, or loosen the AQL at outgoing Q.C. Don't scoff — it happens! If production efficiencies, that normally are realized by moving up the learning curve, don't occur, then corner cutting may appear to *some* to be the only way to keep profit margins reasonable (or, at least, positive). This may help to explain why — on an industrywide basis — as the price of the 741 has decreased, its quality appears to have declined (measured by increased lot rejections at users' incoming Q.C. and more field failures in systems).

Where does all this lead?

To a sober realization that many design engineers, component engineers, and buyers tend to regard use of the 741 as one regards breathing, or the ticking of a clock. That is, they don't pay much attention at all, until breathing gets difficult or the clock stops . . . until the old reliable 741 they were so familiar with is no longer reliable (or even familiar), the apparent saving due to the price war is no longer a saving, the new supplier's 741 doesn't act as it should, and the new design could use a little more accuracy than the standard 741 is specified to give.

The smart buyer no longer buys 741's on price alone (the cost of potentially-lower quality is more than a few cents per unit) but looks for variations of the 741 that are a cut above the average, and must have required extra care to be so identified.

Meet the AD741J, AD741K, AD741L, and AD741S!



# THE AD520: NOT AN OP AMP BUT AN INSTRUMENTATION AMPLIFIER

What is an instrumentation amplifier?

It is a device that accepts a voltage signal as an input and produces a linearly-scaled version at the output. It is a *closed-loop, committed, fixed-gain* amplifier, usually *differential*, with *high input impedance, low drift*, and *high common-mode rejection* over a wide range of frequencies; it is characterized by a set of specifications that describe *overall performance*.

The AD520\*, introduced in Vol. 6, No. 1, is the only monolithic I.C. instrumentation amplifier known to us. However, there have been a number of monolithic I.C. amplifiers offered on the market as "instrumentation operational amplifiers," usually so-called because of their low drift or high CMR. However, it must be clearly understood that they are *open-loop, uncommitted, high-open-loop-gain* devices that must usually be connected in pairs or triads in a circuit involving a number of precision resistors, in order to work as instrumentation amplifiers. Furthermore, their specifications describe the *basic device performance*.

By the time they have been adapted to the application, a number of compromises will have been made that adversely affect cost, complexity, or performance of the assembled closed-loop, committed, fixed-gain circuit. In effect, the *user* (not the manufacturer) must be able to guarantee the overall performance.

By contrast, the AD520K, with a pair of low-T.C. resistors and a few added components (mostly capacitors) with non-critical parameters (Figure 1), will provide gain-of-1000 with CMR = 106dB (min, 1k $\Omega$  source unbalance, 0-100Hz), drift = 5 $\mu\text{V}/^\circ\text{C}$  (max, r.t.i.), slew rate = 2.5V/ $\mu\text{s}$  (min),  $I_b = 40\text{nA}$  (max), at a device cost of \$16 (100's).

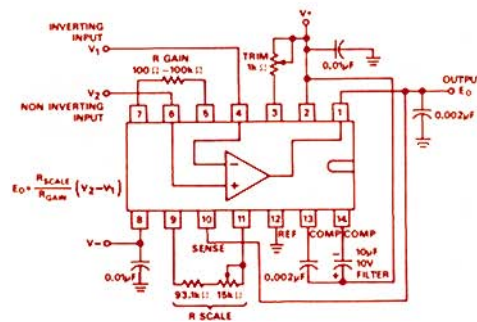


Figure 1. The AD520 in a Typical Application, Showing All Auxiliary Components

An interesting feature of the AD520 is the pair of feedback terminals, labeled *Sense* and *Reference*. They can be used to provide an output bias, current-controlled output (either floating or grounded), and high output current (via an inside-the-loop booster follower) without affecting accuracy. The already low drift can be reduced further by chopping the input signal and using the *Sense* and *Reference* terminals, with a *hold* circuit, to null out input offsets in the *feedback* circuit, without affecting response speed during the *hold* interval. More information on this technique will appear in a future issue of *Dialogue*.



\*For complete data (including 2 pages of specifications) on the AD520, use the reply card. Request J11.

## 30dB AUTOMATIC GAIN CONTROL WITH THE AD531

The circuit of Figure 1 will maintain 3V peak-to-peak output for inputs ranging from 0.1Vp-p to more than 12Vp-p, with better than 2% regulation from 0.4Vp-p to 6Vp-p, and distortion well below 1%. Input frequency can range from 30Hz to 400kHz (-3dB). The level is adjustable either manually or by an external dc reference voltage. The input signal can be either single-ended or differential.

The feedback circuit works in a straightforward manner: if the input signal increases, the output will tend to increase. Its negative peaks, as recognized by the diode and stored on the 1μF capacitor, tend to increase, causing the output of the inverting integrator to increase. This, in turn, causes the denominator to increase, reducing the gain of the AD531 multiplier/divider (XY/I), and tending to keep the output level constant.

In the steady state, the average voltage at point A must be ideally equal to one-half the voltage at point B, but of opposite polarity, making the net input to the integrator equal to zero, and holding the output of the integrator at whatever constant level is necessary to keep the loop in balance. In that state, the negative peak value of  $E_{out}$  is approximately one diode drop below  $V_A$ , so

$$|E_{out}(\text{peak})| \cong \frac{1}{2}V_B + \text{diode drop}$$

In practice, the *set level* potentiometer would be adjusted empirically to calibrate the output at the desired level.

In the simple practical example given here, to illustrate the principle, an unembellished half-wave diode-and-capacitor circuit reads the peak level of the waveform. Naturally, other properties of the waveform, such as mean absolute value or RMS might be used as a measure; also, somewhat more sophisticated temperature-compensated rectification circuitry might be used.

The control voltage ( $V_C$ ) at the output of the amplifier ranges from about -2V (lowest AD531 gain) to the amplifier's lower limit, -13.5V (to handle the smallest input signals). Linearity of  $V_C$  is not important, since it is a manipulated variable inside the loop.

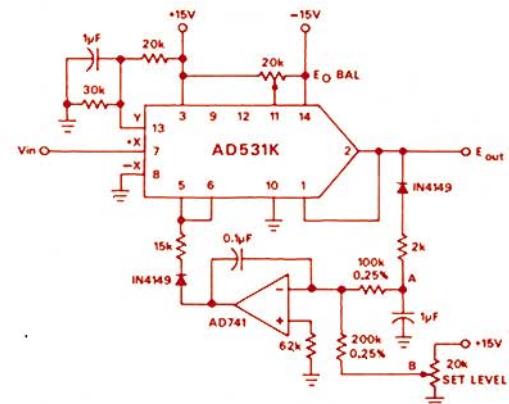


Figure 1. Automatic Gain Control Using the AD531 Has ~30dB Dynamic Range of Input

## TRUE RMS MEASUREMENT USING THE AD531

by Lew Counts

To determine the RMS value of a stationary waveform, most low-cost (and a few expensive) "RMS" meters simply measure the average of the absolute value of the input, using a full-wave rectifier, then multiply it by 1.111, the ratio of RMS: Average for sine waves. Though valid for undistorted sine waves, this approach leads to substantial errors with random noise, triangular waves, or square waves (but they may be calibrated), and to even worse errors with arbitrary waveforms, for which no calibration is possible. For a train of zero-based square pulses, the error is proportional to  $\sqrt{(\text{duty cycle}) - (\text{duty cycle})}$ . Figure 1 shows the error as a function of firing angle for an SCR circuit.

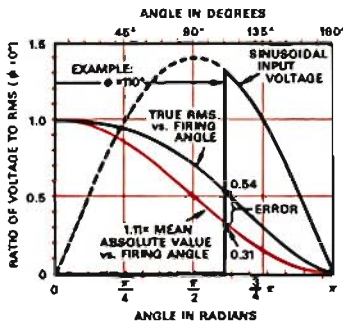


Figure 1. RMS and Mean Value of Ideal Full-Wave SCR Output as a Function of Firing Angle  $\phi$

A better way is to use a true-RMS circuit. A simple low-cost implementation, involving the AD531K\* (a monolithic IC multiplier/divider: XY/I), two AD741 op amps, and a few miscellaneous components, is shown in Figure 2. It is a feedback loop, embodying the implicit relationship,  $V_{in}^2/E_{out} = E_{out}$ , whence  $E_{out} = \sqrt{V_{in}^2}$ , if RC is a sufficiently-long time constant.

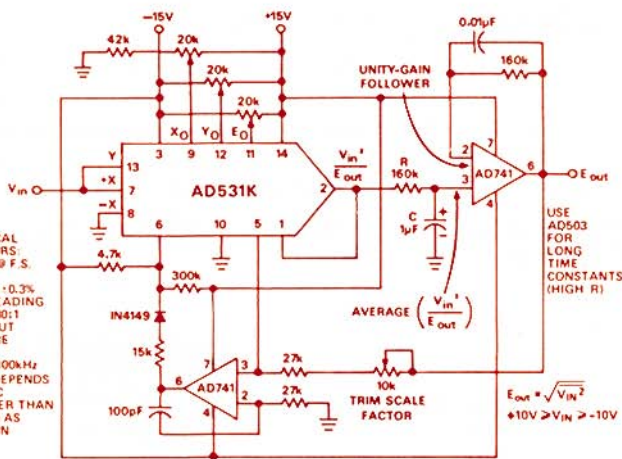


Figure 2. True-RMS-to-DC Converter Using AD531

\*For complete information on the AD531, use the reply card. Request J12.

# Application Briefs

## VECTOR DIFFERENCE $\sqrt{V_a^2 - V_b^2}$ WITH THE AD531

The square-rooting properties of 3-variable analog multiplier-dividers, such as the AD531 and the 433\*, by the feedback solution of an implicit equation (e.g., the RMS circuit, page 13), have led to some interesting uses in vectorial combination. Vector sums were discussed at length in *Dialogue*, Vol. 6, Nos. 2 & 3. The key to the scheme: if  $u^2 + v^2 = w^2$ , then by subtraction and factoring,  $u^2 = (w + v)(w - v)$ . Dividing both sides of the equation by  $(w + v)$ , one can easily recognize an implicit solution for the vector sum,  $w$ , that can be embodied with an XY/I device and 2 op amps. If instead, both sides of the equation are divided by  $u$ , a solution for the vector difference appears:

$$u = \frac{(w + v)(w - v)}{u} = \sqrt{w^2 - v^2}$$

A practical circuit that embodies this equation simply with the monolithic AD531 is shown in Figure 1. Since the X input of the AD531 is a differential input—and the sum can be obtained passively—the only necessary external operational amplifier is an AD741, to convert the fed-back output from a voltage to a current.

When properly calibrated and adjusted for less than 100mV error at full scale, the output will differ from the theoretical value by less than  $\pm 100\text{mV}$  for any pair of input voltages over an output dynamic range between  $10\text{V}:0.3\text{V}$  and  $10\text{V}:0.1\text{V}$ . Bandwidth is DC to 100kHz for best accuracy, and 600kHz for -3dB.

### CALIBRATING THE CIRCUIT

Step	Condition	Adjust	For
1.	CAL. $V_a = V_b = 0\text{V}$	$E_0$ BAL	$E_0 = 0\text{V}$
2.	CAL. $V_a = 20\text{Vp-p}$ , 10Hz, $V_b = 0\text{V}$ Pin 13 (AD531) grounded	Y BAL	Min. $E_0$ swing
3.	CAL. $V_a = V_b = 0$ , 20Vp-p to pin 13 Scope sensitivity as in (2)	X BAL	Min. $E_0$ swing
4.	OPERATE. $V_a = 10.00\text{V}$ , $V_b = 0\text{V}$	GAIN	$E_0 = 10.00\text{V}$
5.	OPERATE. $V_a = 1.00\text{V}$ , $V_b = 0\text{V}$	"Low end"	$E_0 = 1.00\text{V}$
6.	OPERATE. $V_a = V_b = 0\text{V}$	$E_0$ BAL	$E_0 = 0\text{V}$

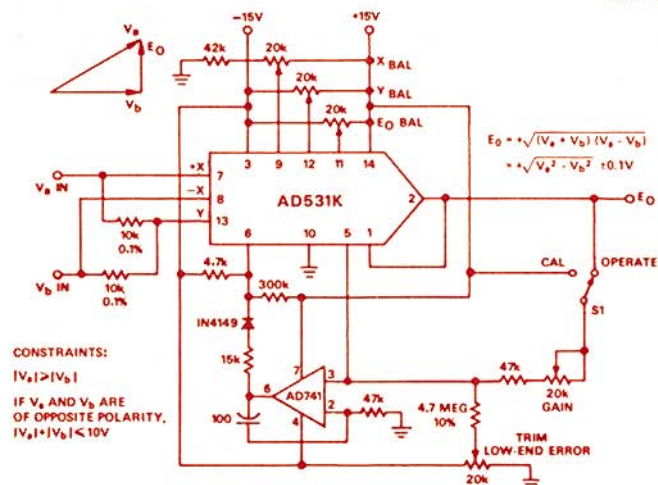


Figure 1. Vector-Difference Circuit Using AD531

\*For technical information on Model 433, use the reply card. Request J13.

## A LOW-NOISE, LOW-DRIFT FET-INPUT AMPLIFIER DESIGN

If you want a low-drift-and-noise operational amplifier for low-frequency, high-impedance applications at minimal cost, is it better to make your own or buy a complete, fully-guaranteed unit? It would be hard for us to make a judgment, unless we know your aptitudes and cost structure. On the other hand, you can know both your own capabilities and our price. In any event, we are equally gratified if the choice is between our 43K (best drift-and-noise vs. price), 40J, or AD503 (low price), and an amplifier that you can build with an AD840 dual-FET, an AD301A op amp\*, and a small handful of components.

Yes, you can build a rather formidable amplifier at low cost.

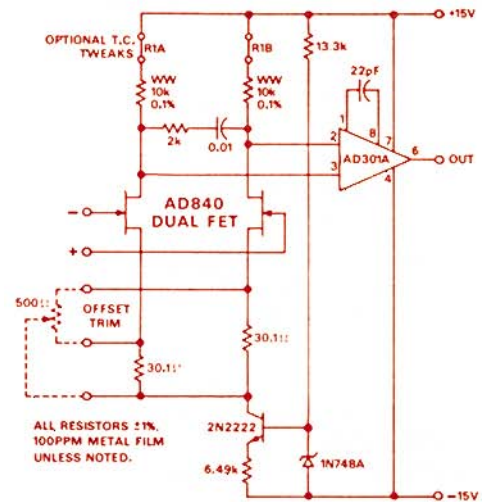


Figure 1. Low Noise Low Drift FET Input Amplifier Using AD840 Dual FET

How do these characteristics sound?

- Offset vs. temperature:  $5\mu\text{V}/^\circ\text{C}$  (tweakable to  $1\mu\text{V}/^\circ\text{C}$ )
- Noise:  $1\mu\text{Vp-p}$  (0.1 to 10Hz),  $8\mu\text{Vrms}$  (5Hz to 10kHz)
- Bias current: 10pA, either input
- CMR: 80dB (-10V to +9V)
- Bandwidth: 700kHz (small-signal, unity gain), 15kHz fp
- Full-power output:  $\pm 10\text{V}$  @  $\pm 5\text{mA}$

They describe the performance of the amplifier shown in Figure 1. The photographs (Figure 2) compare its low-frequency noise with that of a popular I.C. FET-input amplifier that happened to be on the bench. The key to the excellent performance is the AD840 dual FET, with its  $3\mu\text{V}/^\circ\text{C}$  max temperature-drift nonlinearity, introduced in Vol. 6, No. 3 of *Dialogue*.

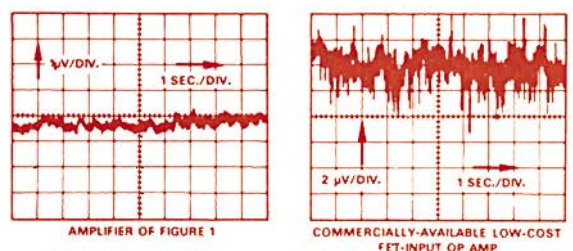


Figure 2. Typical Noise Waveforms DC to 10Hz

\*For technical and price information on all of these devices, request J14.

## LAST ISSUE OF *ANALOG DIALOGUE*

Vol. 6 (1972), No. 3

If you haven't seen the last issue of *Dialogue*\*, here's what you've missed

- Root-Sum-of-Squares Circuits with the 433
- Trigonometric Operations with the 433 (The Powers of Non-Integral Exponents)
- Gate Responses Simplified (A Guide for the Occasional User of Logic)
- Two New Digital Panel Meters
  - 4½-Digit AD2004 Has Floating Input, LED Display
  - 3½-Digit AD2003 Has Differential Input, \$93 in 100's
- Modular Multiplier, Op Amp, Power Supply
  - 10MHz Model 429B Has Less Than 0.5%dc Error, Internally Trimmed
  - Performance/Price (= Value) Maximized in Model 43 FET Op Amp
  - 920 Power Supply: ±15VDC @ ±200mA
- Modules Are At Home in Converter Manifold Boards
  - Subsystem Assembly is Simplified for \$75
- Monolithic I.C. Analog Multiplier-Dividers
  - New AD531 Computes XY/Z: True Output Polarity for ±X, ±Y
  - Two New AD530 Versions: 0.5% AD530L, -55°C to +125°C AD530S/883
  - AD530D: Multiplier in a Hermetic Ceramic Dual In-Line Package
- Two Dual Transistors and a TRAK-FET™
  - Super-β Dual Has  $h_{FE} > 2000$ ,  $V_{CEO} > 20V$  (AD814, 815, 816)
  - Monolithic AD818 Has Excellent Log Conformity
  - Monolithic Dual FET's (AD840) Have Low Drift and Noise
- AD540 FET-Input Op Amp a "Best Buy" (\$4.90 in 100's)

**Erratum:** You've also missed a systematic mistake on page 10 of that issue, that we didn't notice until it was too late to fix: In all AD531 application diagrams, the  $X_0$  pot should be connected between  $+V_s$  and a 42-47kΩ resistor to ground, as shown correctly on pages 13 and 14 of this issue, as well as on the AD531 data sheet. (Unlike the AD530, the AD531's  $X_0$  adjustment is *not* connected from  $+V_s$  to  $-V_s$ .)

## BOOK REVIEW

*OPERATIONAL AMPLIFIERS*, by G. B. Clayton, 1971, 235 pages, 195 illustrations, Butterworth & Co. (Publishers) Ltd., London: 88 Kingsway WC2B 6AB, £3.50 (U.K. price)

One thing the world has long needed is a good practical down-to-earth textbook on operational amplifiers. It need wait no longer. Mr. Clayton, who is Principal Lecturer and Assistant Head of Department in the Department of Physics of the Liverpool Polytechnic, has written the kind of book that, with only a few modifications, we wish we had written.

The chapter headings give some inkling: Fundamentals, Operational Amplifier Specifications, Amplifier Testing and Measurement of Parameters, Applications (Basic Amplifier Circuits), Extension of Basic Circuits, Integrators and Differentiators, Switching and Positive-Feedback Circuits, Measurement and Instrumentation, Practical Considerations (including amplifier selection, check list, importance of error parameters, general circuit techniques, and external passive elements). Each chapter is followed by a set of practical exercises (answers are provided.)

\*If you haven't seen or would like an additional copy of Vol. 6, No. 3, use the reply card. Request J15. If you're in a hurry, request specific products of interest by model number or name.

It is useful, not only as a textbook, but as an everyday guide and reference for anyone who applies operational amplifiers.

D.H.S.

## A SOMEWHAT PARTISAN COLLECTION OF RECENT ITEMS OF INTEREST

(Available upon Request By Title, Unless a Readers' Service Number is Provided)

*Applying the AD504 Precision IC Operational Amplifier*, Application Note, Request J7

*Complete Monolithic MDSSR* (Multiplier-Divider-Squarer-Rooter), AD530 Technical Bulletin

"Computational Module Stresses Applications Versatility," by Lew Counts and Fred Pouliot, reprint from *Electronics*, March 27, 1972, Request J13

*Dual-Slope Integrating Analog-to-Digital Converters*, ADC-1 Application Note, Request J2

"How to Really Look at Low-Drift IC Op Amps," by Stan Harris, reprint from *Electronics*, October 9, 1972, Request J10

"New Applications Open Up for the Versatile Isolation Amplifier," by C. Peter Zicko, reprint from *Electronics*, March 27, 1972, Request J18

*Product Guide Supplement*, Analog Devices, Request J16

*Short-Form Guide to Linear Integrated Circuits*, Request J17

"Sixteen-Bit Data Conversion," by Wayne Marshall and Cyril Brown, a 2-part article reprinted from *Electronics*, September 25 and October 9, 1972, Request J20

## THE A-D CONVERSION HANDBOOK REVISITED Errata and Other Notes

It's not easy to print many thousands of copies† of a 400-page technical book without errors and occasional mishaps. Here are a few of the substantial anomalies reported so far:

1. Page I-25, Figure 5c, the third term of the equation is  $+0.5 V_x^3/100$ .
2. Page II-29, Table 12, Digital Code, D/A Converters, Input: *Serial* or parallel
3. Page II-138, last line under *Differential Nonlinearity*, each step is  $(1 \pm 1/2)$ LSB.
4. Index, page xvii, Amplifier, isolation, listing should be I-4, 15, 82, III-31, 32, 40-42
5. Bindery error: We've had reports that pages I-87 to II-2 were missing in a few copies. If you have such a copy, return it to us, and we'll send you a new (complete) one, unless you believe yours will become a valuable collectors' item.

We've found other minor typographical errors, but nothing that appears serious or remarkable. Naturally, we invite readers to send us details of any mistakes that might cause inconvenience or tend to impeach our credibility.

D.H.S.

†Copies are still available at \$3.95. Send a check to Analog Devices, Inc., P.O. Box 796, Norwood, Mass. 02062. Or, for convenience, you may write "Bill me \$ \_\_\_ for \_\_\_ copies," accompanied by your initials, on the reply card.

# Four new linear integrated circuits worth talking about. Again.



Maybe you remember our ads which introduced some of our new integrated circuits this year.

Better yet, maybe you sent for our product information and evaluation samples.

A lot of people did because sales have been excellent.

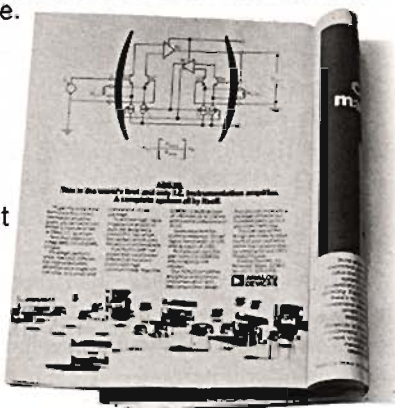
And that's because everything we said about their performance was absolutely true.

Our AD508. No one else gives you this kind of long term drift performance.

Our AD520. The world's first and only I.C. instrumentation amplifier. A complete system all by itself.

Our AD523. It has the lowest bias current of all high performance I.C. operational amplifiers.

Our AD830 dual monolithic FETs. Their performance is so revolutionary, we gave them a new name and came up with a new way to measure them.



They're all worth talking about again so you'll get an idea of the kind of linear I.C.'s we make: multipliers, FET input op amps, high performance op amps, A/D and D/A conversion components, dual monolithic transistors.

And so you'll know what to expect from us.

We'll be using innovative FET, bipolar, and CMOS technology to give you the special and often unique performance you're looking for. At a reasonable price.

It isn't going to be all that hard to do when you look at what we've already done.

We enjoy the leadership position in analog circuitry.

We'd be happy to send you all the details on our four new integrated circuits. As well as our Product Guide which shows the rest of our

I.C. line and all the other things we make to solve more of your problems better than anyone else.

Analog Devices, Inc., Norwood, Mass. 02062 (617) 329-4700



 **ANALOG DEVICES**

FOR INFORMATION, USE REPLY CARD

AD508: Request J19

AD523: Request J21

ALL FOUR:

AD520: Request J11

AD830: Request J22

Request J23